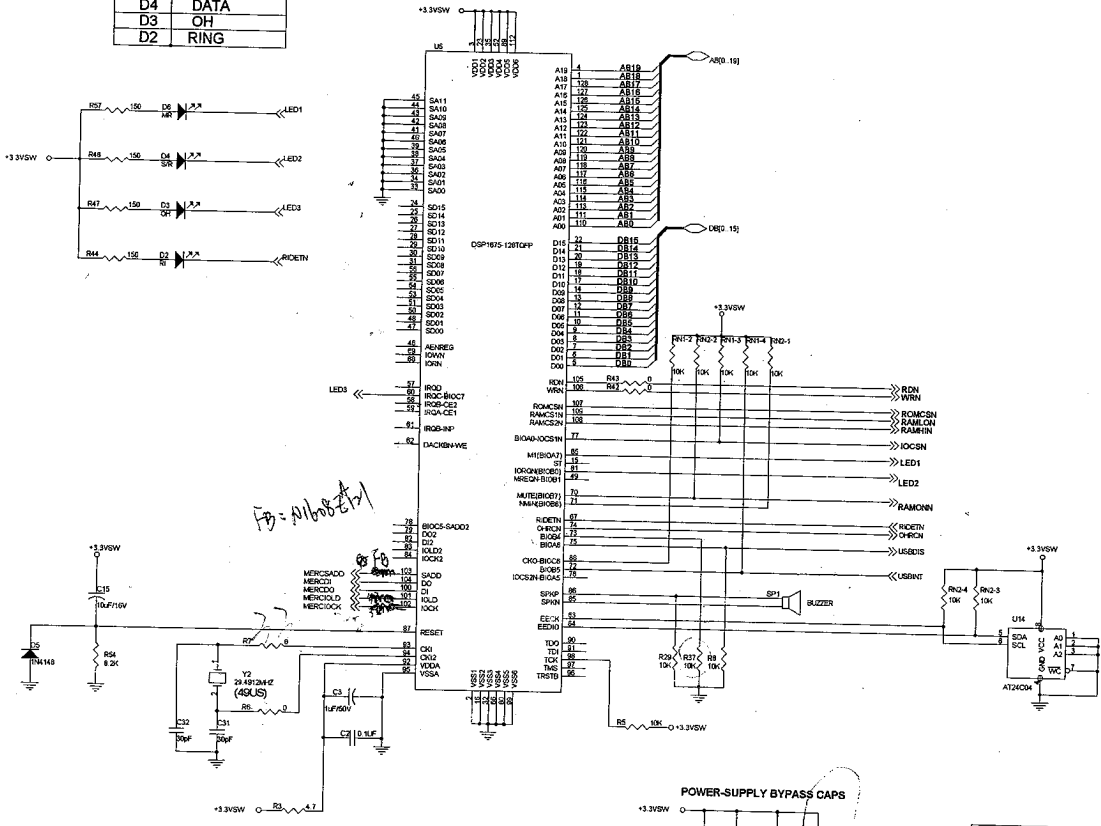


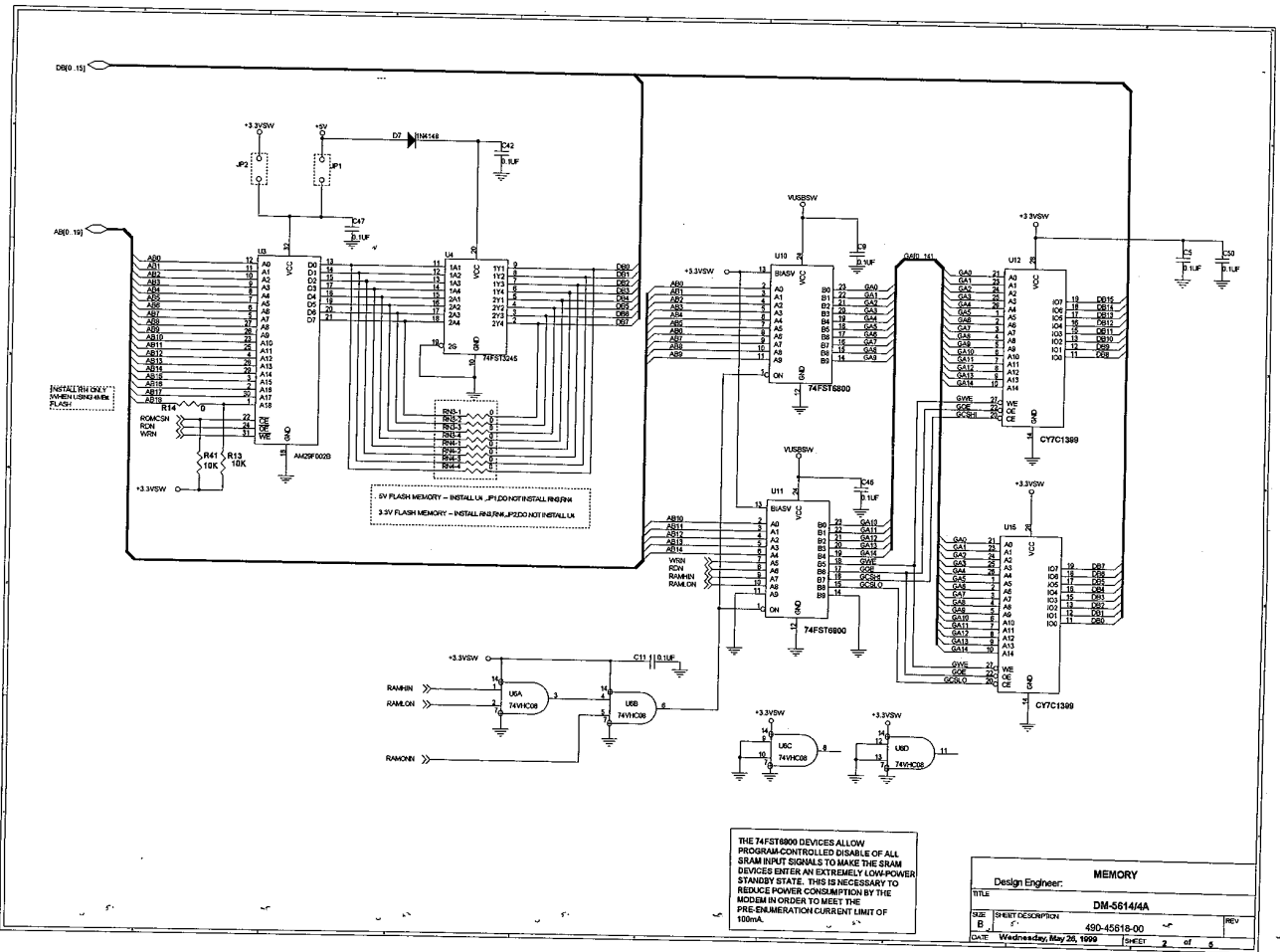
EXHIBIT D

Circuit Diagram

FRONT PANEL LEGEND	
D6	READY
D4	DATA
D3	OH
D2	RING

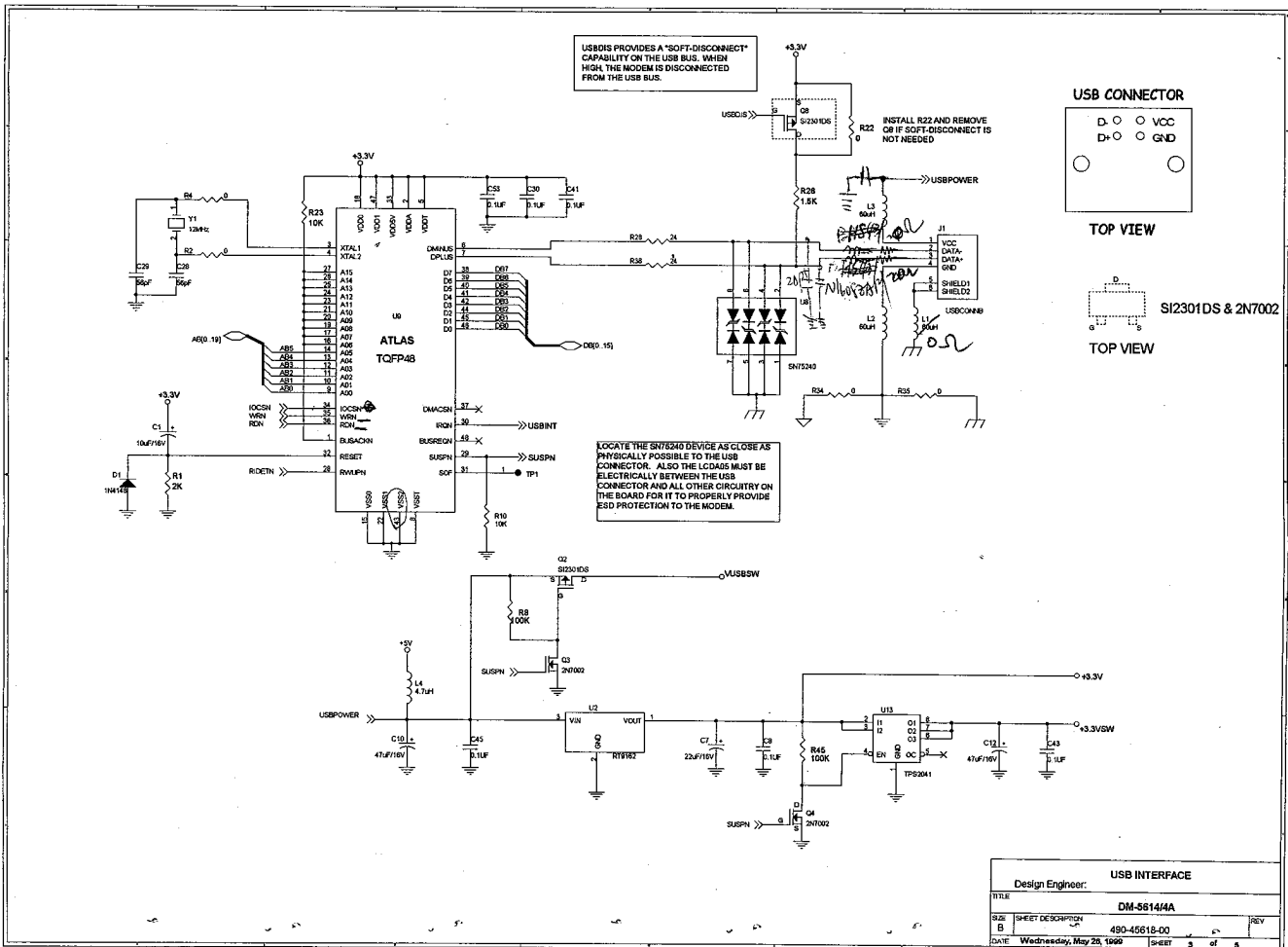


Design Engineer:	DSP
TITLE:	DM-56144A
SHEET DESCRIPTION:	490-45618-00
DATE:	Thursday, May 06, 1999
layer:	1 of 5

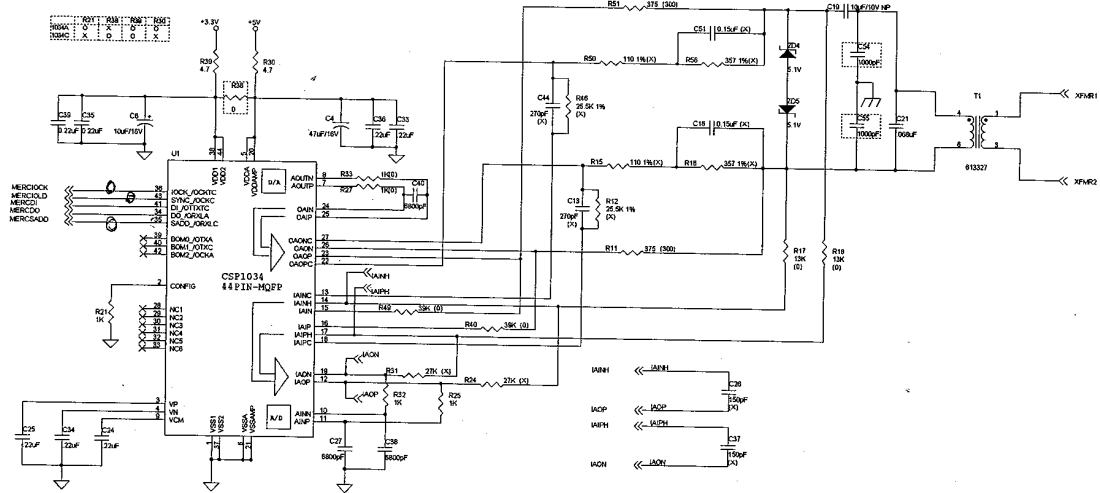


THE 74FST8000 DEVICES ALLOW PROGRAM-CONTROLLED DISABLE OF ALL SRAM INPUT SIGNALS TO MAKE THE SRAM DEVICES ENTER AN EXTREMELY LOW-POWER STANDBY STATE. THIS IS NECESSARY TO REDUCE POWER CONSUMPTION BY THE MODULE IN ORDER TO MEET THE PRE-ENUMERATION CURRENT LIMIT OF 100mA.

Design Engineer:		MEMORY	
TITLE		DM-5814/AA	
REV	DESCRIPTION	490-45618-00	REV
B			
DATE	Wednesday, May 26, 1999	Sheet	2 of 5



LINE CODEC/ HYBRID



CODEC & HYBRID	
FIG	DM-5614/A
Doc	Document Number 490-45618-00
Rev	Wednesday, May 26, 1999

