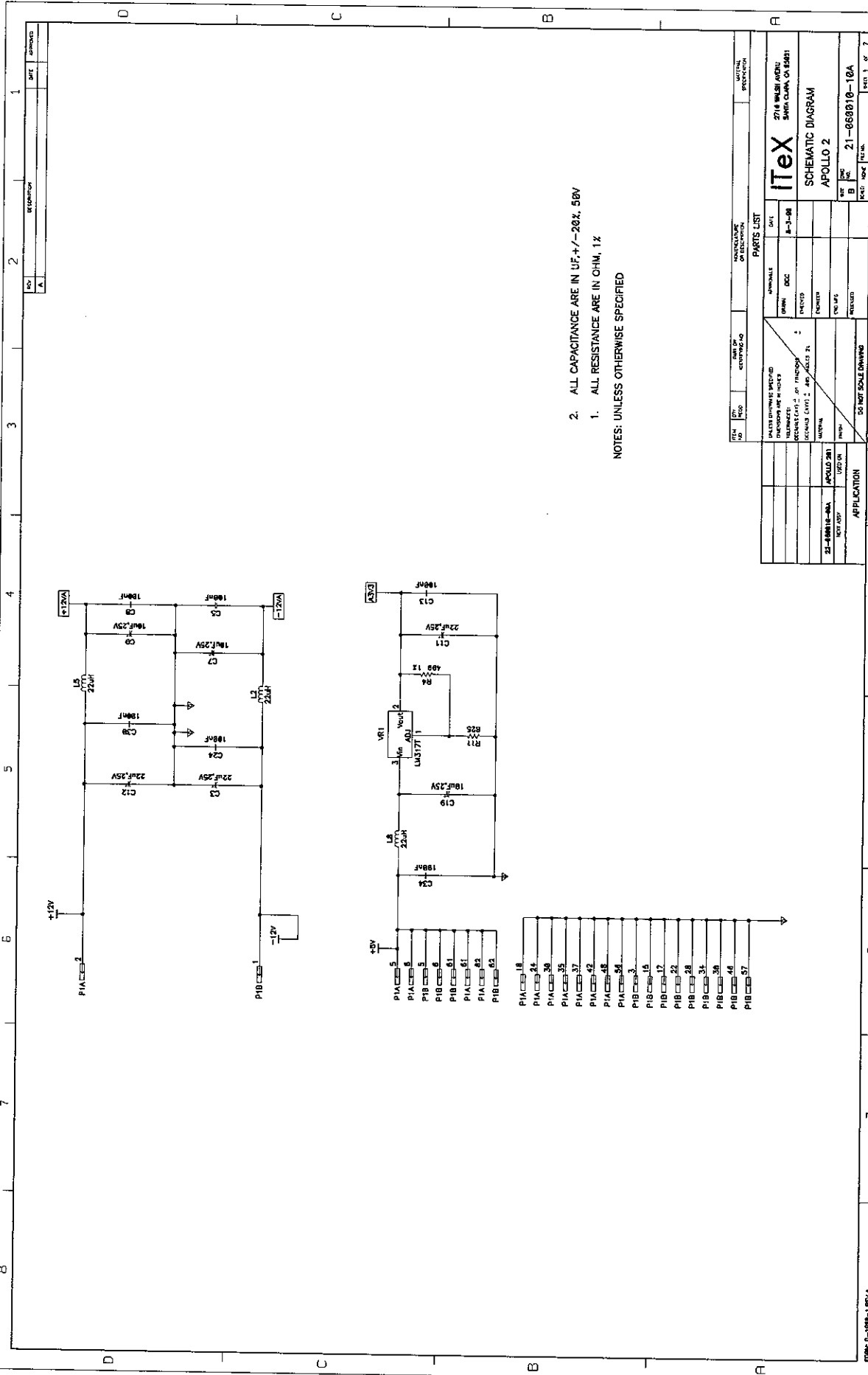


EXHIBIT D

Circuit Diagram



2. ALL CAPACITANCE ARE IN UF, +/- 20%, 50V
1. ALL RESISTANCE ARE IN OHM, 1%.

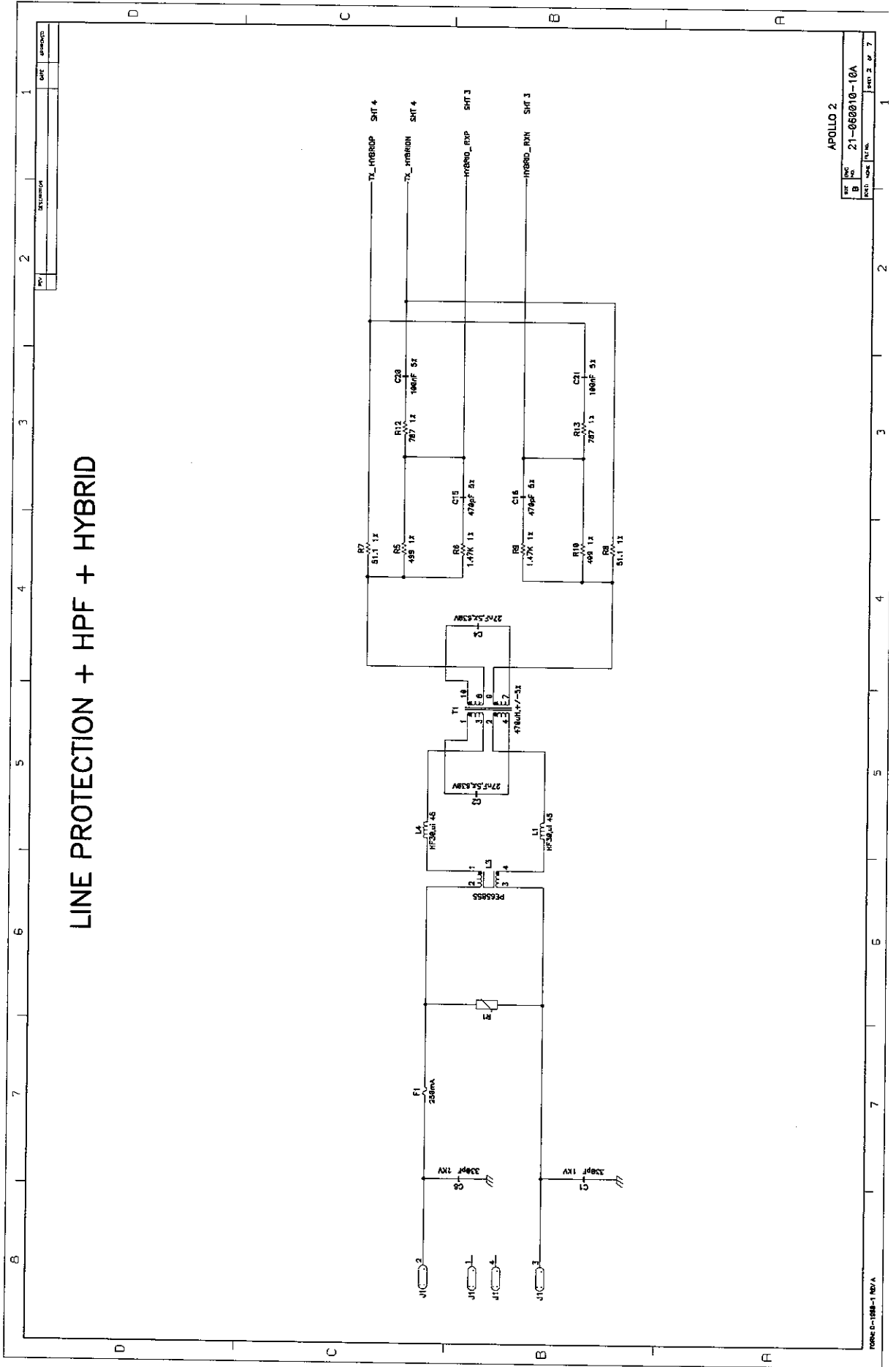
NOTES: UNLESS OTHERWISE SPECIFIED

REV	BY	CHKD	DATE	DESCRIPTION	APPROVAL
1				INITIAL PRODUCTION	

PARTS LIST	
Q1	7818 WLSI ADU
Q2	3903-08
R1	RESISTOR
R2	RESISTOR
R3	RESISTOR
R4	RESISTOR
R5	RESISTOR
R6	RESISTOR
R7	RESISTOR
R8	RESISTOR
C1	220P
C2	100NF
C3	100NF
C4	100NF
C5	100NF
C6	100NF
C7	100NF
C8	220P
C9	100NF
C10	100NF

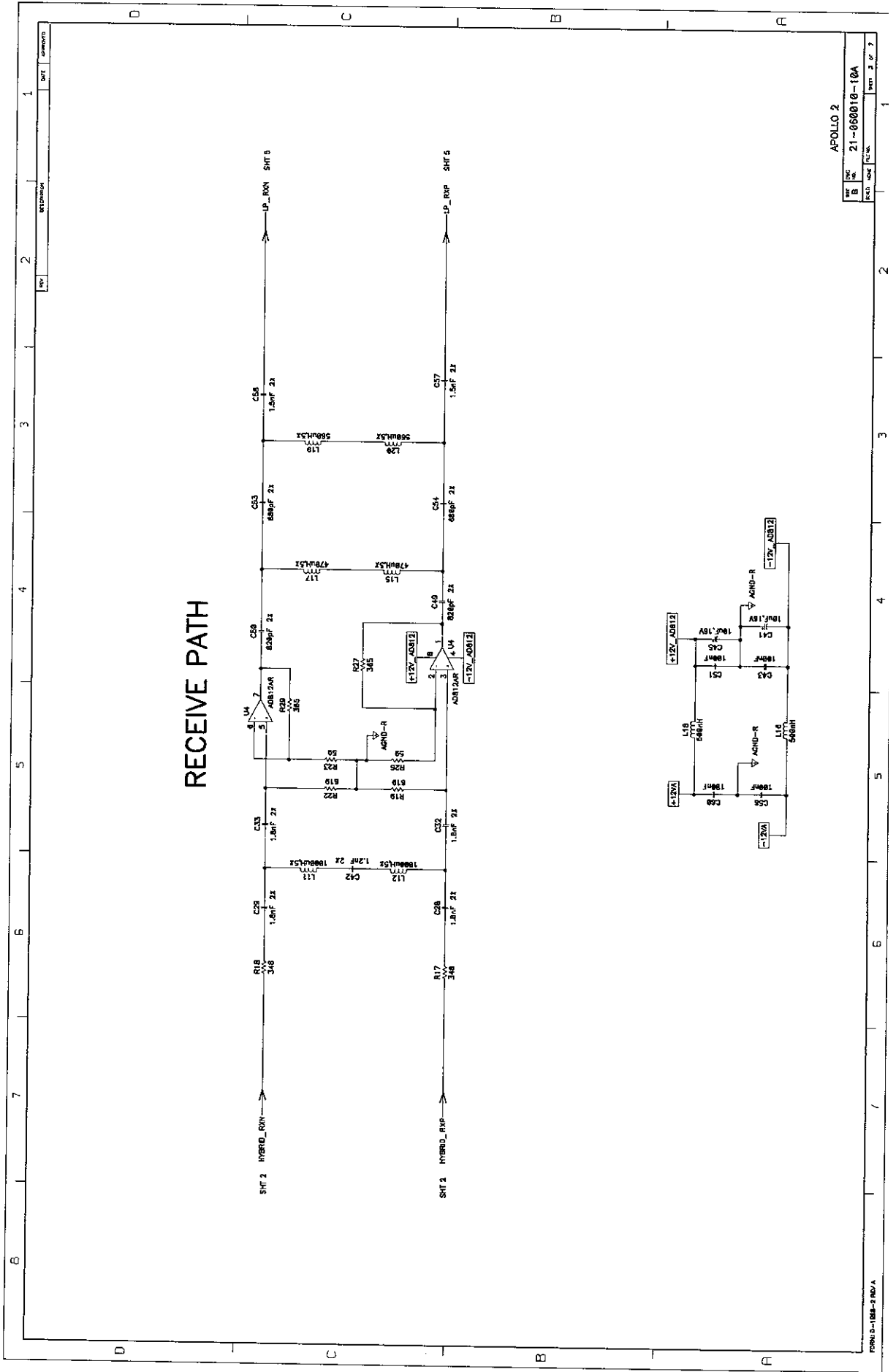
REV	BY	CHKD	DATE	DESCRIPTION
1				21-060010-10A

LINE PROTECTION + HPF + HYBRID

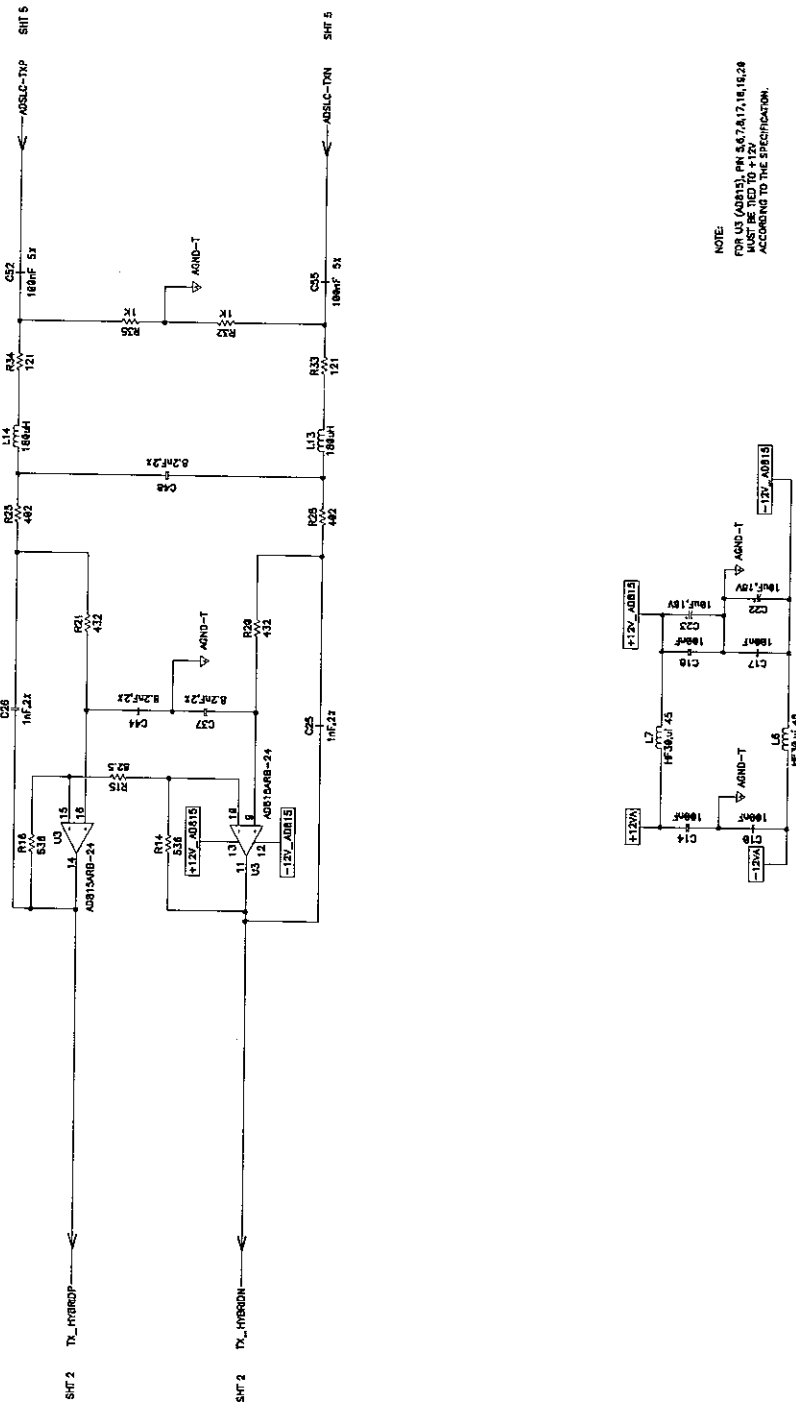


APOLLO 2

REV	DATE	BY	CHKD
B	21-050310-10A		
REV	DATE	BY	CHKD



TRANSMIT PATH



NOTE:
 FOR U3 (AD815), PINS 5, 7, 8, 17, 18, 16, 20
 MUST BE TIED TO +12V
 ACCORDING TO THE SPECIFICATION.

000024

ADSL DIGITAL

