Technical Description and Theory of Operation for Applied Concepts' Stalker Patrol Police Radar

This equipment consists of the following modules:

1. Counting Unit/Display
2. One or two Antennas
3. Infrared Remote Control
4. Power Cable
5. One or two Antenna Cables

Counting Unit/Display

The Counting Unit/Display contains two circuit boards. Please see schematics 002-5311-00 for the main board and 002-5316-00 for the display board.

Main Board

Twelve volt automotive electrical power is supplied to the unit through the cigarette plug Power Cable to pin 1 of J1 on the main circuit board, and pin 2 of J1 is the ground return. EMI filtering is provided by C33, C34 and FB1 and over current protection is provided by thermal fuse F1. Q11 provides reverse polarity protection while maintaining a low voltage drop in normal operation and Z1 is a transient suppressor that prevents high voltage "spikes" on the automotive power from reaching the electronics. This filtered and conditioned power is supplied to the rest of the unit as signal +12USW.

The main board provides three switch-mode power supplies developing 3.3 volts and 5 volts for operation of the main board and display, and a voltage that switches between 5 volts and 8 volts for operation of the antennas.

The 3.3 volt regulator is U6 on the main board. This is a buck-mode regulator operating at 570 KHz. The output of this regulator is supplied to linear regulator U7 on the main board that supplies 1 volt to operate the DSP U12 core. This 1 volt regulator provides regulated output whenever 3.3 volts is present.

The 5 volt regulator is U3 on the main board. This is a buck-mode regulator operating at 570 KHz.

The antenna regulator is U5 on the main board. This is a buck-mode regulator operating at 570 KHz, and switching between 5 volts and 8 volts is accomplished by transistor Q4 under control of the auxiliary processor U15.

All three voltage regulators share a common enable signal provided by power control circuitry Q5, Q6, Q8 and Q10 on the main circuit board. The front-panel POWER switch switches signal PWDN to ground when the switch is pressed. When this signal is switched to ground, transistors Q6 and Q8 are turned on. The drain of Q6 pulls the enable signal for the three regulators high and starts up the system. The drain of Q8 provides signal PDWN_RQST to the auxiliary processor U15 to signal that the POWER switch has been pressed. The auxiliary processor U15 provides signal PSET to control transistor Q10 which also pulls the enable signal for the three

regulators high so that once started up, the auxiliary processor can keep the regulators operating until a power off command is received from the POWER switch.

The auxiliary processor U15 provides overall power control for the system, handles USB communication and power control for the antenna(s) and provides analog to digital converters to allow monitoring of input power voltage through voltage divider R10 and R11 and clamp diodes D16 and D17, and internal temperature sensed by sensor U1. This processor and the Digital Signal Processor (DSP) are both clocked by a crystal oscillator X1 at 16 MHz. This signal is internally multiplied by 20 in the auxiliary processor to obtain a clock at 320 MHz, and then divided down to 80 MHz for the processor clock and 48 MHz for the USB clock.

On initial power up, the auxiliary processor sets the antenna power voltage to 5 volts in compliance with USB standards. This provides sufficient power for the USB interface in the antenna to operate. The processor then attempts to establish a USB link with the antenna, and once the presence of a Stalker Patrol antenna is confirmed the antenna power is switched to 8 volts to provide a higher voltage needed to operate the transmitter. This scheme prevents applying excessive voltage in the event a USB device other than a Stalker Patrol antenna is plugged into the USB connector(s).

At any point in time, only one antenna is powered on. Antenna power switching is handled by transistors Q2, Q3, Q7 and Q8 under control of the auxiliary processor by signals ANT_FRONT and ANT_REAR. The USB data path is also switched between antennas by U8 and U26 under control of the auxiliary processor by signal ANT_FRONT. D9 and D10 are transient suppressors to prevent electrostatic damage to the USB drivers and receivers.

In normal operation, the active antenna will sample data at a rate of 32 KHz. At 2 millisecond intervals, the antenna will transmit the last 64 samples collected along with system information in one packet containing 100 sixteen bit words (1600 total data bits) to the counting unit at the USB bit rate of 48 MHz. The auxiliary processor receives this data and passes it along to the DSP U12 over a Serial Peripheral Interface (SPI) using signals ANT_BCLK, ANT_SDATAI and ANT_FS. Clocking for this data is such that the 1600 bits of data plus analog-to-digital converter data is transmitted in a little less than 2 ms to provide dead time for synchronization. Control information is also sent from the DSP to the auxiliary processor during each 2 ms interval using signal ANT_SDATAO and the ANT_BCLK and ANT_FS signals shared with the receive channel. This data is then transmitted over the bidirectional USB interface to the antenna by the auxiliary processor. Connector J30 provides an interface to the auxiliary processor to permit programming the internal flash memory of the processor. This connector is not used in normal operation of the radar.

The DSP U12 is clocked by the same 16 MHz clock as the auxiliary processor. This clock is internally multiplied by 25 to obtain 400 MHz and then divided by two to obtain a main processor clock at 200 MHz. The DSP receives the antenna data transmitted over the SPI interface and performs the primary signal processing functions of the radar. The DSP also drives the LCD display, receives and interprets serial data from the infrared remote control, generates Doppler audio and beep tones for the speaker, handles external serial (RS-232) communications and monitors the RFI_SENSE signal for the possible presence of a strong radio frequency signal

that might cause disruption of operation. These functions are described in more detail as follows:

The DSP uses an external serial flash memory U2 to store the DSP firmware. At power-on startup, this data is downloaded from the flash memory into internal random access read/write memory and the serial flash is not used after that in normal operation. Four signals are used in this data transfer. SS is a select signal that selects the serial flash. SCK is a serial clock to allow the serial data bits to be clocked into the receiving interface. MOSI carries serial data from the DSP to the serial flash (generally used only during programming), and MISO carries serial data from the flash memory to the DSP.

The SPI interface is partially described above. This interface uses four signals. The ANT_SDATAI signal transmits serial data coming in over the USB interface from the antenna through the auxiliary processor to the DSP. The ANT_SDATAO signal transmits serial data from the DSP to the auxiliary processor which in turn passes that data to the antenna through the USB interface. The ANT_BCLK signal provides a bit clock for the serial data in both directions to permit clocking the data into the receiving interface. The ANT_FS signal defines the boundaries between successive words to allow the data to be reconstructed into data samples and control information.

The HCIN signal carries incoming serial data from the remote control to the DSP. This signal may be provided by an infrared receiver located on the display board via signal HANDC, or by a direct wired signal from pin 4 of J1 and/or pin 2 of J3. The infrared and direct wired signals are combined by transistor Q1 and diode D21 to produce the HCIN signal. This is a self-clocking signal that is interpreted by the DSP to provide system control functionality when buttons are pressed on the remote control.

The DSP handles serial (RS-232) asynchronous communications with external equipment (not provided by Applied Concepts) over signals RXD (receive data) and TXD (transmit data). These signals are buffered and converted to RS-232 voltage levels by U4 and are then routed to pins 7 and 8 of J1. This interface may be programmed to operate at rates from 1200 baud to 115,200 baud.

The DSP also generates serial output data for digital to analog conversion by U23 for the purpose of providing audio representing the Doppler-shifted signal received by the antenna(s) and beep signals providing feedback to an operator. Signal DAC_SDATAO carries the serial outgoing data, signal DAC_BCLK is a bit clock permitting U23 to clock in the data, and signal DAC_FS defines the boundary between successive data words. The bit rate for this data is 10 Khz. The analog output from U23 is on signal LINE_AUDIO. This signal is then fed to a class D speaker power amplifier U24 where the power level is boosted to the level required to drive the internal speaker via pins 1 and 2 of J14.

The DSP monitors the RFI_SENSE signal for possible presence of a strong interfering radio frequency (RF) signal inside the case that might cause malfunction of the electronics. This signal is developed on the main board by a short wire antenna ANT, a low-level schottky detector D18 and a high gain (500x) DC amplifier U14-A. When an interfering signal is present,

this signal is rectified to produce a positive-going signal at pin 3 of U14-A and this signal is amplified to produce the RFI_SENSE output signal. An option is provided to relocate this circuit to the display board permitting RF signals outside the case to be detected. In this case the RFI circuit on the main board is not populated and zero ohm jumpers select the signal source.

The DSP monitors signal VSS (vehicle speed sensor) for the presence of a variable frequency signal indicating the speed of the vehicle the radar is installed in. Use of this interface is optional – it provides a more reliable indication of vehicle speed than can be obtained from processing the radar signal, but detection of vehicle speed from the radar signal is satisfactory without the VSS interface. The circuit operates by providing a floating threshold developed by R66, R64 and C79 that follows the average value of the SPDOHI or SPDOLO signals from pins 5 and 6 of J1. (Normally only one of these is used.) When the input signal is above this threshold, the output of U10-A switches to ground and when the input signal is below this threshold, U10-A switches high. R75 and R85 provide a small amount of hysteresis to prevent noisy transitions. The logic output of U10-A is divided by two by flip-flop U9 to produce a square wave output on the VSS signal to the DSP whose frequency is ½ the frequency of the input signal. The frequency of this signal is measured by the DSP to determine vehicle speed.

The display circuit board generates Signal DIMLO that indicates the ambient light level as a variable frequency signal where the frequency is high when the sensor sees bright light and low when the light level is dim. This signal is monitored by the DSP to provide automatic brightness control for the LCD backlight.

The DSP controls the information shown on the LCD display using signals CE, MOSI and SCK. (Two of these are shared with the serial flash memory U2.) CE will be low when data is being sent to the LCD. MOSI carries the LCD data and SCK is the clock allowing the LCD controller to clock in the data. The DSP also generates DISP_BLANK to blank the display and LBRIT to control the LCD backlight brightness. LBRIT is developed by filtering a pulse-width modulated signal supplied by the DSP on signal BL_PWM. All of these signals are routed to the display circuit board through J2. J2 also routes the on-off switch signal PWDN, the ambient light sensor signal DIMLO and the HANDC signal from the infrared remote receiver.

Display Board

The display board contains a modular LCD display with built-in controller. The signals carrying LCD data from the DSP are routed through connector J3 and some of the signal names change as follows: MOSI -> LDAT1, SCK -> LCLK, CE-> CE, and DISP_BLANK -> INH The LBRIT signal from the DSP is amplified by U2-A and Q2 to provide variable drive current to the LCD at the collector of Q2.

U6 is an infrared receiver that detects infrared serial data from the infrared remote control. The receiver output is routed through J3 pin 8 to the DSP on the HANDC signal.

The display circuit board contains a light-to-frequency converter U7 to sense ambient light level. The frequency of this signal is too high to be used directly by the DSP and the frequency is divided by 256 in U1 to produce the DIMLO signal that is routed through J3 pin 9 to the DSP.

An alternate to the RFI detector circuit on the main board is provided by D18 and U2-B. This circuit uses a copper trace on the circuit board as the antenna but is otherwise similar to the RFI circuit on the main board that has already been described.

Antennas

The antennas contain a microwave assembly implanting the 24.125 GHz antenna, transmitter and receiver, a Gunn filter board that provides effective bypassing of the power to the Gunn oscillator, and a main circuit board providing power conditioning, antenna control, low noise preamplifier, digitizing of the received signal and USB communications to the counting unit.

Microwave Assembly

The microwave assembly contains a stabilized, high Q, Gunn diode waveguide cavity oscillator at 24.125 GHz, a conical horn used for both transmitting and receiving signals, a turnstile type duplexer and connecting waveguide sections. The Gunn oscillator is coupled directly to the waveguide, and the receiver uses a waveguide-mounted mixer diode to recover the Doppler shift of the received signal by mixing with a sample of the transmitted signal. When the received signal and the local oscillator injection signal are applied to the mixer, the difference frequency represents the Doppler shift on the received signal signal.

Final adjustment of the Gunn diode oscillator output frequency is made by adjusting the position of a ceramic rod in the oscillator cavity. The mechanism for changing the position of the rod also moves it as a result of temperature variations allowing the frequency to be compensated over temperature. The frequency is preset at the factory. The power output is determined by the output coupling aperture and cannot be changed in the field. Since the Gunn diode operates at its peak output power point, the output power cannot be made to exceed the factory preset value by any means accessible to the user.

Power output delivered to the turnstile at the base of the horn is nominally 10mW and will not be more than 15mW or less than 5mW over the full operating temperature range of the unit. Frequency stability over temperature is +/- 50MHz from -30 to +50 degrees Centigrade. DC power consumption of a typical oscillator is 5.0V at 250ma and is not adjustable beyond setting the peak power voltage.

The turnstile duplexer is a three-port machined waveguide device for separating the transmitted and received signals. It has two linearly polarized waveguide ports for the Gunn oscillator-generated transmit signal and the received signal. A third waveguide port is used to couple into the narrow opening of the conical horn antenna, which is used as both the transmitting and receiving antenna. The turnstile has the property of allowing linearly polarized electromagnetic energy to be converted into circularly polarized radiation and vice versa and provides separation between the transmitted energy launched from the horn and the reflected energy received back into the horn to prevent receiver overload from the relatively high level transmit signal. The horn and lens shape a 15 degree maximum conical beam pattern with -25dB side lobes while providing 23.4dBi of antenna gain.

The mixer is a waveguide-mounted diode with a frequency tuning adjustment and fixed impedance matching. Since the local oscillator injection is a sample of the transmitted signal, local oscillator leakage is not a problem. The demodulated Doppler signal is carried to the low noise pre-amp circuit located on the antenna main board PCB assembly through a spring contact.

Gunn Filter Board

The only functions of the Gunn filter board are to provide robust bypassing of the Gunn power to prevent spurious Gunn oscillations and mechanical interfacing to the Gunn bias choke.

Antenna Main Board

Please refer to schematic 002-5319-00 in the following discussion. Power is supplied to the antenna on the VBUS signal through the USB interface. This voltage may be either 5 volts (during system start-up) or 8 volts (during normal operation.) This voltage is regulated down to 5 volts by linear regulator U6 and then down to 2.5 volts by U9. The 5 volt power is used to operate the analog circuitry and the analog portion of the codec U7. The 2.5 volts is used as a reference voltage for the low noise preamp U1. The input voltage is also regulated down to 3.3 volts by linear regulator U28. The 3.3 volt power is used to operate the control processor U2, the logic portion of the codec U7 and the clock oscillator and PLL Y1, U5 and U8. A separate regulator U4 is used to supply power to the Gunn oscillator. The output voltage of this regulator may be programmed through digital potentiometer U11 under control of the processor to voltages between 4 and 6 volts permitting the Gunn oscillator to be operated at optimum voltage. All of the regulators on this board provide regulated output whenever input power is present except the Gunn regulator U4. This regulator may be turned off by the processor using signal GUNN-ON to turn the transmitter on and off.

The receive signal detected by the mixer is connected to the low noise preamplifier U1 through a spring contact. U1 implements a differential-input low noise amplifier operating at a voltage gain of 100. This configuration permits optimal amplification of the receive signal while rejecting spurious signals from nearby circuitry and shared ground paths. The output of U1 is fed to codec U7 which is a delta-sigma converter sampling at 32 KHz. The codec provides high quality anti-alias filtering and 24 bit output resolution permitting a dynamic range of over 100 dB.

The digitized data from the codec is routed to the processor on signal DOUT, BCK is the bit clock running at 2.048 MHz and FS is the frame sync identifying word boundaries at a frequency of 32 KHz. The codec can be reset by the processor using signal AD_RST.

Codec clocking is provided by signal MCLK from the phase lock loop-controlled crystal oscillator Y1 operating at a frequency of 12.288 MHz. This oscillator is phase locked to a 500 HZ signal supplied by the processor which is obtained by dividing the 1KHz USB "heartbeat" signal by two. This process insures a synchronous relationship between the codec sample rate and transmission of USB data packets. The phase locked loop is implemented by dividing the FS signal from the codec (nominally 32KHz, the same as the sample rate) by 64 in divider U5 to

obtain a nominally 500 Hz signal representing the oscillator frequency. This signal is compared with the 500Hz reference signal USYNC by phase detector U8 (operating as a quadrature exclusive-or detector). The phase error output from U8 is filtered by R24, C36, R25 and C4 to provide the frequency control signal to Y1. The error signal is of such polarity that it will slew the frequency of Y1 in the direction required to bring the two inputs to U8 to a condition where they are 90 degrees out of phase and at the same frequency.

The antenna processor U2 operates from a separate clock at 12.0 MHz. This signal is internally multiplied up to 48Mhz and this frequency is used both for clocking the processor and generation of USB serial data.

The processor generates an output signal at about 1 KHz on the TEST signal that can be turned on or off to verify integrity and sampling frequency accuracy of the signal path through preamplifier U1 and codec U7. The processor generates the GUNN_ON signal to turn the transmitter on and off on command from the counting unit, and sends and receives serial data signals over the USB interface to the counting unit.

The antenna main board includes a temperature sensor U10 that can be monitored through an analog to digital converter by the processor. This permits adjustment of the Gunn oscillator operating voltage with temperature to maintain optimum operation.

Connector J2 provides an interface for programming the internal flash memory in the processor. This connector is not used during normal operation.

Infrared Remote Control

Please refer to schematic 002-5232-00 in the following discussion. The infrared remote operates from an internal 3 volt battery. The remote uses a remote controller IC U1 to generate the data sent by infrared to the counting unit. This remote controller looks for key closures in the key matrix S1 – S12 and when a key closure is detected, the remote controller sends a modulated 40HKz carrier out on the MDATA signal. This signal is buffered by transistors Q1, Q2, Q3 and Q8 to drive the infrared LEDs D1, D2 and D3. The remote controller is clocked at 455 KHz by ceramic resonator Y1.

One key switch S13 is wired to a monostable multivibrator U2 to turn on the keyboard backlight for a few seconds when the key is pressed. Transistors Q4, Q5 and Q6 provide buffering to drive the array of backlight LEDs D4 - D15 and D18 - D28. The remote also provides for a hard wired connection to the counting unit through J3. In this case, the serial data is transmitted through Q7 to the counting unit without being modulated by the 40 KHz carrier. This interface also allows power to be supplied through J3 and if this power is present the 40 KHz signal to the driver transistors Q1, Q2, and Q3 is inhibited so the device does not transmit infrared signals.