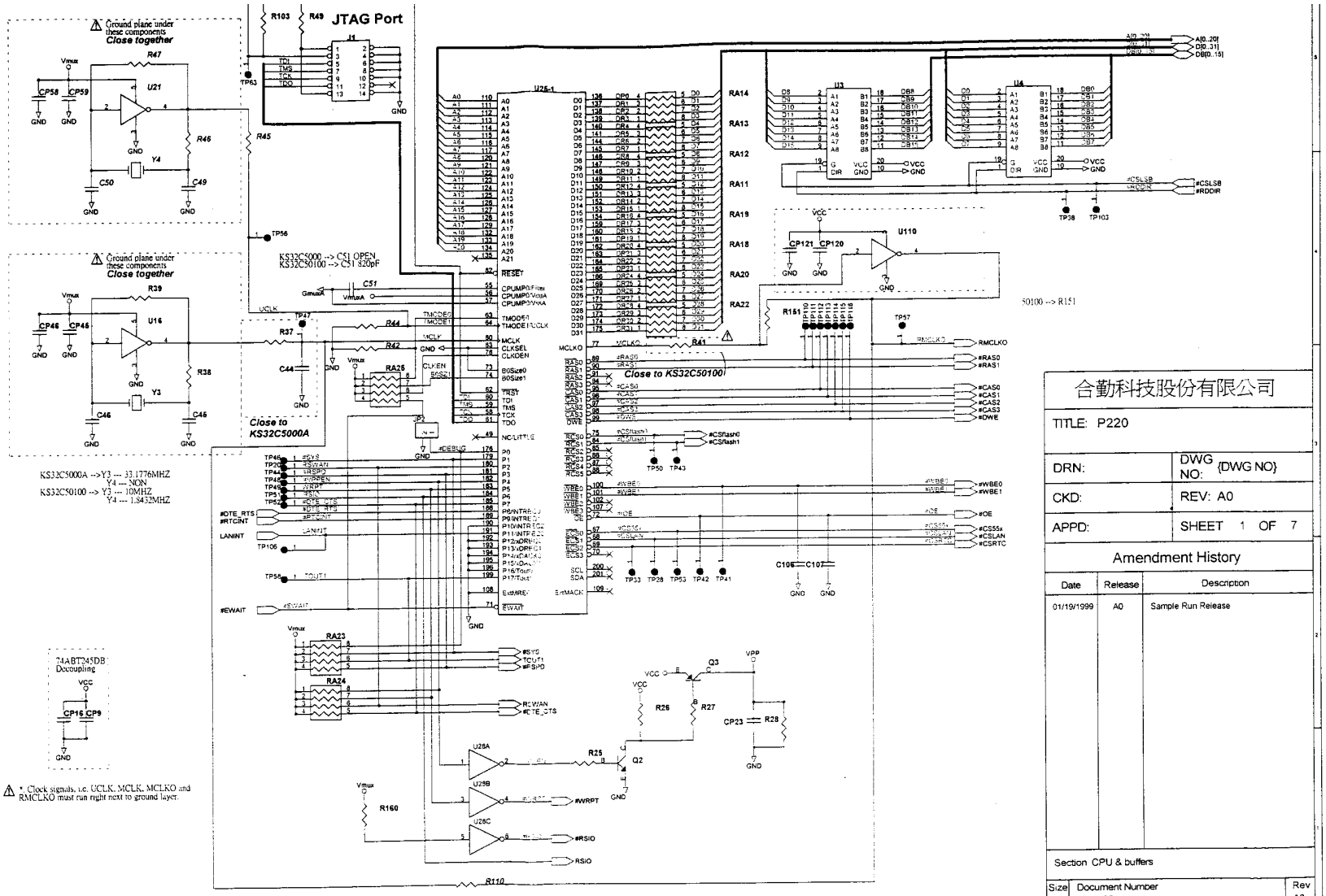

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Amendment History

Date	Release	Description
01/19/1999	A0	Sample Run Release

Section CPU & buffers

Size	Document Number	Rev
C	P100EF_x.dsn	A0
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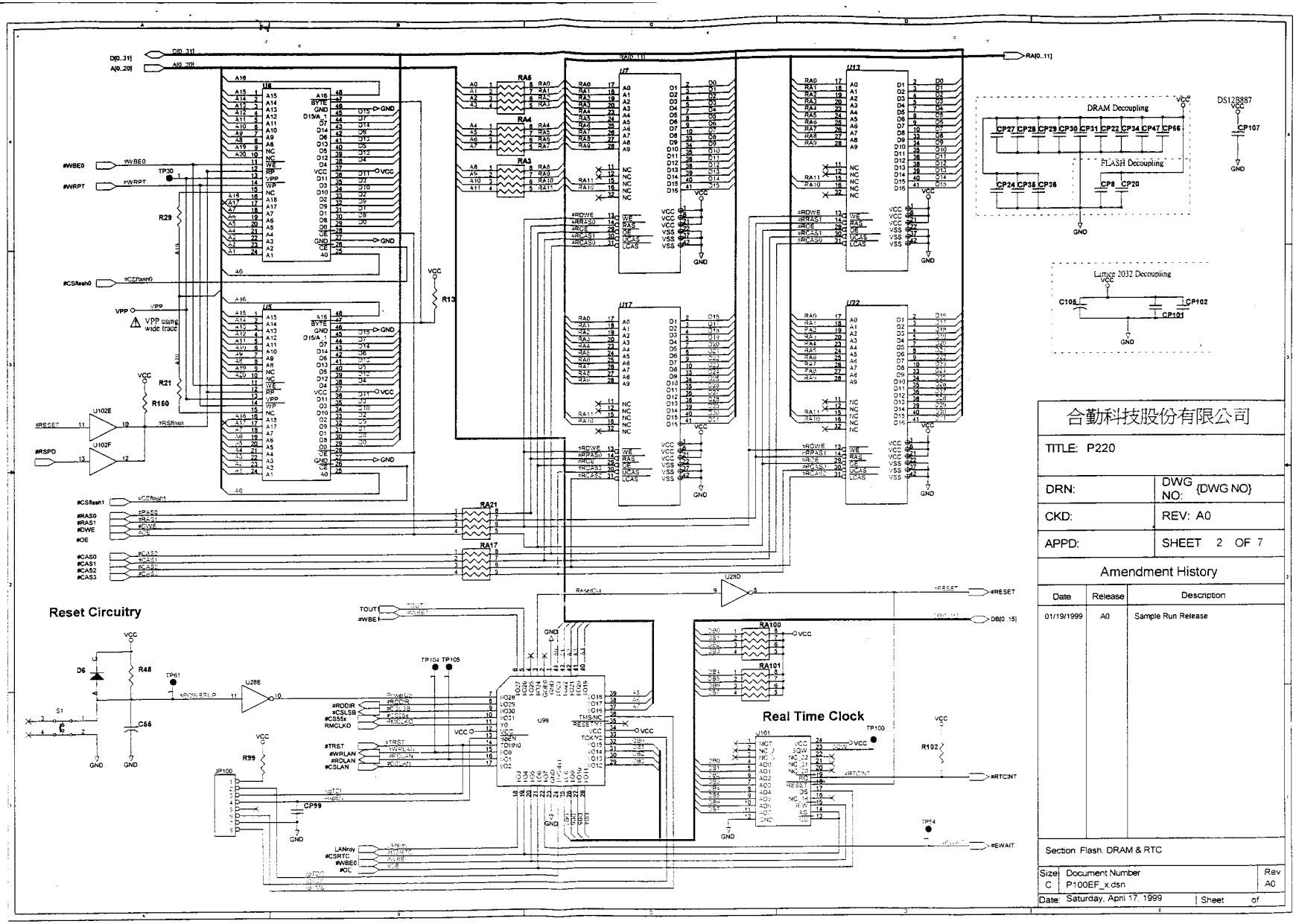

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CKD:	REV: A0
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Amendment History

Date	Release	Description
01/19/1999	A0	Sample Run Release

Section Flash, DRAM & RTC

Size	Document Number	Rev
C	P100EF_x.dsn	A0

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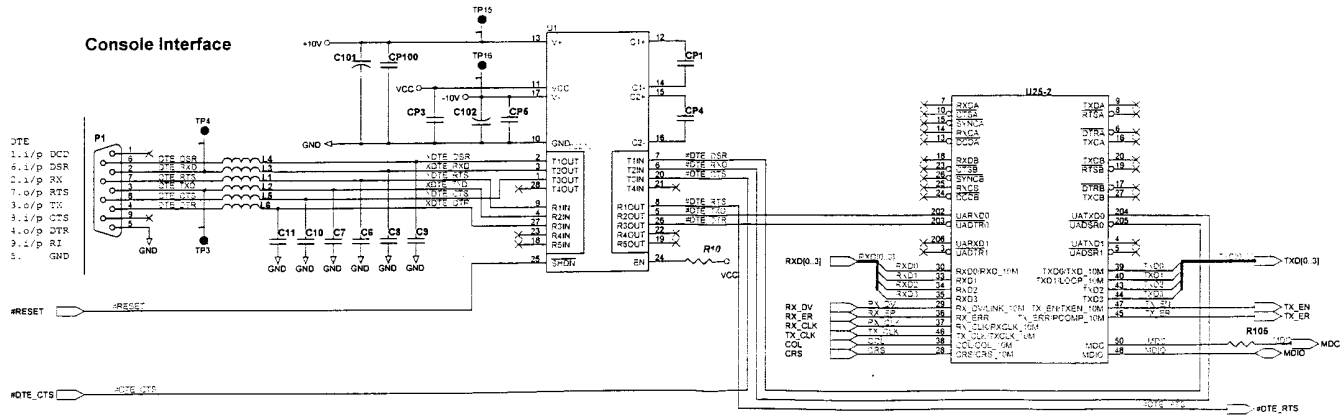

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Amendment History

Date	Release	Description
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Section UARTs & Printer port

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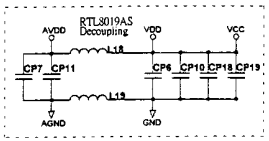

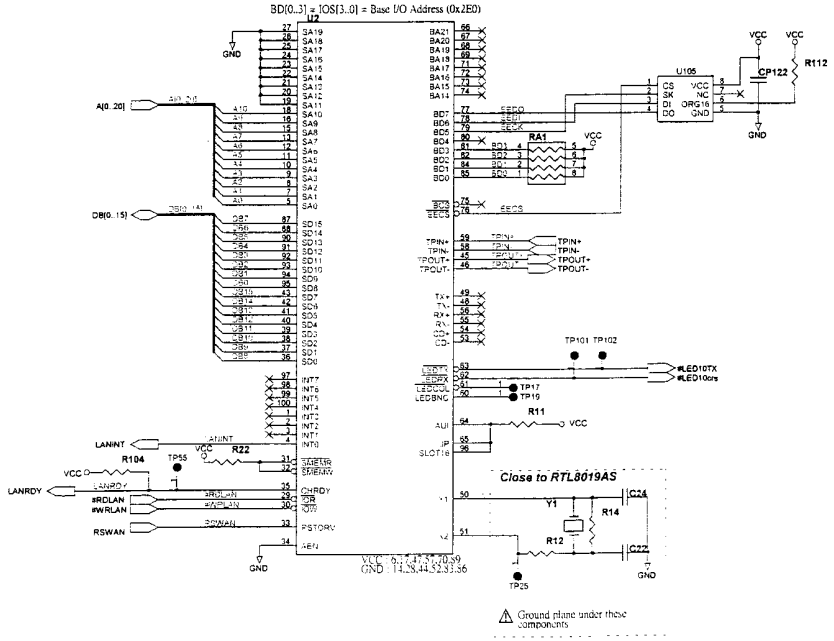

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Amendment History

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Section 4 port hub circuits

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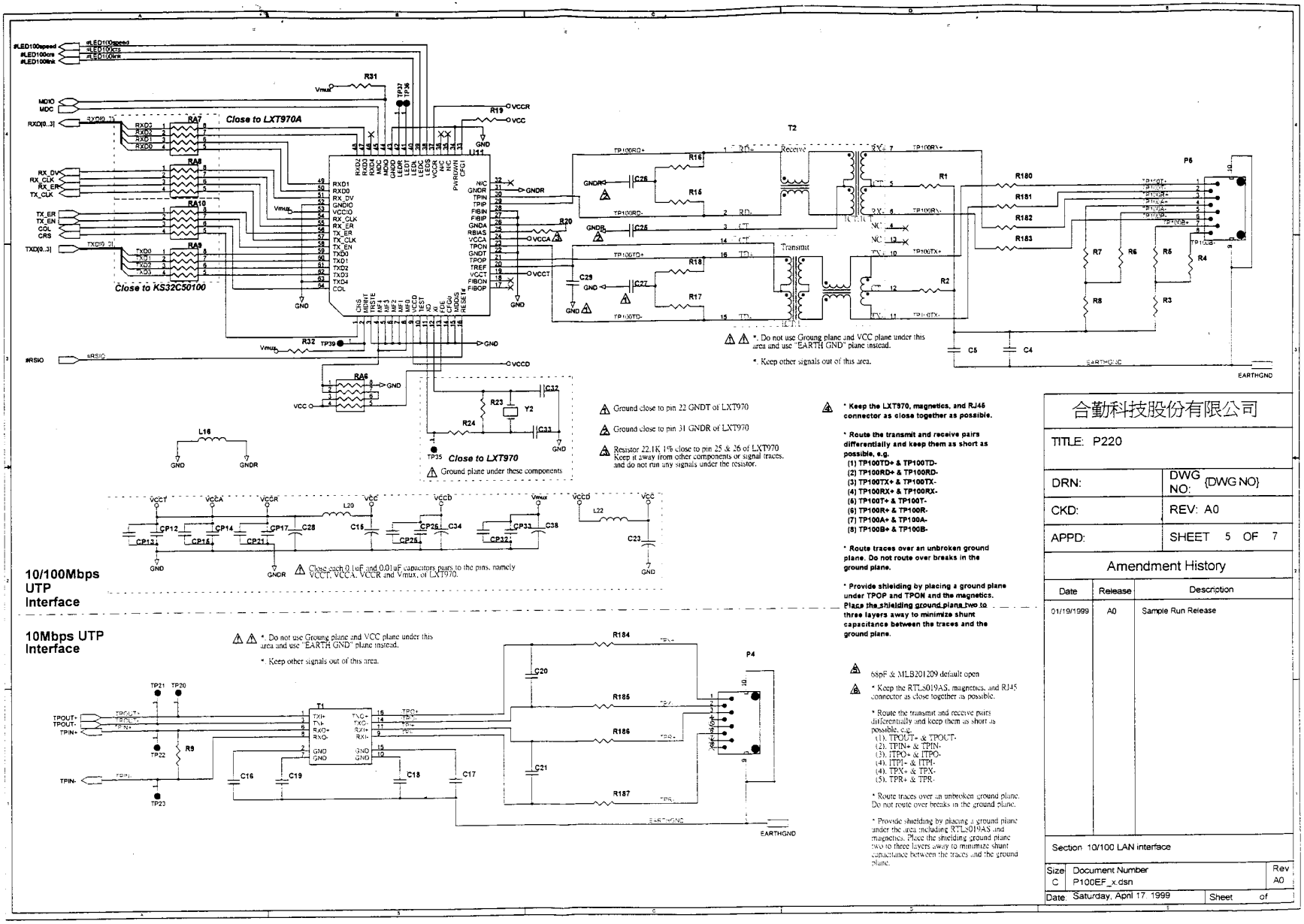

⚠ Ground close to pin 22 GNDT of LXT970

⚠ Ground close to pin 31 GNDR of LXT970

⚠ Resistor 22.1K 1% close to pin 25 & 26 of LXT970 Keep it away from other components or signal traces, and do not run any signals under the resistor.

⚠ Ground plane under these components

⚠ Close each 0.1uF and 0.01uF capacitors pairs to the pins, namely VCCT, VCCA, VCCR and Vmux, of LXT970.

⚠⚠ *. Do not use Groung plane and VCC plane under this area and use "EARTH GND" plane instead.

*. Keep other signals out of this area.

⚠ *** Keep the LXT970, magnetics, and RJ45 connector as close together as possible.**

*** Route the transmit and receive pairs differentially and keep them as short as possible, e.g.**
(1) TP100TD+ & TP100TD-
(2) TP100RD+ & TP100RD-
(3) TP100TX+ & TP100TX-
(4) TP100RX+ & TP100RX-
(5) TP100T+ & TP100T-
(6) TP100R+ & TP100R-
(7) TP100A+ & TP100A-
(8) TP100B+ & TP100B-

*** Route traces over an unbroken ground plane. Do not route over breaks in the ground plane.**

*** Provide shielding by placing a ground plane under TPOP and TPON and the magnetics. Place the shielding ground plane two to three layers away to minimize shunt capacitance between the traces and the ground plane.**

⚠ 68pF & MLB201209 default open

⚠ * Keep the RTL8019AS, magnetics, and RJ45 connector as close together as possible.

* Route the transmit and receive pairs differentially and keep them as short as possible, e.g.
(1). TPOUT+ & TPOUT-
(2). TPIN+ & TPIN-
(3). ITPO+ & ITPO-
(4). ITPI- & ITPI-
(4). TPX+ & TPX-
(5). TPR+ & TPR-

* Route traces over an unbroken ground plane. Do not route over breaks in the ground plane.

* Provide shielding by placing a ground plane under the area including RTL8019AS and magnetics. Place the shielding ground plane two to three layers away to minimize shunt capacitance between the traces and the ground plane.

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Amendment History

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Section: 10/100 LAN interface

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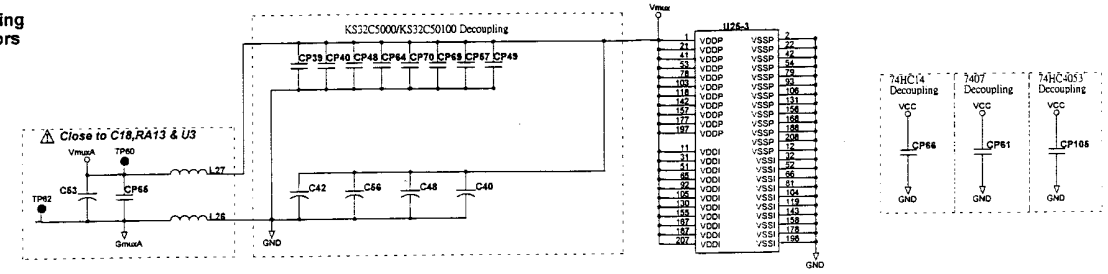
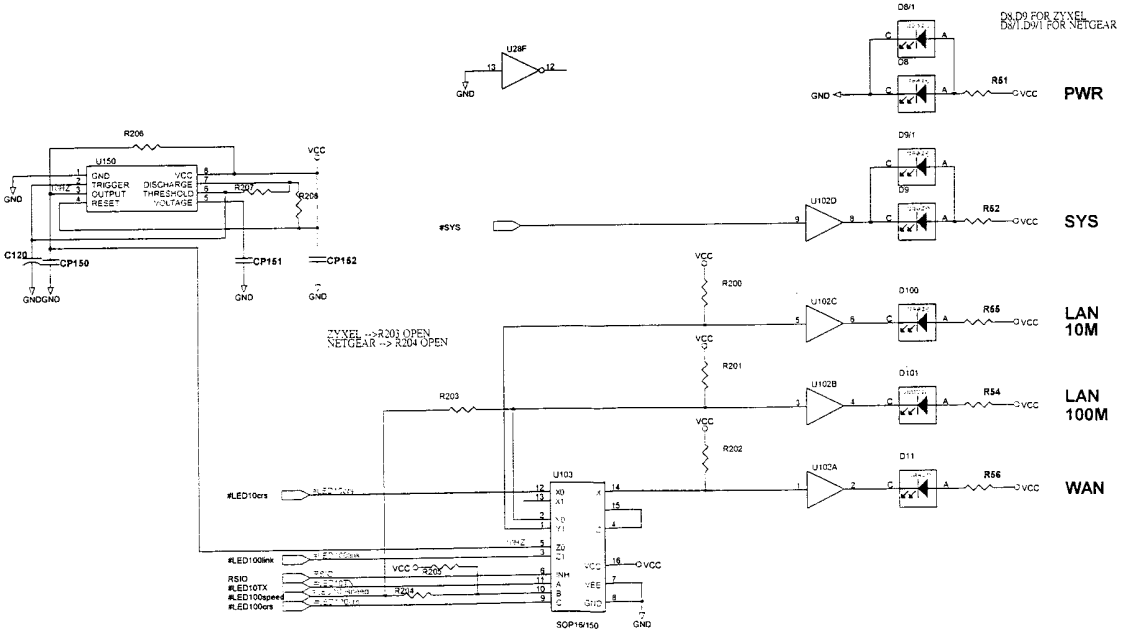
Decoupling Capacitors of CPU



LEDs



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Amendment History

Date	Release	Description
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Section RESET, CPU POWER & LED Circuits

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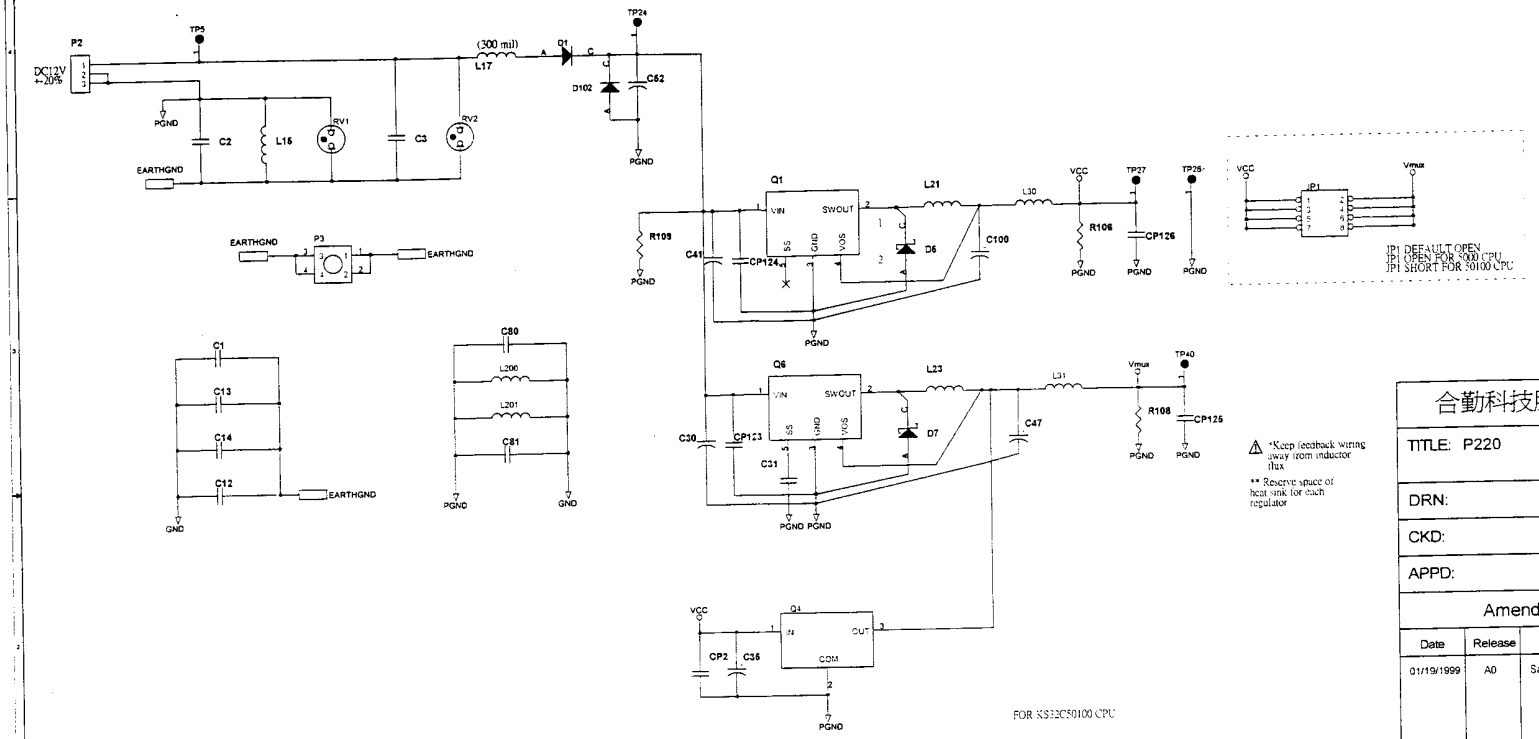

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Amendment History

Date	Release	Description
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Section:Power Circuits

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