EXHIBIT F

16000 TX CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION

Refer to Block Schematic Diagram (16000 Transmitter)

1. INPUT/OUTPUT CONNECTIONS

TB1-1 Circuit ground and negative side of 12 VDC power source
TB1-2 Positive side of 12 VDC power source
TB1-3 Normally closed contact of tamper switch (S-2) {see note}
TB1-4 Common contact of tamper switch (S-2)
TB1-5 Normally open contact of tamper switch (S-2) {see note}
TB1-6 Test Input (self test mode activated by positive input of 5 to 15 VDC)
TB1-7 Test Input (Self test mode activated by connection to ground)
TB1-8 Circuit ground
TB1-9 Circuit ground
J1 Output to D.R.O.
P1 Input to D.R.O.

Note: Normal condition exists when cover of electronic enclosure is secured or tamper switch is "defeated" (pulled all the way out).

2. TAMPER SWITCH

If the cover of the electronics enclosure of the transmitter is opened during normal operation, the Tamper Switch (S2) will cause the electrical connection between terminals #3 and #4 of TB1 to become an open circuit while a closed circuit connection will be formed between terminals #4 and #5 of TB1. The Tamper Switch circuit may be wired in series with the 12 VDC power source for the transmitter or to external alarm circuitry.

3. LINE CONDITIONER

The + 12 VDC from terminal #2 of TB1 is passed through L2 (ferrite bead) and F1 (.100 amp fuse) to a filter which consists of L1, C18, and C19. This filter along with L2 serves to remove high frequency AC components from the +12 VDC line and clamp to ground any high voltage spikes on the line to less than +18 VDC. D4 also serves to protect the system from polarity reversal of the input power. A normal input voltage to the transmitter of 10 to 14 VDC may be measured between TP9 and ground. The output of the line conditioner is connected to the anode of DS1 (light emitting diode). DS1 acts as a "power on" indicator as the total drain current

RJH

of the transmitter is passed through this device.

4. VOLTAGE REGULATOR

The cathode of DS1 is connected to the input of the Voltage Regulator. This regulator consists of U5 (voltage regulator) U6 (op amp) C13, C17, R12, and R13. U5 serves as the series pass element of the regulator while U6 serves as a low current buffer for the divided output of the regulator. When the voltage drop across R12 equals the 1.25 VDC internal voltage reference of U5, the output of the voltage regulator will be a regulated +5.0 VDC. The +5.0 VDC is the power source for all of the active circuitry within the transmitter and may be measured between TP5 and ground. Although not shown within the voltage regulator block, despiking capacitors C5, C14, C15, and C21 are connected to the +5.0 VDC bus throughout the transmitter to bypass switching transients.

5. CRYSTAL OSCILLATOR

The Crystal Oscillator is a "CMOS" version of a Pierce crystal oscillator and consists of U1a ("nor" gate) C1, C2, C3, C4, R1, R2 and Y1 (3.579545 MHz crystal). This circuit oscillates at the fundamental frequency of the crystal Y1 and is trimmed to the frequency of 3.579545 MHz by the adjustment of C2. The output of the oscillator is a 5 volt (p-p) square wave and serves as the input signal for the Frequency Divider. This signal may be measured between TP1 and ground.

6. FIRST FREQUENCY DIVIDER

The first frequency divider consists of J3 (frequency code block), U2 (counter), D1, D2, D3, and R3. The count length of the counter U2 is programmable by means of the frequency code block and feedback components D1, D2, D3, and R3. The 3.579545 MHz signal which appears at the input of the frequency divider causes the counter U2 to count-up until the count length which has been established by J3 is reached. At this point the counter U2 is reset to zero by the feedback components and repeats the count-up and reset sequence. This sequence causes the 3.579545 MHz signal to be divided by the amount programmed by J3. At the end of each count sequence, a 5 volt (peak) pulse appears at the output of the first frequency divider. The first frequency divider output serves as the clock for the second frequency divider.

7. SECOND FREQUENCY DIVIDER

The second frequency divider consists of U10. U10 functions to provide a constant divide by 8. This when coupled with the first programmable divider generates the modulation frequencies shown in the chart below and provides the input to the power amplifier.

Code	Mod Frequency	Clock Divided by
A	9520	376
B	10913	328
C	12093	296
D	13160	272
E	14436	248
F	15980	224

8. POWER AMPLIFIER

The Power Amplifier serves to boost the power of the modulation signal and consists of U1d ("nor" gate), Q2 (P channel, "VMOS" transistor), C16, R14, R15, and R16. U1d acts as an inverting buffer for the modulation signal which appears at the input of the Power Amplifier. The output signal of U1d is connected to the gate of Q2 via C16. This signal is a 5 volt (p-p) inverted version of the modulation and may be measured between TP7 and ground. The transistor Q2 is biased as a overdriven class "A" amplifier and produces at it's drain, a high current 5 volt (p-p) replica of the modulation which appears at the input of the Power Amplifier. The resistor R16 reduces the output signal of Q2 to approximately 3.5 volts (p-p) and serves as a means of limiting the transmitter output power. This signal may be measured between TP8 and ground. The signal at the output of the Power Amplifier provides the power for the Microwave Source via J1 and P1.

9. MICROWAVE SOURCE

The Microwave Source is a "GaAs" field-effect transistor oscillator whose frequency of operation is determined by the resonant characteristics of a ceramic dielectric material. This type of oscillator is referred to as a Dielectric Resonator Oscillator or DRO. The DRO is turned on and off at the modulation rate by the ouput of the Power Amplifier. The output power of the DRO is approximately +2 dBm (avg.) @ 10.525 GHz. This power is coupled to the antenna where it is focused and radiated in the form of a narrow modulated microwave beam.

10. MULTIVIBRATOR

The Multivibrator is a low frequency "CMOS" astable oscillator which consists of U1b,c ("nor" gates), R6, R7 and C9. Under conditions of system self test, this Multivibrator is activated by the gating circuit consisting of U3a (exclusive "or" gate), R4, R5, R17, R18, C6, and C7. The application of a positive voltage of 5 to 15 VDC to terminal #6 of TB1 or a ground to terminal #7 of TB1 will cause the output of U7a to go to a low state and allow the Multivibrator to oscillate. The output of the Multivibrator is a 5 volt (p-p) square wave @ .36 Hz. This square wave serves to drive the input of the Modulator and may be measured between TP3 and ground.

11. MODULATOR

The Modulator is an integrating, voltage to current converter which consists of Q1, R8, R9, and C10. This circuit is active only when the transmitter is in the self test mode and the Multivibrator is activated. The squarewave output of the multivibrator is converted to a Triangular waveform by the R/C network R8 and C10. This waveform is converted from a voltage waveform to a triangular current sinking waveform at the output of the Modulator by Q1, R9 and R10. The current flow in the output of the Modulator is applied to the junction of R12 and R13 of the Voltage Regulator where it produces a triangular voltage modulation of this junction. The voltage at the output of the Modulator is 3.75 VDC, plus or minus the modulation voltage, and may be measured between TP4 and ground. The result of the modulation at the junction of R12 and R13 is a triangular variation in the +5 VDC output voltage of the Voltage Regulator. This variation of +5 VDC bus causes a variation of the output power of the Microwave Source, thus simulating a disturbance of the microwave beam. The variation in the output power has a period of 2.8 seconds and the level of variation may be adjusted from +.25 dB to +3.0 dB by the adjustment of the Modulation Depth control R10.