Operational Description

The module EM730 used Qualcomm's RTR6285 chipset. RTR6285 is the first single-chip UMTS radio-frequency (RF) CMOS transceiver with receive diversity and GPS. In addition, the multi-band UMTS and quad-band EGPRS features allow for global roaming. The RTR6285 is fabricated using 0.18 micron RF CMOS process technology, which enables improved talk and standby time. Thereby effectively enhancing overall network performance. Further, by featuring receive diversity, the RTR6285 allows for better cellular coverage and in-building penetration.

The Circuit Vision analysis on the Qualcomm RTR6285 Transceiver includes all of the receiver (RX) and transmit (TX) paths of the device including all analog regions of the device and all analog to digital interfaces of the device. The main functional blocks that are shown are:

GSM Receive (RX) path which include:

- LNA's
- Receive demodulator
- Receive low pass filter

Rx/Tx phase locked loop including:

- Phase comparator
- Charge pump
- On chip loop filter
- Feedback divider
- Local oscillator generation

Transmit (TX) path which includes:

- Transmit low pass filter
- Transmit modulators
- Output amplifiers

UMTS receive path including:

- LNA
- Receive demodulator

UMTS phase locked loop including:

- Phase comparator
- Charge pump
- On chip loop filter (if present)
- VCO
- Feedback divider
- Local oscillator generation
- Bias circuitry sis includes all of the receive (RX)and transmit (TX) paths of the device including all analog regions of the device and all analog to digital interfaces and some digital circuitry of the device.

Transmitter:

A separate block is used to convert the digital bit streams from the baseband into parallel words to be used in the DACs and Sigma Delta modulator. This block also includes programmable delays for optimizing delays between the different modulation paths. The combined DAC and LP filter is used to convert the digital words of the digital block into analog signals. It also includes an auto-tuning block that compensates for VCO gain variations. The output is scaled according to the desired output power, and an offset can be added for PA linearization. The Tx-buffer is used to drive the PA with the correct power level.

Receiver:

The front end block is followed by a baseband block with active anti-aliasing filters that also suppress blocking signals and interferers. Automatic trimming of the filter RC constant ensures that the bandwidth variation is sufficiently low. The baseband block is followed by a fully integrated ADC of sigma delta structure with high dynamic range. The analog signals are converted to digital bit-streams in a sigma delta converter. The digital output signals are sent over a serial interface to the digital baseband controller for further processing and detection.