

Circuit Description For DSL5008EN(x) Product

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## 1. Introduction

The Aztech DSL5008EN(x) an ADSL2+ router, which has a four-port 10/100BASE-T Ethernet LAN interface, a single ADSL2+ port, 802.11n wireless interface, and one USB 2.0 host interface. It supports 2T2R with PHY rate at 300Mbps.

#### 1.1 ADSL2/2+ Router Processor with Analog Front End

Two-chip ADSL router solution including TC3162U ADSL2/2+ processor and TC3086 integrated analog front end and line driver is used in DSL5005EN(x) product.

The TC3162U ADSL2/2+ processor employs the discrete multi-tone modulation technology compliant to the various standards defined by ANSI and ITU-T. It incorporates a DMT engine, a 32-bit network processor, a USB 2.0 Host or device controller with integrated transceiver, a 10/100 Ethernet MAC with MII interface, an ATM AAL5 hardware SAR, and one PCIe interface for 802.11a/b/g/n WLAN solution. The 10/100 Ethernet MAC with MII interface supports multiple LAN port access. The configurable 480Mbps USB 2.0 host or device controller with transceiver provides storage/printer or a plug-and-play service for PC without external device.

TC3086 is a high-performance CMOS analog front end (AFE) with an integrated line driver for Asymmetrical Digital Subscriber Line Customer Premises Equipment (ADSL CPE) applications. It supports all ADSL standards (ADSL1/2/2+), including Annex A, B, I, J &M. It also supports RE-ADSL2 (Annex L).

#### **1.2 Four Ports Ethernet Switch**

A highly integrated Ethernet switch, TC2205F has a high performance, non-blocking and operates with store-and forward mode. It is a managed switch that meets all IEEE802.3/u/x Fast Ethernet specifications. It has 4-port 10/100 Mbps UTP and one MII/TMII port which supports PHY mode for management and router application.

### 1.3 802.11 b/g/n Wireless

RT5392 is a highly integrated MAC/BBP and 2.4GHz RF single chip with 300Mbps PHY rate supporting. It fully complies with IEEE 802.11n and IEEE 802.11 b/g feature rich wireless connectivity at high standards. Optimized RF architecture and base band algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators without overloading the host processor.

### 1.4 USB Host

The USB port is a dedicated HOST port compliant to USB 2.0 high-speed (480Mbps) which used for storage.

# 1.5 Power Supply

A 12VDC 1A external switching power supply is used to provide power to the platform. The 12V supply is stepped down to the following voltages using external switching regulators and LDO regulator.

o 7.13V

- o 5V
- 3.3V
- o 1.8V
- o 1.2V