Theory of Operation and Block Diagram

FCC/Canada Submittal

The Ambit 802.11a/b module is based on Atheros 802.11a/b radio solution of the AR5001 three-chip set which implements IEEE 802.11a and IEEE 802.11b. This chipset consists of the following:

_ AR5211: An IEEE 802.11a MAC/baseband processor, and CardBus/PCI bus interface.

_ AR5111: Radio-on-a-chip (RoC): An all-CMOS single-chip radio transceiver that converts signals from 5 GHz to the baseband range for use by the AR5211. The AR5111 offers fully integrated transmitter, receiver, and frequency synthesizer functions; eliminating the need for external voltage controlled oscillators (VCOs) and surface acoustic wave (SAW) filters.

_ AR2111 Radio-on-a-chip (RoC): An all CMOS radio transceiver that, when combined with the AR5111, implements a 2.4 GHz OFDM and 2.4 GHz radio solution. The AR2111 offers fully integrated transmitter, receiver, and frequency synthesizer functions. Like the AR5111, the AR2111 does not require external VCOs or SAW filters.

When the AR5111, AR2111 and the AR5211 are combined into a single design, the AR5001 three-chip solution enables a low-cost, compact IEEE 802.11a and IEEE 802.11b combo solution that easily fits on a PC Card or MiniPCI design.

Block Diagram

The AR5001 chipset provides a highly integrated IEEE 802.11a and IEEE 80211.b solution, as shown by the block diagram in Figure 1-1.

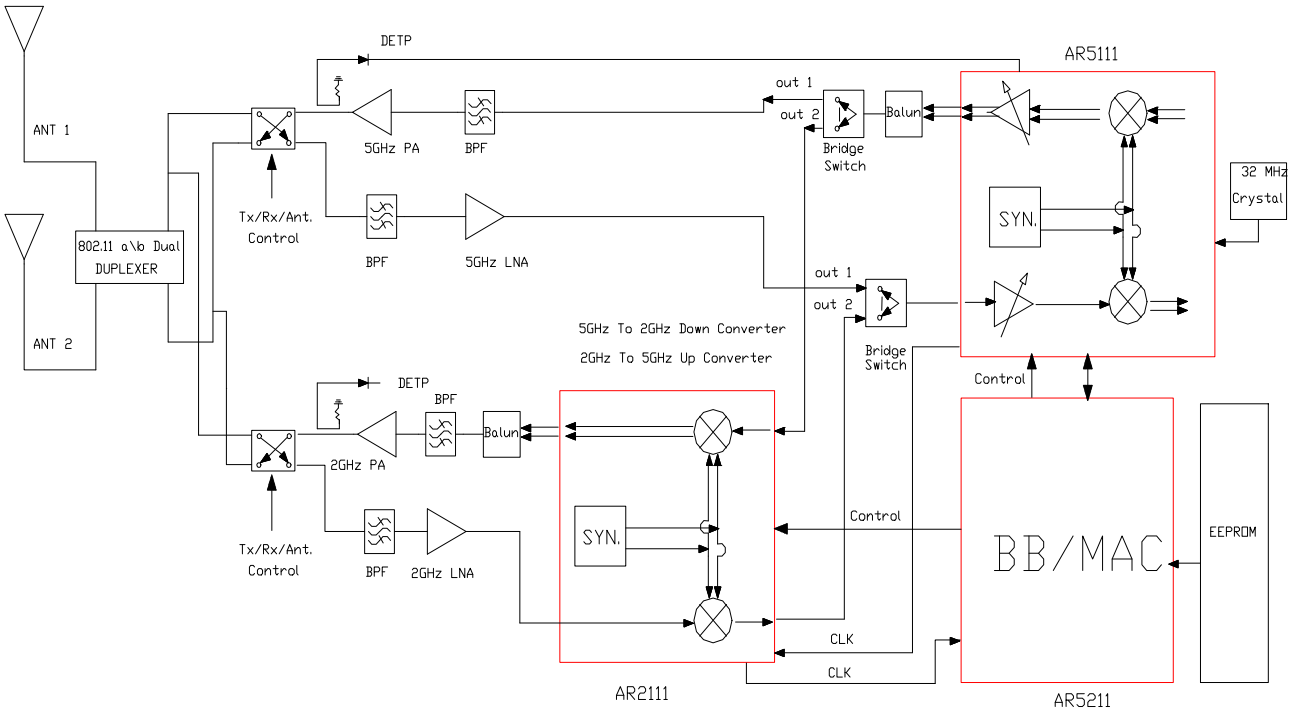

***Figure 1-1.Ambit* a/b Combo Module Block Diagram (Atheros Solution)**

The AR5211 is the origin and destination for all the front-end signals. Both transmit and receive signals are switched and transferred either to a 5GHz front-end or to a second chip (AR2111) which up converts or down converts the 5GHz signals to 2.4GHz. The AR2111, in turn, feeds a 2.4GHz front-end. Both the 2.4GHz and 5GHz front-ends are combined via two diplexers which are designed to feed two dual-band diversity antennae. The 5GHz signal is equivalent to the IEEE 802.11a signal, while the 2.4GHz signal is equivalent to the IEEE 802.11b signal.

MAC/Baseband Processor (AR5211)

The AR5211 chip is an IEEE 802.11a compatible, highly integrated ASIC containing a PCI interface, DMA engine, protocol control unit (PCU) (provides time critical media access control [MAC] functions in a state machine), and a baseband processor (PLCP/PHY).

DMA Engine (AR5211)

The DMA engine is 32 bits wide and feeds data from the PCU to the PCI/CardBus interface. The DMA engine coordinates transfers between it and the attached host through DMA descriptors.

Baseband Processor (PHY – AR5211)

The baseband processor either transfers data from the PCU and builds the frame that the radio frequency (RF) subsystem transmits, or receives the frames coming from the RF subsystem and decodes the frame for transmission to the PCU. The frame format is

constructed with short and long training symbols, intermixed with the data, rate, and length information.

The AR5211 supports the following modulations:
_ BPSK
_ QPSK
_ 16 QAM
_ 64 QAM
_ CCK
_ DSSS

Phase Locked Loop (PLL – AR5211)

The PLL takes the base 32 MHz clock frequency from AR2111 and derives one of the following core frequencies:
_ 40 MHz
_ 80 MHz
_ 160 MHz
The baseband processor and the ADC/DAC use these clocks.

DAC Filter (F)

External reconstruction filters are used between the AR5111 transmit I/Q inputs and the DAC outputs of the AR5211. The DAC uses a low-pass, 20 MHz reconstruction filter to remove spectral images and out-of-band quantization noise. The filters are differential for both the quadrature-phase and in-phase components and are implemented as second-order, current mode, Butterworth filter with a 3 dB corner frequency of 40 MHz. The load is
an internally biased on-chip current mirror. An internal RC filter provides additional attenuation beyond the self-resonance frequency of the external inductor.

Transmit Switch (Tx SPDT)

The purpose of the transmit switch is to route the AR5111 transmit signal to either the 5 GHz front end or the AR2111 for 2 GHz applications.

Receive Switch (Rx SPDT)

The purpose of the receive switch is to route to the AR5111 either the receive signal from the 5 GHz front end or the 2 GHz signal, up converted to 5 GHz, from the AR2111.

Low Noise Amplifiers (LNAs)

5 GHz LNA

The external 5 GHz LNA can be powered on and off through the RX5 signal on the AR5211. The external LNA provides an additional gain and reduces the overall noise figure (NF). The NF of the LNA should be better than 1dB, and its gain should be higher than 13dB.

2 GHz LNA

The external 2 GHz LNA can be powered on and off through the RX2 signal on the AR2111. The external LNA provides an additional gain and reduces the overall noise

figure (NF). The NF of the LNA should be better than 1dB, and its gain should be higher than 13dB.

Bridge Switches

The bridge switches are comprised of four switches arranged in a closed ring. The switch architecture is such that when the transmit is connected to output 1, the receive is connected to output 2, and vice versa.

Two control signals, from the AR5211, with opposite polarity, control the state of the switch. When both control signals are low, the switch isolates all ports.

Each control signal is connected to two opposite switches.

The switches are designed for a loss smaller than 1.5dB, 12dB minimum isolation, and IP3 (3rd order intercept point) better than 45dBm.

Dual Band Antennae

The 802.11a/802.11b antennae (Ant-A, Ant-B) are dual band antenna capable of providing a single antenna pair solution for 2 GHz and 5 GHz applications.

The antenna is a printed type over a finite ground plane.

32 MHz Crystal

The 32 MHz crystal provides the core clock for the AR5111, AR2111 and AR5211. This crystal is attached to the AR5111, which has an on-chip oscillator. The AR5111 provides the output of the oscillator to its internal frequency synthesizer, and also routes the output of the oscillator to an interface pin for use by the AR2111. The AR2111 uses this 32 MHz signal for its internal timing requirements and buffers the signal and directs it to an interface pin for use by the AR5211.

EEPROM

The EEPROM used is an Atmel (AT93C86-10TI-2.7, 2048x8 or 1024x16 - 16 Kb) device used to store the AR5001 configuration information, PC Card tuples, and any OEM-specific data.

The EEPROM contents include PCI configuration data with a read/write protection key, PC Card information structure (CIS) (or tuples), and vendorspecific data. Upon the de-assertion of reset, if the EPRM_EN_L signal of the AR5211 is active, the EEPROM contents are loaded.