Processing Gain Measurements for Conexant's DCT

1. Scope

This document details the results of measurement of the processing gain of a DCT FFF phone with reference to the Code of Federal Regulations, Title 47, Chapter 1, Part 15 Radio Frequency Devices (FCC).

FCC	Federal Communications Commission
SNR	Signal to Noise Ratio
JSR	Jammer to Signal Ratio
CW	Continuous wave (jammer)
HS	Handset
BS	Basestation
DBPSK	Differential Binary Phase Shift Keying

Table 1: Abbreviations

2. An Overview of the Processing Gain

Processing Gain Calculation

Theoretical processing gain limit for the 12bit Spreading BPSK system is 10.8dB.

Processing Gain = 10 Log (Spreaded data rate / Unspreaded data rate)
= 10 Log [(12 Chip/bit * 100Kbit/sec) / 100 Kbit/sec)]
= 10 Log [12]
= 10.8 dB

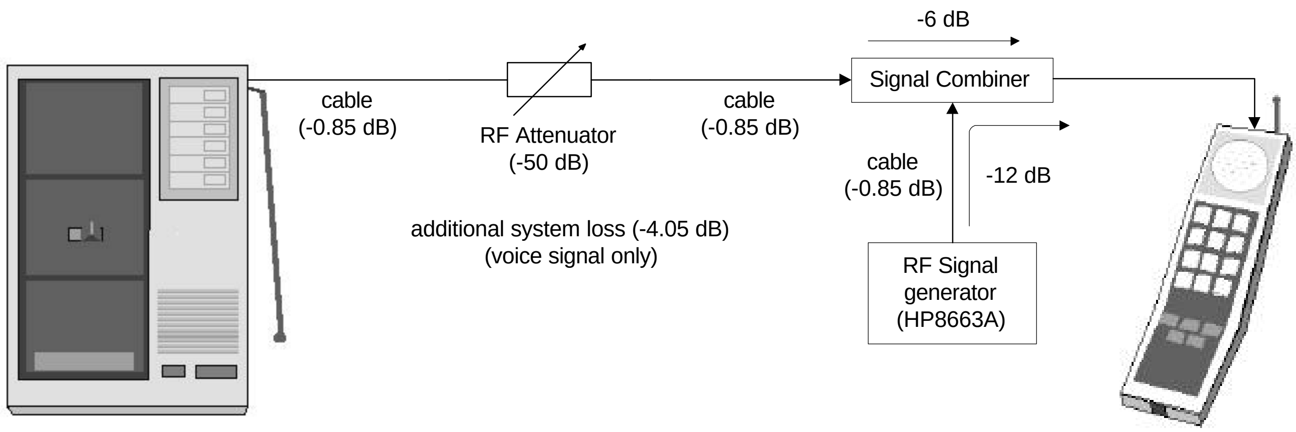
Processing Gain Measurement Method

Following method is specified by the FCC to measure processing gain. The detailed are in FCC documents 15.247 (e)(1). This involves transmitting a CW jammer in the RF passband of the system and measuring the jammer to signal ratio (JSR) required to achieve a certain bit error rate. The choice of the actual value of the bit error rate is left up to the tester. The jammer is stepped in 50 kHz increments across the entire passband and in each case the JSR to achieve the desired bit error rate is measured. The JSR is measured at the RF input to the system under test. The lowest 20% of the JSR data (in dB) are discarded. The processing gain can then be calculated as follows: -

$$G_p = \left(\frac{S}{N}\right)_{theory} + \left(\frac{J}{S}\right)_{measured} + L_{system}$$

where G_p is the processing gain, the SNR is that theoretically predicted for the system under the test to achieve the desired bit error rate, the JSR is the lowest value (in dB) in the remaining data set and L_{sys} adjusts for non-ideal system losses. L_{sys} can not be greater than 2 dB.

3. Processing Gain Measurement Test Setup



The following parameters were used in the test setup.

HS Tx power (dBm)	-1.9	
BS LNA gain (dB)	0	
Channel attenuation (dB)	-50	
Test system losses (signal) (dB)	-11.75	-4.05 dB (system), -6 dB (signal combiner), -1.7 dB (2 cables)
Test system losses (jammer) (dB)	-12.85	-12 dB (signal combiner), -0.85 dB (cable)

Table 2: Test Setup Parameters

4. Results & Calculation

The following measurement results were taken at the basestation. The desired bit error rate was set at 10^{-3}.

Jammer Frequency (MHz)	BER (BS)	Received jammer power (dBm)	Received signal power (dBm)	Jammer/Signal ratio (dB)
913.80	9.4×10^{-4}	-59.55	-63.65	4.1
913.85	9.6×10^{-4}	-57.95	-63.65	5.7
913.90	9.6×10^{-4}	-60.15	-63.65	3.5
913.95	9.6×10^{-4}	-64.25	-63.65	-0.6
914.00	1.1×10^{-3}	-61.55	-63.65	2.1
914.05	9.8×10^{-4}	-61.55	-63.65	2.1
914.10	1.1×10^{-3}	-61.95	-63.65	1.7
914.15	9.2×10^{-4}	-62.85	-63.65	0.8
914.20	1.0×10^{-3}	-59.85	-63.65	3.8
914.25	1.0×10^{-3}	-61.15	-63.65	2.5
914.30	1.1×10^{-3}	-62.05	-63.65	1.6
914.35	1.0×10^{-3}	-57.65	-63.65	6.0
914.40	1.1×10^{-3}	-55.65	-63.65	8.0
914.45	1.0×10^{-3}	-49.35	-63.65	14.3
914.50	1.1×10^{-3}	-59.25	-63.65	4.4
914.55	1.0×10^{-3}	-62.35	-63.65	1.3
914.60	9.7×10^{-4}	-59.05	-63.65	4.6
914.65	1.0×10^{-3}	-61.05	-63.65	2.6
914.70	1.1×10^{-3}	-62.55	-63.65	1.1
914.75	9.0×10^{-4}	-61.95	-63.65	1.7
914.80	1.0×10^{-3}	-61.05	-63.65	2.6
914.85	9.9×10^{-4}	-62.35	-63.65	1.3
914.90	1.1×10^{-3}	-64.05	-63.65	-0.4
914.95	9.2×10^{-4}	-56.25	-63.65	7.4
915.00	1.0×10^{-3}	-59.85	-63.65	3.8
915.05	1.1×10^{-3}	-57.25	-63.65	6.4
915.10	9.9×10^{-4}	-58.15	-63.65	5.5

Table 3: Test Results

For DBPSK at 10^{-3} bit error rate the required SNR is 8.0 dB. Using the results above and the data in the table below the processing gain is calculated to be 11.3 dB.

required SNR (dB)	8.0
system losses (dB)	2.0
J/S ratio at 80% point (dB)	1.30
FCC Processing gain (dB)	**11.3**

Table 4: Processing Gain Calculation data

Conclusions

The result measured for processing gain of 11.3 dB is close to the actual processing gain due to a 12 chip spreading code of $10 \times \log_{10}(12) = 10.8$ dB