Exhibit I: Operational Description

FCC ID: HN2WN-5MP01

TDK IEEE802.11a Mini-PCI radio

Functional description

See: Reference to Block diagram attached.

TDK's IEEE802.11a wireless LAN Mini-PCI radio is a 5.15-5.35Ghz ISM band radio design using OFDM (**O**rthogonal **F**requency **D**ivision **M**ultiplexing) modulation scheme based on Atheros's AR5000 chipset.

There are three main components in this radio design.

1) RF Front End section: This section includes the receive and transmit signal path for the 5Ghz RF signal, balun impedance transformers, LNA, PA, RX/TX switch, band-pass filter (BPF) and diversity antenna switch.
2) Analog section: This section includes an Atheros's AR5110 chip, which is an integrated, IEEE802.11a compliant, 5Ghz CMOS transceiver. This section includes a PLL loop filter to set the bandwidth of the on-chip PLL, a 32Mhz crystal, channel select filter, and base band filters for ADC and DAC blocks.
3) Digital section: This section contains an Atheros's AR5210 chip, which is an IEEE802.11a MAC, Base band processor, and CardBus/PCI Bus interface. This section also includes a serial EEPROM, GPIOs, LEDs, and control signals for the analog and RF section.

Transmit operation:

In the transmit path, wireless LAN transmitting data is passed between AR5200 and the host system using PCI/CardBus interface. The transfer of data take place through a direct memory access (DMA) mechanism to free the host CPU from performing actual transfer of data. Next, the MAC block within the AR5210, after performing the WEP and CRC operation, deposits the packets received from DMA engine into the 4kB FIFO. The base band processor transfers TX data from MAC, and builds the frame for the analog section AR5110 for transmission. This framed data is digital-to-analog converted by 9-bit current mode DAC and passed to the AR5110 through base band filters. The AR5110 amplifies this analog signal, up converts it to the 5Ghz range, and transmits the signal

through an on-chip power amplifier. The signal is impedance matched to 50 ohms with balun transformer, and converts the balanced differential signal to an unbalanced, single-ended signal for transmission. An off-chip power booster further amplifiers this 5Ghz RF signal. After going through an RX/TX switch for TX path, BPF and Diversity antenna switch, RF signal is sent to selected antenna port for transmission.

Receive operation:

In the receive path, 5Ghz RF signal is received through one of the diversity antenna port and after going the Diversity antenna switch and BPF. RF signal is routed to low noise amplifier for receiving through RX/TX switch. The LNA amplifies the 5Ghz RF signal and sends it to an on-chip 5Ghz LNA within the AR5110 through an impedance matched balun transformer that converts the unbalanced, singled-ended signal to the balanced, differential signal. The received signal is down converted to base band by RF and IF mixer stages within the AR5110 chip, and sent to an amplifier stage through an off-chip channel select filter. The channel select filter ensures that out-of-band signals are suppressed before the signal reaches the programmable gain amplifiers (PGAs). After amplification by PGAs, the received signal is sent to an analog-to-digital converter port of the AR5210 through an anti-aliasing filter. Digital data from the ADC is sent to the base band processor, and is converted to frames and decoded by performing various signal-processing operation. The decoded frames are then passed to the MAC, and subsequently to the host systems through the PCI/CardBus interface.

Intermec

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To Whom It May Concern:

Intermec Technologies, Corp. hereby declares that our Model WN-5MP01 5 GHz UNII transceiver complies with FCC Part 15.407(c) requirements as described below:
By design, the radio device will stop transmitting unless continuously presented data from the processor.
The discontinuing of transmission in the absence of information occurs by the design of the 802.11 MAC and 802.11a PHY.
The discontinuing of transmission in the presence of operational failure occurs when the processor detects an exception interrupt. The interrupt code will cause the AP to reboot to recover from the operational failure. If the interrupt code is also corrupted, a double exception occurs which halts the processor.
Our user documentation states this fact and warns the users. If you have any questions, regarding this or any other Intermec products, please feel free to contact me (phone: 425 356 1765, fax: 425 348 2633, email: carl.turk@intermec.com).
Sincerely,

Carl K. Turk, MSEE
Sr. EMC Engineer
Intermec Technologies Corp