Exhibit I: Operational Description

FCC ID: HN22011B

Compact Flash

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1. Introduction

1.1 Trilogy Product Background

Trilogy products transfer data at Ethernet speeds (11Mbps instantaneous data rate) over the air between two or more users or between a user and the wired network. The WLAN is not a single product, it is a digital radio system with product components that can be configured to meet a multitude of customer requirements. The Trilogy Access Point links to a wired LAN via a wired Ethernet connection. Wireless NICs communicate to the wired LAN through the AP. Multiple Access Points are deployed in a cellular layout plan similar in concept to the cellular telephone base station layout.

1.2 Purpose

This document defines the functional characteristics of the Trilogy 3 CF Adapter Mobile Unit (MU). Much of the basic functionality is provided by Intersil as part of their 802.11 DS implementation for the Intersil PRISM radio using the Intersil HFA3842/3873 microcontroller. In particular, the host interface access mechanisms, packet send, receive, queuing, timer services, and buffer management are already implemented and do not require further development. Therefore, this document primarily addresses the Symbol radio configuration and firmware enhancements required for the Trilogy product.

Detailed descriptions of the operation of the CF host interface (PCMCIA) may be found in the Programmer's Manual from Intersil and CF+ and CompactFlash Specification Revision 1.4 .

1.3 Goals

The adapter will support all required modes of operation as an 802.11 Direct Sequence MU or as an AP transmit/receive sub-system

The adapter will support station operation in CAM and PSP modes, as well as certain features required for site survey

The adapter will support *adaptive* frequency changes for compatible DS Access Points, in countries that support more than one channel

In production, the adapter will utilize the HFA3873 combination MAC and Baseband in place of the individual HFA3842 and 3863 devices outlined in this specification. The primary purpose for the conversion is to reduce product cost and achieve a single sided PCB design.

1.4 Key Features

- Direct Sequence 802.11 physical layer
- High data rate capability – 11 MBPS, 5.5 MBPS, 2 and 1 MBPS
- 3.3 volt CF Type I thickness with and Type II thickness on the extended section for the internal antenna package.
- 16 bit host interface using PCMCIA/CF IO mode
- In-line WEP algorithm
- Enhanced power save algorithm
- Robust roaming and dynamic rate switching
- Pin 45(SPKR) can be wired to provide an active high Media Free (MF) signal level for S24/BloothTooth coexistence support

1.5 What Will Not be Supported

The adapter will not support an ultra-low power mode of operation (< 1 ma). For PSP mode, it will remove power to as many circuits as possible, but clock control limitations prevent the HFA3842 controller from using a 32 KHz or other low power oscillator for sleep mode.

The adapter will not support sleep mode, nor will the driver require wake-up/resume operations since the controller and clock will always be active (although the adapter will consume as little power as possible when there are no receive, transmit, internal (roam) or host activities in progress)

1.6 References

1.6.1 Internal References

- Trilogy MU Firmware-Driver Interface Specification, Bob Neilsen
- Trilogy Network Interface PC Card Product Requirements Document
- Trilogy Network Interface PCI Card Product Requirements Document
- Trilogy Access Point Product Requirements Document
- qual_environmental_PCI_plan, Qualification plan for the PCI Card
- qual_environmental_PCC_plan Qualification plan for the PC Card
- qual_environmental_ AP_plan Qualification plan for the Access Point

- SS-03800-74, Environmental Guideline and Qualification Test Standard

1.6.2 HFA3842 References

Note – The following documents are proprietary and confidential

- HFA3842 Programmer's Manual
- HFA3842 Hardware Reference Manual

1.6.3 Other Device Specifications

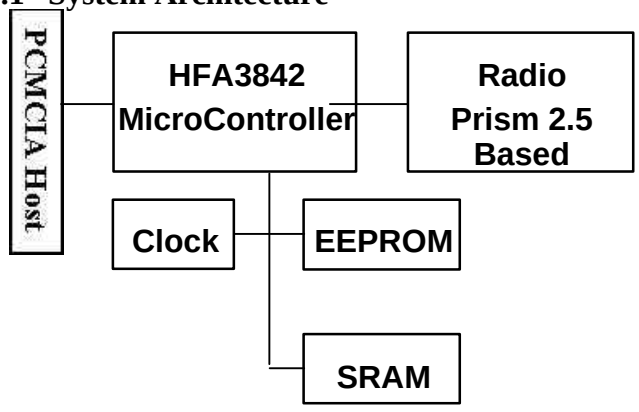
- HFA3863A Direct Sequence Spread Spectrum Baseband Processor, Intersil Semiconductor, 1999
- HFA 3783/3685A Direct Sequence RF Modem, Intersil
- EM128C16 - 128K by 16 bit Ultra Low power Asynchronous Static RAM bit, Enable Semiconductor, www.enablesemi.com, 10/98
- M24C08-W, ST Microelectronics , 8K by 1 bit 3-volt only, Serial I2C EEPROM.

1.6.4 External References

- Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, IEEE 802.11, D8.0 1 May 1998 (Or current approved specification)
- Draft 802.11 Specification for High Speed Wireless LANs (TBS)
- PC Card Standard (Version 2.01), Personal Computer Memory Card Internal Association, 1995 (or latest revision)
- CF+ and CompactFlash Specification Revision 1.4 .

2. Architecture

2.1 System Architecture



The adapter consists of a 2.4 GHz radio with direct sequence transmit and receive circuitry using Intersil 3863 Base Band Processor and HFA3685/HFA3783 Intersil chipset known as the PRISM 2.5 chipset. The controller circuitry consists of an Intersil HFA3842/3873 MAC controller with PCMCIA interface, EEPROM and SRAM. Crystal oscillators are used to drive the controller and transmit/receive circuits. Power control circuits are used to selectively enable radio circuitry. Power on reset is accomplished from the host PCMCIA interface and with resistors to put circuits into the off state until the firmware

has enabled the outputs from the controller.

2.2 Component Descriptions

The HFA3842 microcontroller executes under firmware control to process radio, timer and host events/operations. This chip executes RISC-type instructions in one clock using a 3-stage pipeline. The chip supports up to 8 active contexts. Context switching occurs when higher priority events cause an "instant" switch to the appropriate higher priority context. Contexts can be configured as "foreground" or "background", where foreground contexts always have priority, and background contexts operate in a round-robin fashion. When there are no eligible contexts, the device consumes very little power. Up to 64 K words of control store and 8 M bytes of RAM buffers are accessible by the CPU address registers.

A bootstrap EEPROM is activated at startup allowing the CIS to be activated and the FW to be downloaded from the host. All firmware executes from the control store address space in the SRAM in order to provide the required throughput for 11 MBPS data rates and WEP (Wired Equivalent Privacy encryption/decryption)

The 256 KB SRAM supports low memory variables and host interface, as well as a linked list of send/receive buffers and host configuration buffers. The upper half of SRAM is used to store the executable control store code.

The Host CF interface accesses memory/registers via the HFA3842 controller; Command/Status registers and Buffer Access Paths are provided to support a simple, fast interface mechanism

The radio card includes the Direct Sequence send/receive circuitry, RF synthesizers, reference oscillator, and power switching circuits

2.3 Hardware Environment

2.3.1 Introduction

The WCF2011BMWW & WCF2011BEWW CF Card can be used in handheld, notebook or fixed computers to provide wireless network access. The CF Card communicates over the air between two or more users or between a user and the wired network. The CF Card implements the IEEE 802.11b physical (RF) specification. It operates at 1, 2, 5.5 or 11 Mbps. The PC Card uses the Intersil Prism chip set for modulation, demodulation, spreading and despreading of the RF signals.

2.3.1.1 Card Dimensions

The WCF2011BMWW & WCF2011BEWW CF Card complies with the dimensions of a CF Type I card on thickness and width**.** The length is 2.183 +/- .008 inches, the width is 1.685 +/-.004 inches and the thickness is .130 inches maximum.

2.3.1.2 CF Card Antenna Connectors

One version of the CF Card comes with RF connectors. The coaxial connectors are MM9329 style connectors from Murata.

When the CF Card is used internal to the host (embedded in the host) antennas can be attached to the CF Card through the two MM9329 connectors. The antennas, which can be sold, have been tested and included with the regulatory test report.

2.3.1.3 CF Card Antennas

A version of the CF Card is produced with an integrated permanently attached antenna. The antenna portion of the card is at the end of the card so it extends out of the card slot.

Antenna Minimum Requirements

- Bandwidth: 2.4 to 2.5 GHz
- VSWR: < 2.0
- Impedance: 50 ohm
- Pattern/Gain: When the unit containing the antenna is held in its preferred position the vertically polarized gain over 135 degrees of azimuth and covering +/- 15 degrees elevation should be greater than -3 dBi for best results, -7 dBi minimum.
- Connector: The radio uses two MM9329 style connectors.
- Diversity: Optional. Two feeds with polarization or spatial diversity.

Regulatory Note: Many country regulations require special testing and reporting of antenna performance or of the system with the antenna attached. Please check the appropriate regulatory authority or Symbol for more information.

2.3.1.4 Operating Channels

The FCC (US), IC (Canada), and ETSI (Europe) specify operation from 2.4 GHz to 2.4835 GHz. The channels used are channel 1 - 2412 MHz, channel 2 - 2417 MHz, channel 3 - 2422 MHz, channel 4 - 2427 MHz, channel 5 - 2432 MHz, channel 6 - 2437 MHz, channel 7 - 2442 MHz, channel 8 - 2447 MHz, channel 9 - 2452 MHz, channel 10 - 2457 MHz, channel 11 - 2462 MHz, channel 12 - 2467 MHz, channel 13 – 2472 MHz.

Note: Channels used in US is 1-11, EU is 1-13 (exception France is 10-13).

2.3.1.5 Modulation and Channel Data Rates

Four modulation formats and data rates are specified by the IEEE 802.11b specification. A copy of the pertinent specifications is included in the appendix of this report. The basic access rate is based on 1 Mbit/s DBPSK modulation. The enhanced access rate is based on 2 Mbit/s DQPSK. The extended Direct Sequence specification defines two additional data rates. The high rate access rates shall be based on the Complementary Code Keying (CCK) modulation scheme for 5.5 Mbit/s and 11 Mbit/s.

3. Block Diagrams

The WCF2011BMWW & WCF2011BEWW CF Card uses the Intersil Corp. chip set to implement the spreading, modulation, demodulation and de-spreading. The RF up and down conversion approach is the common superhetrodyne architecture with the integrated chip set (HFA3685/HFA3783) manufactured by Intersil. The channel frequency, fc, is created (transmit) or converted (receive) by mixing with a low side LO frequency, flo, to the 374 MHz IF (fc= flo + 374 MHz). The 374 MHz IF is converted to/from based band using the Intersil I/Q modulator demodulator HFA3783 IC.
To see the Block Diagram please Click here.

3.1 Transmitter Path

The Intersil HFA3863 baseband processor creates the transmit waveform and outputs the signal on the TX I/Q lines. The Intersil HFA3783 up-converts the transmit baseband signal to 374 MHz. To control the side lobes the transmit signal is passed through a SAW filter (374 MHz center, 20 MHz BW). The signal is then amplified and mixed up to the channel frequency using Intersil HFA3685 IC. The LO frequency is lowside (fc – 374M). The signal is then filtered amplified and filtered (2.4 to 2.5 GHz passband) to create the required output power while keeping spurious and harmonic emissions in spec. Two switches are incorporated at the output to provide for antenna diversity and receive/transmit switching.

3.2 Receive Path

The receive signal passes through the front-end diversity and transmit/receive switches. The signal is amplified filtered by Intersil HFA3685 and then down-converted to 374 MHz. The LO frequency is lowside (fc – 374M). The receive signal is passed through the SAW to provide adjacent channel selectivity. The Intersil HFA3783 creates the baseband I/Q signals and the signal is de-spread and demodulated in the Intersil HFA3863.

3.3 Microprocessor Control

The Intersil HFA3842 micro-controller along with flash and SRAM memory run the control of the transmitter and receiver. The HFA3842 micro-controller is clocked at 14.67 MHz by a 44 MHz crystal. The HFA3842 along with the embedded firmware run the 802.11 Media Access Control (MAC) layer control. The MAC control sends and receives packets and transfers data to and from the CF interface to the host computer. The host computer that the CF Card is inserted into can be a handheld, notebook or fixed computer.

3.4 Frequency Generation

The first and second LO are generated by two external VCOs. The first LO feeds the Intersil 3685 generate the channel frequency minus 374 MHz. The second LO which feeds the Intersil HFA3783 is 2 times 374 MHz (748 MHz). A 44 MHz crystal is the reference for the synthesizer. The synthesizer is controlled by the HFA3842 micro-controller.

4. RF Signal Performance

The CF Card meet the IEEE Std 802.11b, 11 Mbps PHY specification.

4.1 Specifications

Unless otherwise stated the following specifications hold over –20C to +70C, and 3.3V +/- 5%.

Description	MAX	MIN	Unit	Comments
Functional				
Standby Current	20	5	mA	
Transmit Current	500	300	mA	
Receive Current	250	180	mA	
Frequency Tolerance 0C to 55C	+25	-25	PPM	
Frequency Tolerance -20C to 70C	+25	-25	PPM	
Receiver				
Sensitivity, 11 Mbps, 0C to 55C		-84	dBm	8% PER 1024 Octects
Sensitivity, 5.5 Mbps, 0C to 55C		-87	dBm	8% PER 1024 Octects
Sensitivity, 2 Mbps, 0C to 55C		-88	dBm	8% PER 1024 Octects
Sensitivity, 1 Mbps, 0C to 55C		-90	dBm	8% PER 1024 Octects
Sensitivity, 11 Mbps, -20C to 70C		-78	dBm	8% PER 1024 Octects
Sensitivity, 5.5 Mbps, -20C to 70C		-81	dBm	8% PER 1024 Octects
Sensitivity, 2 Mbps, -20C to 70C		-82	dBm	8% PER 1024 Octects
Sensitivity, 1 Mbps, -20C to 70C		-84	dBm	8% PER 1024 Octects
Sensitivity High Signal Level		-10	dBm	All data rates, 8% PER 1024 Octects
Adjacent Channel Selectivity		35 dB	dB	Between any two channels separated by ≥25MHz in any channel group. Measured per IEEE802.11b 18.4.8.3
Out of band Selectivity		50 dB		Measured per IEEE802.11b 18.4.8.3
RSSI Value at –60 dbm signal level.			int	Record value in ATE database and in NIC flash memory.
RSSI Dynamic range @ 2442, RSSI value differences.	25	5	int	Signal levels: -30 & -60 dbm
RSSI Dynamic range @ 2442, RSSI value differences.	40	8	int	Signal levels: -60 & -90 dbm
RSSI Dynamic range @ 2442, RSSI value differences.	80	25	int	Signal levels: -30 & -90 dbm
Transmitter				
Power Level, 0C to 55C	19	15	dBm	
Power Level, -20C to +70C	19	13	dBm	
Transmit Signal Quality Measurements should be made using 100 kHz resolution bandwidth and a 30 kHz video bandwidth. dBr means dB relative to the SINx/x peak		-30	dBr	f c – 22 MHz < f < f c –11 f c +11 MHz < f < f c + 22 MHz
		-50	dBr	f < f c –22 MHz, and f > f c + 22 MHz
Transmit Modulation				Meets IEEE802.11b 18.4.7.9
Carrier Suppression		15	dB	
RF output rise time	2	0.2	µS	10% to 90%
RF output fall time	2	0.2	µS	90% to 10%
Timing				
Channel Switching Time	224		µS	Measured per IEEE802.11b 18.4.6.12
Transmit to Receive Switch Time	10		µS	Measured per IEEE802.11b 18.4.6.9

Receive to Transmit Switch Time	5		uS	Measured per IEEE802.11b 18.4.6.10
CCA Detect Time	15		uS	Measured per IEEE802.11b 18.4.8.4

4.2 State Timing

Power on to 44 MHz stable. All VCC/temperatures 2412 MHz only.

Power on until Synthesizer programming allowed.

HF Synthesizer Settling Time. Measure the time between the final load pulse and the point where the discriminator waveform settles to within +/- 25 ppm of the final value.

LF Synthesizer Settling Time. Measure the time between the final load pulse and the point where the discriminator waveform settles to within +/- 25 ppm of the final value. >>

4.3 Carrier Sense/Clear Channel Assessment

<< Add CCA description>>

5. Product Power Requirements

Power for the CF card is supplied through the CF interface and will not require an external power adapter or battery pack. The average current draw to stay associated and be able to receive packets when using the power save protocol should be under 60 mA. The card should be capable of being turned off while residing in the PC Card slot.

5.1 Operating Current

The NIC is should be able to work with a 3.3 V +/- 5% power source. The NIC current consumption depends on the operating state. The operating state is controlled by the NIC driver software and the NIC CPU. In addition to the currents given Table 4.1, transient in-rush currents occur when switching on the receiver and transmitter. The pulse characteristics, and peak in rush current depend on the capacitance and resistance of the host power supply. The NIC presents a capacitive load of approximately 80 uF. Noise on the 3.3 V power supply should be below 30 mV RMS.

6. Regulatory

The CF Card will meet the following regulatory standards.

- FCC part 15.247, 15.205, 15.209 US
- Spread Spectrum FCC Part 15 Class B US Unintentional Emissions
- ETSI EN 300 328-1 European Spread Spectrum
- DOC RSS-210 Canadian Spread Spectrum
- RCD STD-33R Japan Spread Spectrum
- EN 301 489-1 v1.2.1 (7-2000) Part 1: EMC , Common technical requirement
- EN 301 489-17 v1.1.1 (9-2000) Part 17 : Specific conditions for 2.4Ghz wide-band data
- EN55022 Class B: Emissions
- IEC 601-1-2: EMC - Medical Electrical equipment, will be attempted but is not mandatory)

- EN 61000-6-2 (EMC - Industrial environment (includes 10V/m radiated immunity), will be attempted but is not mandatory)