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Request for Type Acceptance
of the
JTech On-Premise Paging System

SMARTALERT 200
Model Series-SMARTALERT 200
FCC ID: HLG-SMARTALERT 200

Test Performed by:

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System Specifications

JTech Communication's Inc. Premise Paging System "SmartAlert 200"

Master Base Paging Transmitter with phone Interface

Protocol: Serial ASCII or numeric keyboard
Data Format: RS-232-C
Communication Rate: Data rate via the serial bus is 1200 BPS, N,8,1 with hardware flow control

JTech Pager Network

Protocol: JTech with wide area repeater broadcast
Communication: FSK POCSAG format 512 BPS

Transmitter:

Frequency Range: 450-470MHz. 12.5 KHz single splinter channels
Power Output: 2 watt maximum
Antenna: 1/4 wave whip
Frequency Stability: .00025% (2.5 ppm)
Modulation: FSK/ direct FM 512 BPS
Emission: 7K0F1D

Physical and Environmental

Operating Temperature:	-30oC to + 60oC (paging master station) 0oC to + 70oC (belt worn pager)
Storage Temperature:	-30oC to +60oC
Humidty:	0% to 90% non-condensing
Size:	Master Base Paging Transmitter: 2.7in (67mm) Height x 14in (355mm) Width x 6.1in (155mm) Depth
Weight:	Master Base Paging Transmitter: 1.2lbs. (.543 Kg.)

Technical Description Overview

A SmartAlert 200 Premise Paging System

The JTECH SmartAlert 200 system consists of frequency synthesized transmitter and telephone interface designed to provide paging from private phone system.. A RS-232-C port is available so that a terminal or desktop computer can be used to input alpha numeric messages.. This capability allows the transmitter data input and paging message to be input by standard telephone touch tone keypad.
The SmartAlert 200 operates on 12.5 kHz or 25 kHz UHF assigned channels. The RF transmitter maximum output power is 2 watts and the encode data rate is 512 bps. Emission type is 7K0F1D.

B. SmartAlert 200 Master Base Paging Transmitter

The paging transmitter is frequency synthesized and uses a phase lock loop (PLL) design. The reference oscillator is a voltage controlled temperature compensated crystal oscillator (VC-TCXO) and determines the temperature frequency stability of the final output. The design uses a number of control elements to insure that the final transmit channel is achieved before enabling the power amplifier. Modulation of the loop requires modulating the voltage controlled oscillator (VCO) and the reference oscillator. A 2 port modulation scheme insures good fidelity modulation for the low frequency paging data. Additional circuits under control of the micro processor via an I2C bus control factory set channel frequency, RS-232-C interface.

C. Major Component Count and Active Devices on transmitter board

Integrated and hybrid circuits 10 and transistors 2

U1 RF Power Module Hybrid integrated circuit	RA07N4047M
U2 Voltage regulator + 5 volts	UMC5N
U3 Analog switch	MC14053
U4 Quad Operational Amplifier	LMC6582
U5 Voltage regulator + 9 volts	L78S09CT
U6 RF Preamp	MAV-11BSM
U7 PLL synthesizer integrated circuit	ADF4110
U9 TCXO Hybrid integrated circuit	TEW TX1824M
U18 I2C-2-Parallel Converter	PCF8574A
Y1 Voltage control oscillator VCO hybrid	RTVCA450-10
Q1 Transistor	MMBT3906
Q3 Power control voltage follower	MMBT2222
U5 RS232 Tranceiver	MAX232

Technical Description Detail Pager Master Transmitter

Frequency Synthesizer

a. Reference Oscillator and VCTCXO

The reference oscillator provides the frequency stability vs. temperature characteristic for the transmitter. The reference element is compensated to better than 2.5 ppm and is supplied as a pre-packaged hybrid unit or equivalent. Modulation is direct FM introduced to a varactor port and provides low frequency data modulation. The output of the reference at 9.6 MHz. is applied to the synthesizer U7 where it is internally divided to provide a reference frequency of 12.5 KHz.

b. PLL Synthesizer, Data Modulation, and Loop Filter

The PLL system consists of three (3) main devices; the synthesizer IC U7, VCO Y1, and the reference oscillator. Control of the synthesizer U7 is provided by microcontroller and resident firmware. The synthesizer uses a dual modulus pre-scaler and is a standard indirect PLL technique. The IC U7 consists of phase/frequency detector, 1/N counter or main divider, two modulus counter and control, and reference counter.

Main control of these internal circuit blocks within U7 is via control over an I2C bus to PIN 12 of U7. Data clock is provided to PIN 11. The reference oscillator operating at 9.6MHz. is divided to a fixed 12.5 kHz. Control of the 450-470 MHz VCO is via U7 phase frequency comparator and charge pump circuit with external loop filter.

The appropriate value of the 1/N counter can be obtained from the 2 modulus equation with the 2 modulus count equal to 31/32, the reference frequency at 12.5KHz. and the VCO frequency equal to the transmit channel. The loop filter is a conventional low pass with phase lead compensation provided by R12 and C60. Pre-integration of the charge pump pulses is provided by C34 and additional reference filtering of the charge pump pulses is provided by R39 and C35. Modulation fidelity is maintained by introducing the data signal at 2 points in the loop. One data signal is applied to the VCO control line voltage via the loop filter. The other is introduced to the reference oscillator. In order to modulate the VCO correctly, and introduce a summing junction for modulation and VCO control. The modulation signal voltage is converted into a current. R38 provides this function.

Data shaping for the VCO modulation is provided by low pass filter R40 and R41 and C61. Data shaping for the reference oscillator and VCO modulation port is provided by a low pass data filter. U4.and U3 along with R20, R26, R28, and C47 through C49 provide a low pass filter. Additional filtering is provided by R40, R41 and C61. Since 2 point modulation is used it is necessary to control the amount of deviation contributed to each modulation port. An imbalance of signal at one port or the other will produce either excessive integration or differentiation of the modulation. Since the modulation gain of the reference is much less than the VCO, deviation adjustment is directly connected to U9 the reference oscillator and controlled by R5 and R4. Deviation compensation is controlled by R54.

Transmitter Controller (Master controller board)

c. Microcontroller

The controller 80c52 provides via an I2C interface bus programming of the synthesizer U7. In addition the microcontroller encodes the input data from the RS232 or telephone input and finally into POCSAG data format. The POCSAG format provides modulation signal with no significant low frequency component. The

Microcontroller firmware also handles power management routines including switching the power amplifier on after frequency and phase lock is achieved. The controller clock is 12 MHz. set by C1 and C2 and crystal Y1. External communication via a serial port JP5 with the controller is handled by an RS-232 interface U3. This device contains an internal voltage charge pump with C5 through C9. RF decoupling of the RS-232 port is provided for via L1 through L4 and C10 through C13. Remaining ports of the controller are dedicated to the I2C bus with serial data, serial clock, and the power amplifier enable line.
A set of 5 volt regulators provide low noise stable supply voltage for the PLL and components. U5 provides continuous 5 volts while U2 provides 5 volts only in transmit.

RF Power and Supply Distribution

d. Power amplifier and Low Pass RF Filter

The VCO output Y1 pin 6 is applied to a resistive power splitter and attenuator using R7, R8 and R9. This split and reduced power is input to the synthesizer pre-scaler at PIN 6 and the pre-amp U6 pin 1. The pre-amp output is matched to the input pf the power amplifier hybrid module U1 PIN 1 through a pi network R6, R14 and R15. A one milli-watt signal (0 dbm) input to the PA module provides rated output power and is factory set via power adjust R25. Low source impedance voltage control for PA power adjustment is provided by emitter follower Q3. Power amplifier enable is controlled by Q1. An out of lock condition forced by the PLL will cause Q1 to an OFF state. With these pins low no output power will occur.
During transmit maximum current passes to U1 PIN 3.. RF output is obtained at U1 PIN 4 and is low pass filtered by a 7 section Chebychev filter using C36 through C38 and C42 along with L6 through L8.

e. Power Distribution

Main power supply distribution is from a 13.5 volt external power supply. This supply is rated at 2.4 amps maximum, 35 watt and has built in shut down protection for short circuit protection. Reverse polarity protection is provided by D3. This could occur if incorrectly polarized DC plug or incorrect power supply is used. Supply via J1 is RFI filtered via L1, L2 and C5. Additional voltage regulators on transmitter board provide constant 5 and 9 volts Transient control of power and frequency is maintained by shaping the transmit enable signal controlling Q3. This is accomplished by voltage divider R17, R27, R25 and R30 along with C16 and C17.