Technical Description Overview

A.The Series 2600 desktop transmitter operates on 12.5 kHz or 25 kHz UHF assigned channels. The RF transmitter maximum output power is 2 watts and the encode data rate is 1024 bps. Emission type is 7K0F1D.

B. Series 2600 transmitter

The paging transmitter is frequency synthesized and uses a phase lock loop (PLL) design. The reference oscillator is a voltage controlled temperature compensated crystal oscillator (VC-TCXO) and determines the temperature frequency stability of the final output. The design uses a number of control elements to insure that the final transmit channel is achieved before enabling the power amplifier. Modulation of the loop requires modulating the voltage controlled oscillator (VCO) and the reference oscillator. A 2 port modulation scheme insures good fidelity modulation for the low frequency paging data. Additional circuits under control of the micro processor via an I2C bus control factory set channel frequency, RS-232-C interface.

C. Major Component and Active Devices on transmitter section

U20 Voltage regulator + 9 volts	l78scv
U1 Voltage regulator + 5 volts	lm7805
U3 Analog switch	CD4053
U4 Quad Operational Amplifier	LMC6582
U8 RS-232 Serial Interface integrated circuit	MAX232A
U6 RF Power Module Hybrid integrated circuit	RA07N4047M
U7 PLL synthesizer integrated circuit	ADF4110
U8 Buffer amp	MAV11BSM
U9 TCXO Hybrid integrated circuit	TEW TX1824M
Y3 Voltage control oscillator VCO hybrid	RTVCA450-10
Q2 Digital Transistor	BCX17
Q3 Power control voltage follower	MMBV2222

Technical Description Detail Pager Master Transmitter

Frequency Synthesizer

a. Reference Oscillator and VCTCXO

The reference oscillator provides the frequency stability vs. temperature characteristic for the transmitter. The reference element is compensated to better than 2.5 ppm and is supplied as a pre-packaged hybrid unit or equivalent. Modulation is direct FM introduced to a varactor port and provides low frequency data modulation. The output of the reference at 9.6 MHz. is applied to the synthesizer U7 where it is internally divided to provide a reference frequency of 12.5 KHz.

b. PLL Synthesizer, Data Modulation, and Loop Filter

The PLL system consists of three (3) main devices; the synthesizer IC U7, VCO Y3, and the reference oscillator. Control of the synthesizer U7 is provided by microcontroller and resident firmware. The synthesizer uses a dual modulus prescaler and is a standard indirect PLL technique. The IC U7 consists of phase/frequency detector, 1/N counter or main divider, two modulus counter and control, and reference counter. Main control of these internal circuit blocks within U7 is via control over a control bus to PINs 11-14 of U7. Data clock is provided to PIN 8. The reference oscillator operating at 9.6MHz. is divided to a fixed 12.5 kHz. Control of the 450-470 MHz VCO is via U7 phase frequency comparator and charge pump circuit with external loop filter. Appropriate value of the 1/N counter can be obtained from the 2 modulus equation with the 2 modulus count equal to 31/32, the reference frequency at 12.5KHz. and the VCO frequency equal to the transmit channel. The loop filter is a conventional low pass with phase lead compensation provided by R12 and C60. Pre-integration of the charge pump pulses is provided by C34 and additional reference filtering of the charge pump pulses is provided by R39 and C35. Modulation fidelity is maintained by introducing the data signal at 2 points in the loop. One data signal is applied to the VCO control line voltage via the loop filter. The other is introduced to the reference oscillator. In order to modulate the VCO correctly, and introduce a summing junction for modulation and VCO control, the modulation signal voltage is converted into a current. R38 provides this function. Data shaping for the VCO modulation is provided by low pass filter R40 and 41 and C61. Data shaping for the reference oscillator and VCO modulation port is provided by a low pass data filter. U4.and U3 along with R20, R26, R28, and C47 through C49 provide a low pass filter. Additional filtering is provided by R40, 41 and C61. Since 2 point modulation is used it is necessary to control the amount of deviation contributed to each modulation port. An imbalance of signal at one port or the other will produce either excessive integration or differentiation of the modulation. Since the modulation gain of the reference is much less than the VCO, deviation adjustment is directly connected to U9 the reference oscillator and controlled by R5,R4. Deviation compensation is controlled by R54.

Transmitter Controller

c. Microcontroller

The controller 89c55 provides via an I2C interface bus programming of the synthesizer U7. In addition the microcontroller encodes the keyboard input data with additional bits for error correction and finally into pocsag data format. Microcontroller firmware also handles power management routines including switching the power amplifier on after frequency and phase lock is achieved, if no keyboard activity is The controller clock is 12 MHz. set by C10 and 11 and crystal Y1. External communication via a serial port J1 with the controller is handled by an RS-232 interface U8.

RF Power and Supply Distribution

e. Power amplifier and Low Pass RF Filter

The VCO output Y3 is applied to a resistive power splitter using R15, R16and R17. This split and reduced power is input to the synthesizer prescaler and buffer amplifier.Signal from buffer amp. Is applied to power module U6 . Power Module provides rated output power and is factory set via power adjust R52. Low source impedance voltage control for PA power adjust is provided by follower Q3. Power amplifier enable is controlled by a series transistor switch Q2 switch. RF output is obtained at PIN 4 and is low pass filtered by a 7 section Chebychev filter using C36 through C38 and C42 along with L6 through L8.

f. Power Distribution

Main power supply distribution is from an 13.6 volt external power supply. This supply is rated at 2.4 amps maximum, and has built in shut down protection for short circuit protection. Reverse polarity protection is provided by D2. This could occur if incorrectly polarized DC plug or incorrect power supply is used. Supply via J2 is RFI filtered via L2, L3 and C1,C2 .