DUTY_CYCLE_BILL.doc

This is the billion code modulation duty cycle calculation. Refer to FCC 47 CFR Ch. 1 (10-1-02 Edition) Page 691.

	ON	OFF	TOTAL TIME
1 msec first sync pulse	1 mS	N/A	1 mS
10 digits	30 mS	10 mS	40 mS
37 msec blanktime	N/A	37 mS	37 mS
3 msec second sync pulse	3 mS	N/A	3 mS
4.666 digits	14 mS	5 mS	19 mS
Total	48 mS		100 mS

20 log 48/100 = -6.37

NOTES:

Each digit allowed 4 mS. Each digit starts with an OFF mS.

1 mS/bit

Could be all OFF	0 mS ON	4 mS OFF
Could be 1 ON	1 mS ON	3 mS OFF
Could be 2 ON	2 mS ON	2 mS OFF
Could be 3 ON	3 mS ON	1 mS OFF (WORST CASE)

This calculation has all bits ON for each digit (WORST CASE). This would rarely happen in a transmitter because all ON for the digits would be an unrealistic transmitter code.