NOVATEL WIRELESS

Technical Description

(Theory of Operation / Description of Frequency Determining Circuits / Description of Spurious and Harmonic Suppression Circuits)

for

NRM-6831 CDPD PC Card

TS-01016602

NOVATEL WIRELESS

REVISION HISTORY

REV#	ER/C#	EFF. DATE	DESCRIPTION	PREPARED	APPROVED
0			**Copied from Vespa**		
1			Modified for PC Card	G. May	

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1. INTRODUCTION

This document is intended as a complete technical description of the Novatel CDPD PC Card (NRM-6831), Novatel Part Number 01016602. The sections that follow give a theory of operation and component level design description. Wherever possible, typical waveforms, bias points, and signal levels are given as an aid to understanding operation.

The sections of this document are ideally self-contained with as few references to outside material as practically possible. References to other documents are shown in ***italics*** for ease of location.

2. INTERFACE SPECIFICATION

2.1 Baseband Interface

Power, data, and control signals are connected to the Novatel CDPD PC Card via a 68-pin PC Card connector J401. The pin assignment is given in *PC Card Standard - Volume 2: Electrical Specification.*

2.1.1 Power Connections

The operating power supply to the NRM is via VCC1,2 and GND. The two VCC lines on the PC Card are tied together at the interface connector. The grounds on the PC Card are tied together at the interface connector. Both VCC lines should be 5.0 VDC ± 5%, over the current range of 0 to 1000 mA.

It should be noted that all exposed metal is connected to the ground plane.

2.1.2 Signal Connections

The NRM is controlled via a TTL logic level PC Card bus comprised of Data, Address, and Control lines. All inputs are 5 Volt tolerant, and all output levels are standard 3.3 V.

2.2 RF Interface

The antenna connection to the NRM-6831 is via a connector soldered to the PCB.

3. ELECTRICAL SPECIFICATIONS

3.1 Power Supplies and Power Control

Power in the NRM is very compartmentalized. Each major section of circuitry has its own controllable regulator. 5.0 V DC is supplied on the PC Card VCC pins. The distribution of power is as follows:

VDC:	Vcc	3.3 V	Digital logic supply
	An_3V	3.0 V	Mixed signal circuitry
	Rx_3V	3.0 V	RF Receive section

Tx_3V	3.0 V	RF Transmit section
VDCPA	3.6 V	RF power amplifier
		The PA limiter (regulator) is a discrete design with a P-channel FET

3.1.1 PC Card VCC

The host provides the NRM with 5.0 VDC ± 5% at VCC1,2. This net is called VDC. VDC is used as the supply for the four low-dropout regulators and PA current limiter shown.

3.1.2 Digital Power (VCC)

VCC is the 3.3 V power supply for the NRM CPU and associated circuitry. VCC is generated by regulator U102, which is supplied by VDC at filtering capacitor C131. U102 is always enabled. Bulk output filtering is provided by C102 and C130.

3.1.3 Analog Power (AN_3V)

The baseband analog circuitry is powered by the supply AN_3V. This is derived by presenting VDC to regulator U303. U303 is controlled by the CPU by tying its CTRL line to AN_3V_EN. Bulk output filtering is provided by C332. Capacitor C316 provides filtering for the internal reference of the regulator.

3.1.4 RF Transmitter Power (TX_3.0V)

The NRM transmitter circuitry, with the exception of the PA itself and the modulator is powered by the 3.0 V supply TX_3.0V. This is generated by passing VDC through the filter C284 at the input of regulator U212. This regulator's output is enabled by the control signal TX_ON. Bulk output filtering is provided by C282. Capacitor C207 provides filtering for the internal reference of the regulator.

3.1.4.1 PA Power Supply (VDCPA)

The NRM uses a GaAsFET PA and requires no negative gate bias. VDC is passed through Q501, a P-channel FET that is used to drop it down to approximately 3.6 V. The limiter is always on, therefore, power is always applied to the PA. The circuit is sensitive to the FET's (partial) on characteristics and must be retuned if a FET other than the NDS8434A is used.

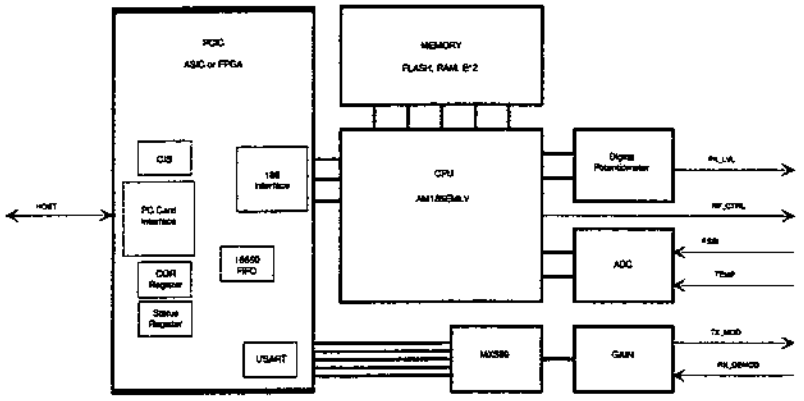
3.1.5 RF Receiver Power (RX_3.0V)

The NRM receiver circuitry, VCOs and modulation circuitry is powered by the 3.0 V supply RX_3.0V. This is derived by passing VDC through capacitor C283 at the input of regulator U213. Bulk output filtering is provided by C287. Capacitor C205 provides filtering for the internal reference of the regulator.

3.2 Baseband Circuitry

The baseband section of the NRM looks somewhat like:

CDPD ------3.3volt Baseband Block Diagram
TYPEII



The CPU is the central controller of the module, running the TCP/IP and CDPD protocol software along with any host level interface software required. RF control also emanates from the CPU with separate ADC and DAC units handling the analog control signals. Digital modulation signals to and from the CPU are processed, via the USART (implemented in the PCIC), by the MX589 GMSK Modem and a variable gain block.

3.2.1 CPU and Support

3.2.1.1 CPU

The CPU (U1) is an AMD AM186EMLV in a 100-pin TQFP package. This device is powered by VCPU and is decoupled by C121, 122, 124, 125, 128. CPU reset is provided by PCIC using the bits in the COR and the reset line on the PC Card interface. The CPU is provided with a 24.576 MHz clock, which yields a bus speed of 24.576 MHz.

3.2.1.2 PCIC

The PCIC (U401) is an ASIC or FPGA. The clock for PCIC is provided by the CPU (24.576MHz).

When implemented as an FPGA (Xilinx Spartan 30 XL) the program for the FPGA is downloaded in master serial mode from the SPROM (U402). R420 is used to pull down the Mode pin to configure the FPGA into this programming mode. The FPGA may be programmed from the download cable in slave serial mode by removing R420 and fly-wiring the appropriate signal out to the download cable. While the FPGA is in the initialized (unprogrammed) or programming states, the CPU is held in reset.

Implemented in PCIC is a full PC Card interface, a 16550 FIFO, a 8251 USART, and the interface to the CPU.

3.2.1.2.1 PCIC PC Card interface

The PC Card interface terminates the 68 pin PC Card connector (J401). This interface is a data/address/control bus. The PC host is the master of this bus and provides the address and control lines. PCIC acts as a slave and executes the read/write accesses. PCIC can also generate an interrupt to the PC host. Only accesses on the low byte of the 16 data lines are supported. All PCIC PC Card interfaces are 5V tolerant, and the outputs are standard 3.3V CMOS.

The CIS address space on the PC Card interface is used to identify the PC Card and it's capabilities to the host. The CIS is implemented in PCIC as a block of RAM. This ram is uninitiated on power-up and must be loaded from the CPU before the PC Card interface is enabled.

The COR (Configure Option Register) and the Status Register are the only registers supported on PCIC.

For more information on the PC Card interface signals and address spaces, please refer to the ***PC Card Standard - Volume 2: Electrical Specification***.

3.2.1.2.2 PCIC 16550 FIFO

The 16550 FIFO is available to the PC host when the PCIC is put in I/O mode. PCIC emulates a 16550 UART with 16 byte FIFO. This is used to transfer data between the host and the CPU. From the host's perspective, the 16550 look like a standard COM port. The host sends/receives data as if it was talking to a serial interface on the COM port. The data written into the emulated 16550 is placed in the FIFO. This causes an interrupt on the CPU, and the CPU reads out the data. The similarly the CPU may write data into the FIFO, causing an interrupt on the host, at which time the host may read the data out of the FIFO. The data is always store in the FIFO on PCIC and is never serially transmitted.

3.2.1.2.3 PCIC 186 interface

The PCIC appears on the 186 bus as a peripheral in the 186's I/O space. The PCIC is capable of generating interrupts to the CPU. Chip select for PCIC is provided by CPU pin 88 (PCS1) which decodes I/O addresses 0x1000-0x103F.

3.2.1.2.4 PCIC USART

The USART is a programmable communications interface used to pass data between the CPU and the GMSK modem.

Independent bit clocks for both RX and TX data are provided by the GMSK modem.

3.2.2 Memory and Decoding

The NRM has three memory devices; FLASH EEPROM, Static RAM, and Serial EEPROM.

3.2.2.1 Memory Map

Required to be added

3.2.2.2 FLASH EEPROM (Firmware)

The primary firmware storage is provided by the FLASH EEPROM U101. Currently, this is a 2 Mbit AM29LV200 organized in 16-bit mode (pin 47, _BYTE, pulled high) to provide 128 kwords of storage. The chip is powered by VCC and decoupled via C123.

3.2.2.3 Static RAM (Working Memory)

The 1 Mbit (64 kwords) Static RAM, U104, provides the working memory for the NRM. The chip is powered by VCC and decoupled via C120.

3.2.2.4 Serial EEPROM (Non-Volatile Storage)

The NRM requires non-volatile RAM in order to store such information as calibration factors, IP addresses, and such. U103 is 16 kbit EEPROM which communicates with the CPU using the standard microwire GPSB bus. U03 is powered by VCC.

3.2.2.5 Firmware Loading

The AMD embedded processor family lacks an integrated bootloader. As such, it is required that NRM firmware be programmed into FLASH before it is populated.

3.2.3 Analog Support

The CPU is required to measure and generate analog voltages in order to control the RF deck. This is accomplished as follows.

3.2.3.1 PA Control

U300 is a 8 bit 100K digital pot. It is powered by AN_3.0V and decoupled by C327. Data is loaded into the digital pot input register from the GPSB bus. The digital pot provides a voltage divider ratio based on the regulator output to control the PA power.

3.2.3.2 ADC

U304 is a four channel, 8 bit ADC with a serial interface. It is powered by VCC and decoupled with C329 and C31. U304's reference voltage is generated internally and filtered with C333.

Currently, only two input channels are used. CH0 measures the RSSI reading generated by the demodulator IC. CH2 reads TEMP provided by the resistor divider of thermistor RT201 and R218.

3.2.4 CDPD Data

All digital processing of the CDPD data stream is performed in the CPU. Converting the digital stream to and from an analog GMSK signal for the RF deck is handled by the GMSK modem.

3.2.4.1 GMSK Modem

The NRM uses a MXCOM (original CML design) GMSK modem called a MX589 (U301). This device takes incoming serial data from the PCIC USART and generates an outgoing GMSK

modulation signal with a bit rate of 19,200 bits/second and BT=0.5. Incoming demodulated data is conditioned and converted to a serial bit stream to the USART.

U301 is powered by AN_3V and decoupled with the combination of C304 and C324. Pins 8 (RX_PSAVE) and 18 (TX_PSAVE) are tied low, disabling the power save modes. A 4.9152MHz input is provided from PCIC and forms the signal-processing clock of the device. (PCIC derives this signal by dividing it's 24.576 Mhz clock by 5.) Pins 3 (CLKDIVA) and 4 (CLKDIVB) set the internal bit clock to 19,200 bits/second. Pin 15 (BT) is pulled high, setting BT to 0.5. The bias voltage generator (pin 9, VBIAS) is filtered by C330. This voltage is also presented to the alignment gain block.

Transmit data is presented at pin 19 (TX_DATA). This data is internally synchronized to the 19,200 bit clock. This same clock is used to pull the data out of the USART using pin 22 (TX_CLK). The output TX_OUT (pin 16) is filtered with R324 and C307 to reduce high frequency noise and is presented to the alignment gain block as 1Vpp centered at VBIAS. The input TX_EN (pin 17) can be used to send the TX_OUT pin to a high impedance state. In normal operation, this enable is pulled high through R321. Using this enable to facilitate alignment is covered in ***TP-01015984 - NRM-6831Alignment Process***.

Demodulated receive data from the RF deck is directly coupled (R319) to improve sensitivity. It is then connected to the receive input amplifier of U301. This is a standard inverting amplifier with the negative input (RX_IN, 11) and output signals (RX_FB, 10) available. R326,C303 set the gain of the amplifier and provide a cutoff of about 72KHz. The signal level at RX_FB should be 1Vpp centered at VBIAS. Internally, this signal is further filtered and centered about U301's bias point with the aid of external sample and hold capacitors C322 and C323 connected to pin 13 (DOC1) and pin 14 (DOC2) respectively.

The modem performs clock recovery from the demodulated signal under control of pin 6 (RXDCACQ) and pin 7 (PLLACQ). These pins are connected together and controlled by the CPU via U100's pin 71 (DT). Setting this control high results in the internal clock circuitry entering acquire mode. When low, the PLLs settle into tracking mode. The input: _RX_HOLD (pin 5) can be used to free-wheel the PLLs during signal fades. This signal is connected to the CPU's P2.6 output. It is activated during channel tuning operations. This prevents DC transients in the receive baseband signal from affecting the MX589's ability to synchronize to the incoming data stream. Binary receive data is presented at RX_DATA (20) with the recovered clock at RX_CLK (21). These signals are connected to the USART.

3.2.4.2 Alignment Gain

Alignment of RF transmit deviation is performed by a programmable digital potentiometer (U300) with 8 bits of resolution.

3.2.5 Clock Sources

The NRM has two independent clock sources. The primary module clock is provided by the 15.36MHz TCXO (U208) in the RF section. This is the source for the RF synthesizers. For the baseband circuitry, a CPU clock is required of 24.576 MHz. This is provided by a 24.576 MHz Xtal (Y100). This clock is used to derive the 4.9152MHz clock for the GMSK modem U14. This signal clocks the modem IC and the USART.

3.2.6 Power Management

The power management for the NRM-6831 is implemented as per the CDPD 1.1 specifications. The modem has one low power mode known as sleep mode in which baseband section is placed in a low power state and the receive section is periodically turned on to monitor the channel.

3.3 Baseband To RF Deck Interface

The baseband to RF deck interface signals of the NRM can be found at the right edge of schematic page 3. With few exceptions, the digital control lines are all filtered with series 1.2 k resistors and 470 pF capacitors to ground. Transmit and receive analog information should be AC coupled at the baseband side. The individual signals are summarized in the table below and described in detail in the following sections. A block diagram of the RF deck is shown below.

Signal	Direction	Purpose
PA_LEVEL	BB→RF	DC control level for the PA power control.
LNA_GAIN	BB→RF	Control of LNA gain
RX_ON	BB→RF	Enables the receive section
TX_ON	BB→RF	Enables the transmit section
LOOP_ENAH	BB→RF	TX synthesizer loop control. 1 = closed loop.
SYNTH_CLK	BB→RF	Synthesizer serial control bus clock.
SYNTH_DATA	BB↔RF	Synthesizer serial control bus data.
SYNTH_LE	BB→RF	Synthesizer serial bus load enable
SYNTH_LD	BB←RF	Lock status line from synthesizer. 1=Locked
TX_DET	BB←RF	Reports if RF power is present at the PA output. 1=RF present
RSSI	BB←RF	Receive signal strength indication.
TCXO_CTRL	BB→RF	DC control for the TCXO frequency
TX_MOD	BB→RF	Transmit information to the TX modulator.
RX_DEMOD	BB←RF	Demodulated data from the receiver.

RF Block Diagram

3.3.1 Power Signals

VDC is the main power supply to the NRM RF deck. Currently, its voltage is specified as 5.0 V. This is regulated to provide separate RX 3V and TX 3 V supplies and the VDCPA is also fed directly to the PA. Current handling requirements for this supply are ???mA during transmissions at full power (0.6W).

PA_LEVEL is the output of a 8 bit digital potentiometer. This signal acts to control the PA's output power. For PL7, the voltage is in the range of ???V. For PL2 (max), the voltage is in the range of ???V. The load on this line is typically ?? kohm.

3.3.2 Synthesizer Control Signals

SYNTH_CLK and SYNTH_DATA are the serial communication lines between the CPU and the synthesizer IC. These lines are used to program the synthesizers to tune to various frequencies. Data is latched on the rising edge of the clock. Maximum allowed clock frequency is ??? kHz. Typically, the NRM uses 320 kHz. The exact data formats can be found in the manufacturers' data sheets for synthesizer U210. The synthesizer (LMX1601) requires typical TTL levels or better and are high impedance (1mA typ).

SYNTH_LE are the enable signals for the serial communications interface to the synthesizer. The latch enable line for the synthesizer should be pulsed high for 2 us, or longer, after the rising edge of the last SYNTH_CLK cycle of the transfer. Level requirements ???.

LOOP_EN is used to break the 90MHz TX LO loop. If LOOP_EN is high, then the 90MHz VCO is controlled by the synthesizer in the normal fashion. If this signal is low, then the VCO free runs at its last control voltage. LOOP_EN is typically pulsed low during transmit bursts. The signal load is >100 kohm.

3.3.3 Status Signals

SYNTH_LD are status signals from the synthesizer indicating that it is in lock. A high level indicates that the synthesizers are functioning properly and the PLLs are locked. These are TTL level outputs capable of 1 mA. Care should be taken to debounce these lines in software, as they will oscillate as the synthesizers settles on a new frequency.

RF_DET indicates the presence of RF power at the output of the PA. It is used as a fail-safe by the CPU to ensure that no false transmissions are allowed. Typically, the CPU should shut down the NRM if RF is detected in a situation where the CPU hasn't enabled transmissions. This is a TTL level signal with 100 kohm source impedance. A high level indicates the presence of RF power.

RSSI is the receive signal strength indication from the demodulator IC. This level ranges from approximately 1.0 V for receive signals near the sensitivity level of -116 dBm, to 2.3 V at a high level of -50 dBm. This should be terminated in a high impedance.

3.3.4 Modulation Signals

TX_MOD is the signal to be modulated onto the carrier. It should be AC coupled. Typically 35 mV_{RMS} results in 1.0 kHz transmit deviation. The impedance seen by this signal is <68 kohm

RX_DEMOD is the signal from the final stage of the demodulator IC. It should be DC coupled. Typically, 1.0 kHz deviation at the receiver produces 35 mV_{RMS}. This is a low impedance source.

3.4 RF Synthesizers and VCOs

There are two phase locked loops (PLLs) in the RF deck. One is a fixed frequency oscillator operating at 90 MHz. The other is a UHF VCO tunable from 914.01 to 938.97 MHz. The UHF oscillator (referred to as RFLO) is the first LO used in the receiver section. It is also mixed with the 90 MHz oscillator (in the TX Mixer) to generate the transmit carrier (824.01 to 848.97 MHz). Data and voice are modulated onto the 90 MHz oscillator (referred as TXLO).

The TCXO operating at 14.85 MHz is also fed to a clock tripler Q201 to provide the Rx second IF LO at 3X14.85MHZ or 44.55MHz.

3.4.1 Specifications

The following is a list of electrical specifications for the two main voltage controlled oscillators (VCOs) in the NRM.

3.4.1.1 UHF VCO

Parameter	Min	Typ	Max	Units
Operating Frequency	914	---	939	MHz
Supply Voltage	-	3.0		volts
Supply Current			8	mA
Output Impedance		50		ohms
Output Power	-6			dBm
Control Voltage	.5	---	2.7	volts

3.4.1.2 TXLO

Parameter	Min	Typ	Max	Units
Operating Frequency		90		MHz
Supply Voltage		3.0		volts
Supply Current		4.5		mA
Output Level		-10		mVRMS
Control Voltage		1.3		volts

3.4.1.3 RXIFLO

Parameter	Min	Typ	Max	Units
Operating Frequency		44.55		MHz
Supply Voltage		3.0		volts

3.4.1.4 TCXO (Reference Oscillator)

Parameter	Min	Typ	Max	Units
Oscillator Frequency		14.85		MHz
Supply Voltage		3.0		volts
Supply Current			2	mA
Frequency Stability		+/- 1		ppm
Output Level	0.8			VPP

3.4.2 Overall Circuit Description

Among the two PLLs, there is only one high frequency VCO, which is used in conjunction with a lower frequency one. The RX 2nd LO is a tripler circuit coming directly off the TCXO. This topology was chosen for the following reasons:

- Synthesis of all LO frequencies eliminates tuning points, minimizing manufacturing costs and the effects of component tolerances and temperature drift.

- TX modulation at a single, low frequency improves linearity over temperature and across the transmit band
- Only one high frequency prescaler is required which helps reduce current consumption and cost
- Only one high frequency VCO is required which simplifies circuit design and cost (expensive resonators and high frequency transistors)

The PLLs of the RF deck are synthesized by U210, a National Semiconductor LMX1601 low cost dual PLL. The tripler, Q201 is biased with a simple 2 resistor bias, because the second IF mixer on the demodulator IC is not sensitive to voltage level. The integrated charge pumps of the synthesizers drive passive loop filters. The outputs of these in turn provide the control voltages to each of the two VCO's.

3.4.3 Detailed Circuit Description

3.4.3.1 RFLO

The output of UHF VCO (U203) is buffered by amplifier U201 before it splits into two through a power divider. The output of the power divider feeds both the 1st RX Mixer (U202) and the TX Mixer (U207). The synthesizer IC (U210) input is taken directly from U203 through C226.

3.4.3.2 RXIFLO

This function is a clock tripler consisting of transistor Q201, with the tuned circuit of L218, L226, C206, C295 as the resonator. The VCO frequency is controlled by the TCXO output, which is tripled.

1.1.3.3 TXLO

The TX VCO (Q202) is an oscillator with the output from this going to the TX Mixer (U207), and is coupled to synthesizer IC U210 by C219. Details of this PLL follow.

3.4.3.3 Circuit Design Considerations

3.4.3.3.1.1 Modulation

To minimize gain variations from unit to unit, data (TX_MOD) is modulated onto a second varactor (CR201) which has a fixed reverse bias and is lightly coupled to the resonant circuit through C223.

1.1.3.3.1.3.1 Loop Control

The signal LOOP_EN controls analog switches U215 to open or close the PLL. The switch is normally closed, and the PLL remains in lock, with the resulting frequency accuracy of the reference oscillator.

The TXLO is run open-loop during transmission in order to eliminate the phase error, which would otherwise appear on the modulated carrier, since the error correction signal of a closed PLL would tend to cancel the frequency deviation applied to the VCO by the modulating data. Until the loop is opened, C274 and C277 are charged to the DC voltage, which hold the VCO at exactly 90 MHz. In the open loop state, the switch, U215, appears as an open circuit. The NRM will operate within

its frequency accuracy specification for data bursts of up to 1.5 seconds duration, which is the maximum burst length allowed by the processor.

3.5 Receiver

This section discusses the design of the NRM receiver. Topics covered by the receiver's technical description are electrical specifications; basic circuit block descriptions, and detailed technical description of the circuits.

3.5.1 Specifications

3.5.1.1 SAW Diplexer Filter

Parameter	TX Filter	RX Filter	Units
Center Frequency	836.5	881.5	MHz
Bandwidth	25	25	MHz
Insertion Loss (max)	2.5	4.3	dB
Ripple (max)	1.5	2.5	dB
VSWR (max)	2.5	2.7	
Input Power	1.2	1.2	W
Attenuation 869-894 MHz	40		dB
Attenuation 824-849 MHz		50	dB
Attenuation 914-939 MHz		35	dB

3.5.1.2 SAW Band Pass Filter

Parameter	Value	Units
Center Frequency	881	MHz
Bandwidth	25	MHz
Ripple (max)	2	dB
Insertion Loss (max)	3	dB
VSWR (max)	2.5	
Attenuation TX Band (min)	20	dB
Attenuation LO + Image Band (min)	20	dB
Termination Impedance	50	Ω
Operating Temperature Range	-30 to +85	°C

3.5.1.3 RF LNA/Mixer

Parameter	Value	Units
RF Input Frequency Band	869-894	MHz
LO Input Frequency Band	914-939	MHz
IF Output Frequency	45	MHz
LNA Gain	18.5	dB
LNA Noise Figure	1.8	dB
LNA Supply Current	5	mA
Mixer Supply Current	3-4	mA

Mixer Conversion Gain	0	dB
Mixer Noise Figure	< 12	dB
Input Return Loss	> 10	dB
LO Drive Level	-4	dBm

3.5.1.4 IF Crystal Filter

Parameter	Value	Units
Center Frequency	45	MHz
Bandwidth (min)	30	kHz
Ripple (max)	1	dB
Insertion Loss (max)	3	dB
15 dB Stop Bandwidth	60	kHz
Image Attenuation (fc=900 kHz)	70	dB
Termination Impedance	1.1 kΩ // 0 pF	
Operating Temperature Range	-30 to +85	°C

3.5.1.5 IF Amplifier

Parameter	Value	Units
Operating Frequency	45	MHz
Input Impedance	1.2	kΩ
Output Impedance	7	kΩ
Current Draw	<1.5	mA
Gain	>8	dB
Output 3 dB Compression Point	>-10	dBm

3.5.1.6 FM Demodulator IC

Parameter	Value	Units
Supply Voltage	2.7-6.0	V
Quiescent Current	5	mA
Operating Temperature	-30 to +85	°C
Mixer Input Frequency	45	MHz
Mixer Input Impedance	7	kΩ
Mixer Conversion Gain (min)	15	dB
LO Frequency	44.55	MHz
IF Amp Operating Frequency	450	kHz
Total IF Amp Gain (typ)	118	dB
AM Rejection	45	dB
RSSI Dynamic Range	>60	dB
Demodulation Sensitivity	35 peak	mV/kHz

3.5.1.7 IF Ceramic Filters

Parameter	Value	Units
Center Frequency	450	kHz
Bandwidth 6 dB (min)	+/-15	kHz

Bandwidth 50 dB (max)	+/-50	kHz
Ripple (max)	.5	dB
Insertion Loss (max)	6	dB
Stopband Attenuation 450 ± 100 kHz	47	dB
Group Delay	15	µs
Input / Output Impedance	2	kΩ

3.5.2 Overall Circuit Description

The NRM is a full duplex transceiver using a dual-conversion superheterodyne receiver with high-side LO injection. The transmitter and receiver are connected to a common antenna through an antenna diplexer filter which provides the required isolation and out of band rejection.

On the receive side, the diplexer is followed by a LNA/Filter/Mixer. The 45 MHz first intermediate frequency (IF) signal is fed to a crystal filter, IF amplifier and demodulator.

The IF receiver circuit converts the 45 MHz IF to the 450 kHz demodulated baseband output. Mixing, amplification, detection and RSSI functions are performed by a single IC. The received IF signal is mixed with the 44.55 MHz RXIFLO to produce the 450 kHz second IF. This is amplified and limited, and filtered by two external band pass filters for channel selectivity. The limited, filtered IF is demodulated by a frequency discriminator. An LC tank produces a 90 degree phase shifted signal, which is added to an in-phase signal to produce the demodulated output. Audio gain vs. temperature compensation is also implemented in the demodulator IC.

3.5.3 Detailed Circuit Description

3.5.3.1 Diplexer Filter

The SAW diplexer (FL203) comprises a transmit filter and a receive filter. The transmit filter is used to filter the PA output and to filter the noise in the receive band which prevents desensing.

The receive side of the diplexer prevents any out of band spurious signals from leaking into the receiver and causing interference with the desired signal. It must also attenuate the transmit signal to a level where the first mixer in the receiver is not being driven into compression. Finally, the receive filter in the diplexer must also prevent the first local oscillator from leaking out of the receiver and thus radiating out on the antenna.

3.5.3.2 RF LNA/Mixer

The circuit is configured as an LNA/BPF/Mixer. The LNA has a gain of about 16dB and a noise figure of about 1.8. The filter is primarily to reject the PA for desensing with about 20 dB of attenuation. Image rejection is about 20dB. The mixer is used for conversion from 881MHz to the IF frequency of 45MHz.

1.1.1.3 IF Crystal Filter

The crystal filter's function is to remove the second IF image frequency (44.55 MHz - 900 kHz = 43.65 MHz). It has the secondary effect of contributing to adjacent and alternate channel rejection, although it is not needed for that purpose.

Key factors in the design of the crystal filter section were its impedance match and the amount of isolation provided between its input and output. Out of band attenuation, insertion loss, ripple, and bandwidth are all highly sensitive to the impedance at its output and input ports. L221 and L223 are shielded to improve the input/output isolation of the filter.

3.5.3.4 IF Amplifier

The 45 MHz IF amplifier (Q200) provides enough amplification to meet the sensitivity requirements of the demodulator IC. It also performs an impedance transformation from the crystal filter 1.2 kΩ output impedance to the demodulator IC's 7 kΩ input impedance. DC bias was set to provide adequate gain to the signal, but at a low enough level to not degrade standby performance.

3.5.3.5 IF Receiver

3.5.3.5.1 Second Mixer

The second mixer is internal to the TA31132FN FM demodulator IC (U211). It is a low power VHF monolithic double-balanced mixer. In this application the mixer input is used is a single ended configuration which allows it to be fed directly from the IF amplifier. The 44.55 MHz RXIFLO is fed to the mixer through an internal buffer. This isolates the oscillator output from any 45 MHz RF to LO leakage from the mixer, which may interfere with the RXIFLO PLL operation.

3.5.3.5.2 Limiter and Filter

The second mixer is followed by ceramic filter CF201, an IF amplifier, interstage ceramic filter CF200, and another IF amplifier. The two limiting IF amplifiers have a combined gain in excess of 100 dB, and drive the received signal into hard limiting before it is applied to the FM detector. The limited IF has a degree of AM rejection, except for the very weakest received signal levels. CF200 and CF201 are identical, 4-element, 450 kHz bandpass filters. The filter characteristics are responsible for the adjacent and alternate channel rejection of the receiver.

3.5.3.5.3 FM Demodulator

The limited IF is split into two paths. One is applied directly to one input of the phase detector, while the other is phase shifted 90 degrees and applied to the other input of the detector. The output is a demodulated baseband signal.

The phase shift is accomplished by the quadrature network consisting of C204,245,248, L224, and R247. Capacitor C204, L224 sets the center frequency of the resonant circuit to 450 kHz. R247 loads the Q of the resonator to desensitize the phase shift with respect to change in frequency. C256 is a DC block.

Demodulated FM is taken from the AF output pin and fed into an inverting amplifier. This amplifier is internal to the IC, but its gain and temperature compensation is set by external components. Its gain is set to provide 35 mV_{RMS}/ kHz peak deviation and RT200 is used to adjust the gain to keep the demodulation sensitivity relatively constant over the operating temperature range. The output of this amplifier is the signal RX_DEMOD to the baseband section. There, the signal level is adjusted in gain and processed.

3.5.3.5.4 RSSI circuit

The RSSI circuit on the IC is a logarithmic current-to-voltage converter that senses the level of amplification required by the IF amplifiers to drive the signal into hard limiting. The RSSI output is a DC voltage directly (though nonlinearly) proportional to the power of the received signal

3.6 Transmitter

3.6.1 Specifications

3.6.1.1 Transmit Bandpass Filter (FL201)

Parameter	Value	Units
Center Frequency	836.5	MHz
Bandwidth	25	MHz
Ripple (max)	2	dB
Insertion Loss (max)	3.5	dB
VSWR (max)	2.5	
Attenuation RX Band (min)	25	dB
Attenuation LO + Image Band (min)	30	dB
Termination Impedance	50	Ω
Operating Temperature Range	-30 to +70	°C

3.6.1.2 PA Driver Amplifier (U206)

Parameter	Value	Units
Operating Frequency (max)	1900	MHz
Current Draw (typ)	36	mA
Gain (typ)	21	dB
Gain Variation		dB
Saturated Output Power	11.5	dBm

3.6.1.3 PA (U205)

Parameter	Value	Units
Operating Frequency	824 - 849	MHz
Power Control Current	5	mA
Input Return Loss (max)	-6	dB
Efficiency (min)	50	%
Gain Control Range (min)	20	dB
Max Output Power (7 dBm input)	30.5	dBm

3.6.1.4 Directional Coupler (DC200)

Parameter	Value	Units
Operating Frequency	824 - 849	MHz
Coupling	20 ± 1	dB
Input VSWR (max)	1.3	
Insertion Loss (max)	0.45	dB
Isolation (min)	30	dB
ATTENUATION - 2Fo	25	dB
3Fo	20	dB

4Fo	20	dB

3.6.2 Overall Circuit Description

The 90 MHz TX VCO is directly FM modulated by the Gaussian-filtered baseband data signal TX_MOD to produce a GMSK-modulated IF signal. This is mixed with the RFLO to generate a modulated signal at the transmitter carrier frequency. The upconverted signal is amplified by a fixed gain driver amplifier. This is followed by an interstage filter and the adjustable-gain power amplifier (PA), where the level is boosted to the programmed transmitter power level.

The PA output connects to a directional coupler. The coupler direct port connects to the transmit port of the antenna diplexer filter, and through the diplexer to the antenna port. The coupled port connects to the PA level detector circuit. The level detector produces a voltage proportional to the PA level, which is a control signal for two circuits: the PA level control loop and RF threshold detector. The PA level control loop works by comparing the detector output and the voltage output PA_LEVEL, and adjusting the PA power control line. The threshold detector is intended to output logic signal RF_DET whenever the transmitted power level exceeds -60 dBm, and is used by the controller's RF fail-safe function.

3.6.3 Detailed Circuit Description

3.6.3.1 Modulator

The Gaussian filtered baseband data signal TX_MOD is applied directly to the frequency control port of the TXLO VCO to produce a GMSK modulated RF signal, as already described in the section about ***TXLO***. The level of TX_MOD is controlled by variable gain amplifier U302, which is programmed to yield the required frequency deviation on the modulated output. The TXLO output is upconverted by the transmit mixer to produce the modulated carrier.

- Very sensitive to power supply variations (high pushing figure)
- Load pulling immunity due to mixer power switching is accomplished by increasing the drive level and voltage dividing the load across a resistor
- The modulating varactor is loosely capacitively coupled to the resonating inductor so that the modulation signal is well grounded at 9.6 kHz and therefore is prevented from modulating the VCO varactor.
- The inductor used for the oscillator was chosen for its low profile and tight 3% tolerance so that the parasitic coupling to the shield could be minimized and the tuning range could be reduced.
- The modulator was laid out in the opposite corner to the power amplifier so that the temperature effects during an open loop burst could be reduced. To further reduce temperature induced load pulling the modulator components were spaced close together so that a temperature compensating capacitor would be effective.
- 6200 pF COG capacitors were used for the loop filter to eliminate the loop filter contribution to temperature change induced pulling.

- The CMOS switch used to open the loop was placed in the middle of the loop filter to permit the use of an X7R capacitor and thereby provide for some flexibility in the design of the PLL.
- The PLL loop bandwidth is approximately 1 kHz. The loop bandwidth was opened to the point where there was no evidence of distortion with a 9.6 kHz "1010..." dotting bit pattern so that the loop opening could be delayed to the time just before the sync. word was transmitted. This allows the loop to recover from supply voltage changes and frequency load pulling effects due to power amplifier ramp up.
- The loop filter pole that is usually used for sideband suppression in earlier design is required to increase the total capacitance at the output of the CMOS switch so that when the output capacitance of the switch changes state its effects are minimized.
- Modulating varactor is biased in its most linear region which is 2.1 Volts. Note that the base band circuitry is DC coupled at a level of 1.5 V. This also contributes to the bias.
-

3.6.3.2 Transmit Mixer

The TX mixer uses the NEC UPC8106 mixer IC. The RFLO (914.04 to 938.97 MHz) and TXLO (90 MHz) are mixed to generate the transmit carrier (824.04 to 848.97 MHz). The mixer provides 10 dB of conversion gain (from 800 to 900 MHz).

3.6.3.3 PA Driver Amplifier (U206)

The PA driver amplifier (U206) provides approximately 21 dB of gain, raising the transmit signal strength to a nominal level of +10 dBm. Power is provided by TX_3V and filtered by C266. Switching is provided to achieve the IS-19B requirement of <-65 dBm output power during "carrier off" and "channel switching" times. L220 provides output biasing. No external matching is required for the output. The input is matched into the mixer with C2138, C250 and L200.

3.6.3.4 Transmit Bandpass Filter (FL201)

The transmit bandpass filter (FL201) is a SAW with 25 dB of rejection at the RFLO and image frequencies and about 25 dB out of band. Typical output level of this filter is +7 dBm. The input of the SAW is 50ohm. The output of the SAW is coupled into the PA with C230.

3.6.3.5 Transmit Power Amplifier

3.6.3.5.1 PA Module

The PA module (U205) is a 30.5dBm GaAs Power Amplifier MMIC. It requires no negative voltage and power control is via a high impedance power control input requiring 5 mA drive max.

3.6.3.5.2 Power Control Loop

The PA power control loop senses the PA output power, converts it to a representative voltage, and compares it to the control signal PA_LEVEL, an 8-bit potentiometer output. The PA is capable of >20 dB of dynamic range. Control is achieved by varying the PA's VAPC supply.

The output of the PA is sensed by directional coupler DC200. The direct path is from port A to port B. With port D terminated (R235), a sample of the transmit power 20 dB down is generated at port C. Power is converted to voltage by RF detector diode CR200. As the coupler has a 50ohm output impedance and the diode has an input impedance of roughly ??, some serious matching has to occur. This is accomplished by C221, L212, and L225. This match is selected to provide more headroom for the power detect circuitry between "no power" and power level 7. Filtering is provided by C252. At this point we have a DC voltage which uniquely represents the PA's output power. This is used by two circuits, the power control loop and the RF power fail-safe monitor, which is described in the following section.

The output of the detector is presented to the power control error amplifier (U204) negative input through the lowpass filter of C249.

The error amplifier U204 uses its positive input from PA_LEVEL as a reference level and tries to swing its negative input to the same voltage by varying its output and thus the PA power gain. In this manner the control loop tries to keep the PA power constant to the value calibrated for each PA_LEVEL setting.

3.6.3.5.3 RF Fail-safe

The NRM must have a means of detecting when it is radiating power at the antenna, and must shut down if it detects transmission happening when it shouldn't be.

The output of the PA level detector (described above) is connected to a non-inverting input of U204 through the low pass filter of R235 and C234. The inverting input (U204-6) is a reference voltage generated by the precision resistors R263, R274. This voltage (725 mV) represents the level at the non-inverting input corresponding to no RF power. Any level present at the non-inverting input that is higher than this must be an indication of transmitter power being present. In this situation, the output of U114 will swing to TX_3V. This signal, RF_DET, is sent to the controller through the EMI filter.

RF_DET is sampled by the controller once every minute with the first 1-minute timer starting 10 seconds after the unit is powered up. If RF power is detected when it shouldn't be, a 150 ms timer is started and RF_DET is re-sampled at its expiry. This builds some hysteresis into the system to avoid false alarm glitches. If RF is still present, the controller immediately powers down the NRM.