Theory of Operation: Phaser RF Module (24-42507-01)
FCC ID:H9PPHASERMODULE

1. Purpose

The purpose of this document and the respective schematic is to provide a description of the detailed design of the Phaser RF module.

2. References

[1] Schematic: Phaser RF Module 17-42507-01

3. Overview

This document details the RF sections of the Phaser module. It is not intended to describe the in-depth details of component value selection and matching. Rather it is an overview of the radio architecture.

4. Module Interface

The interface to the module consists of eleven signals. Four are for various power enables. RF_VCC_ENB* enables power to the radio, RF_TXV_ENB* enables power to the transmitter output stage U308, RF_RXV_ENB* enables power to the receiver, and RF_/RXV_ENB* which enables power to U305 (the first transmitter stage). See the figure at the end of this document for a timing diagram of a transmit/receive session.

The next three, RF_SYNTH_DATA, RF_SYNTH_CLK, and RF_SYNTH_LATCH are used to serially program the frequency synthesizer on the radio. The synthesizer needs to be reprogrammed during each RF session because the PLL is used as a reference for both receive and transmit. Thus, it must change frequency by 10.7Mhz (the IF frequency) each time it switches between receive and transmit. For example, the synthesizer is programmed to 2402 MHz to transmit, after the data is transmitted the synthesizer is reprogrammed to 2412.7 MHz and set to receive to await an acknowledgment.

The next signal is RF_SYNTH_REF. The RF synthesizer needs a reference clock to generate its timing and synchronization. The reference clock frequency must be either a sine wave or square wave at 6.2Mhz ±22ppm. Setting the synthesizer's reference divide ratio to 62 allows the RF frequency to be resolved in 100 kHz steps (6.2 MHz/62 = 100 kHz). This will provide for the 10.7 MHz difference between TX and RX frequencies.

The next two lines are RF_RXD, and RF_TXD. These are the raw received data from the radio and the desired transmit data to the radio, respectively. They are connected to a UART channel of a microprocessor. The baud rate used on this channel is 48 kbps.

The last line is RF_CARR_SENS. This signal originates from a comparator on the radio's RSSI line. It provides an indication about a received RF signal's strength. It is used to alert the microprocessor that the receiver senses a strong carrier signal. So far this signal has not proved to be sensitive enough to be used reliably as an indicator of RF data.

5. Transmit Duty Cycle Limitations

Since the transmit output power of the Phaser module exceeds 0dBm (1 milliwatt), a duty-cycle limitation must be placed on the transmission of data. This is done to keep the average transmit power within FCC specifications. The maximum transmit duty cycle for the Phaser RF module is 30%. This means that the module cannot transmit more than 30ms out of every 100ms interval. The duty cycle is controlled inherently by setting a maximum data frame size. The software that generates a frame imposes a limit of 30ms in total length. After the transmission, the software delays 70ms minimum to guarantee the 30% duty cycle. During actual transmission, a raw bit rate of 48kbps is transmitted. The transmit data is connected directly to a UART.

6. Radio Section

The radio used in the Phaser design is based on the older Nomad (predecessor to Phaser) architecture, with many improvements. It is tuned for 50Kbps operation, using 81 1Mhz channels between 2.4GHz and 2.5GHz. Based on the standard single conversion super-heterodyne FM digital radio design, both the scanner and base contain transmit and receive sections designed to communicate half-duplex.

6.1 Transmit section

To produce the FM signal at the desired RF channel frequency, the output from a VCO is directly modulated with the transmit data. The VCO (U310), working in conjunction with the RF synthesizer (U307) and low pass filter U312 to form a PLL. In an attempt to lock the VCO to a certain phase and frequency, U307 provides an error voltage, which becomes the VCOADJ signal. Once locked, the output of the VCO is a constant frequency. This frequency (the carrier) is set by the microprocessor via the three serial control signals (RF_SYNTH_DATA, RF_SYNTH_CLK, and RF_SYNTH_LATCH). The transmit data arrives at comparator U309 via the RF_TXD signal. The comparator's output is directly coupled to the VCO error signal. Thus, as the data switches between 1 and 0, the frequency of the VCO shifts slightly around some middle frequency (the carrier). Note that if the data contained on RF_TXD contains too many consecutive 1's or 0's, the PLL will have time to correct and depth of modulation reduces to zero. Thus, the radio has certain limitations on the transmit data, discussed in the later section. Resistor R322 controls the amount of "pull" the transmit data has on the VCO, thus controlling the FM deviation (or modulation).

The VCO output is passed through two stages of RF amplifiers and enters the RF switch, U302. In transmit mode, this switch is set to pass the output signal through the filter FL301 and onto the antenna. The nominal output power is 8dBm, at the antenna connector.

6.2 Receive section

The incoming RF signal arrives at the antenna and passes through a band pass filter FL301. In receive mode, the RF signal passes through an RF switch and two stages of high gain RF amplifiers (U302, U303 & U304). Then it enters a mixer (U306) which down converts the signal to the IF frequency of 10.7Mhz. Note that the previously discussed VCO is used to mix with the incoming RF signal. Thus, the microprocessor sets the synthesizer (U307) to 10.7Mhz above the desired receive frequency. The IF signal then passes through FL302, a 10.7Mhz ceramic filter with a 3db bandwidth of 280Khz. Finally, the IF signal enters the FM demodulator (U311) which reduces the signal to baseband and feeds the data slicer (U309). The output signal of U309 is the received data. U312 is used to create a carrier sense signal, based

on the RSSI output from the FM demodulator chip. Its output thresholds at approximately –40dBm of input power (at the antenna). Note that if no RF energy is present at the tuned channel, the data slicer will operate near the noise floor. Thus, complete random garbage will pour out of the RF_RXD signal. As mentioned previously, the microprocessor must sift through all this garbage to find a valid transmit frame.

6.2.1 Power control

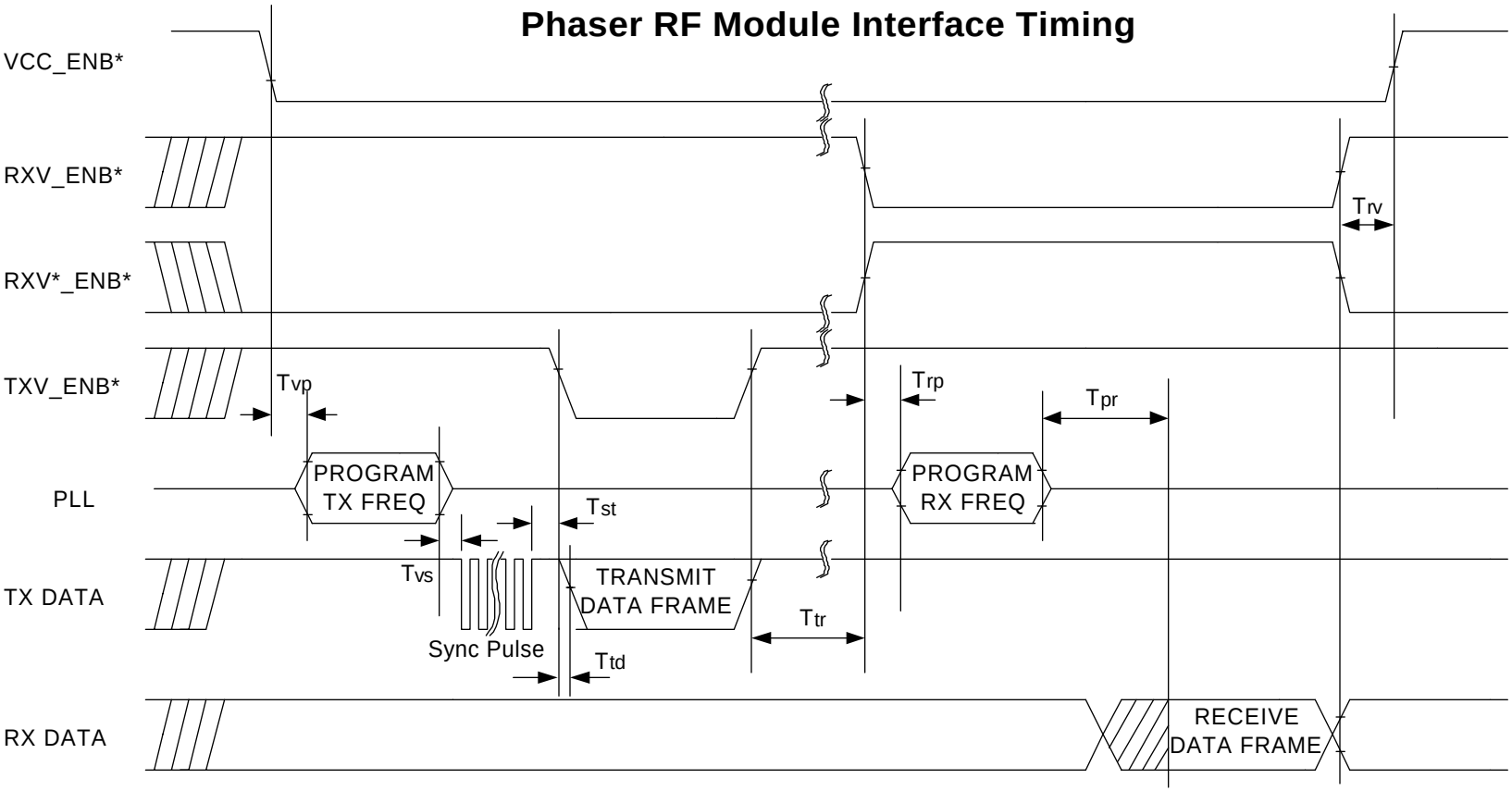
To conserve power, Vcc to the entire radio is controlled via the RF_VCC_ENB* signal. As shown in the schematic, this signal removes power to both receive and transmit sections by turning off Q302. Further, during normal operation, only the receiver or the transmitter may be on at once (half duplex). Thus, RF_RXV_ENB*, RF_/RXV_ENB* and RF_TXV_ENB* control MOSFETs which apply power to the respective sections of the circuitry. The TXV signal is the power for the transmitter output stage U308, RXV* powers the first TX stage U305, and the RXV signal is the power for all the receiver components.

U305 is turned on with RXV* to allow the VCO to lock before TXV is applied. Once TXV is applied the RF signal is output. If both TX stages were powered with TXV, garbage would be transmitted while the VCO was trying to lock. This would not only cause spurs, but also cut into our 30% duty cycle (30ms out of 100ms) allowable transmit window.

7. Antennas

The module uses an inverted-F type antenna for omnidirectional performance. The two attached figures show isometric and top views of the antenna. The grounding system for the antenna is simple. The two outer pins connect the PC board ground to the ground plane of the antenna. The center pin connects the radio to the antenna element. An insulator around this pin prevents shorting to the ground plane. The four tabs fit into slots on the PC board. These tabs serve to hold the antenna securely in place. The electrical connection is made through the three pins, which slide into “compliant” sockets in the PC board.

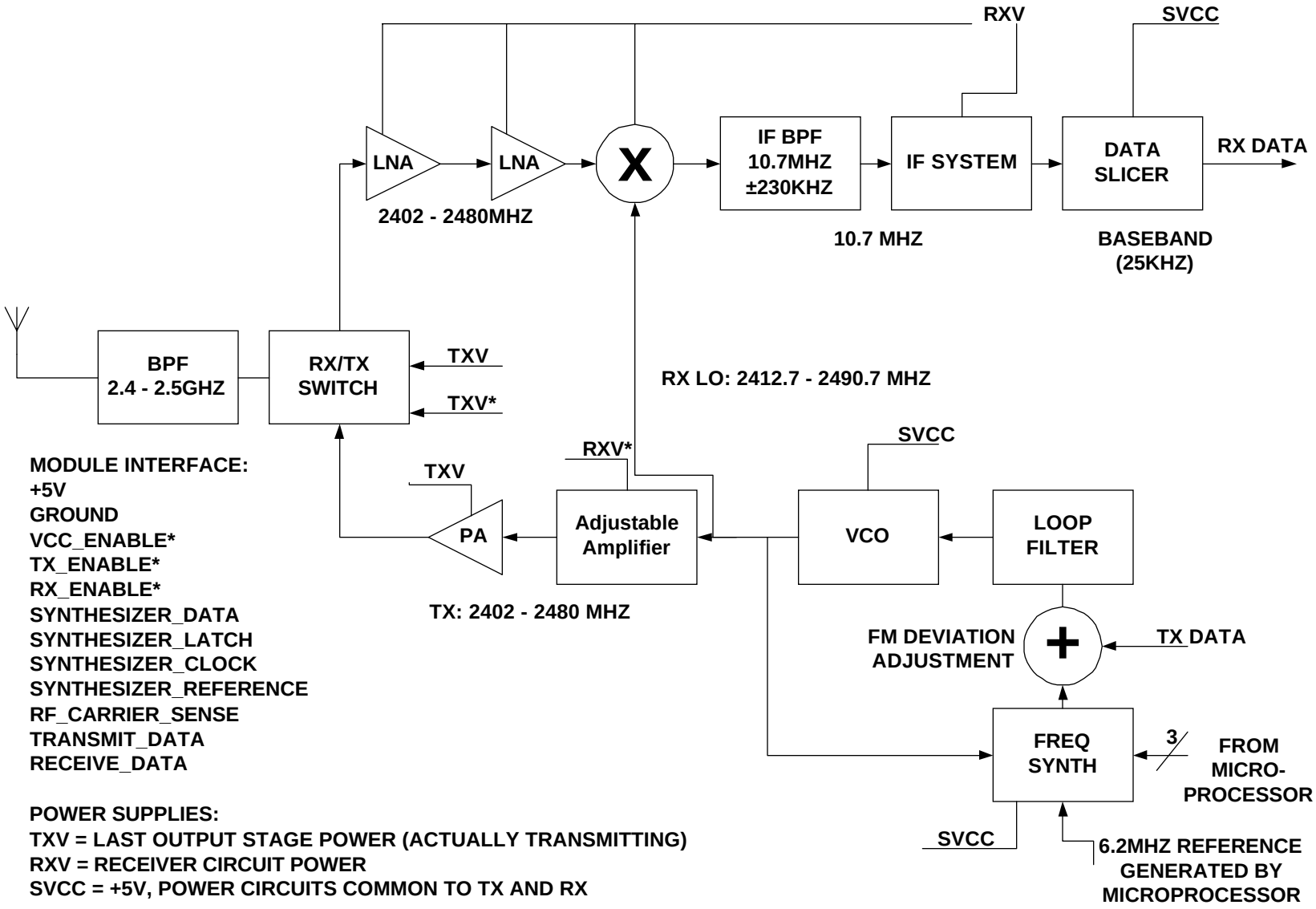
Phaser RF Module Interface Timing



Notes: 1) The PLL programming is performed via SYNTH_DATA, SYNTH_CLK and SYNTH_LATCH signals. Refer to LMX2315 datasheet.
2) The sync pulse must last at least **10ms** and must be a square wave with a period of 2 bit times (1 bit high, 1 bit low)
3) The RX DATA signal contains random noise when the receiver is enabled. Valid data will appear when a transmission is received.
4) Transmitted and received data must be generated at 48kbps and must be encoded using an algorithm designed by Symbol

T_{vp}: Vcc enable to PLL programming	1ms min
T_{vs}: End of PLL programming to beginning of sync waveform	75us min
T_{st}: End of sync waveform to beginning of transmit data	0ms max
T_{tr}: Completion of transmission to entering receive mode	1ms min
T_{rp}: Receive enable to beginning of PLL programming	0ms min
T_{pr}: End of PLL programming to valid receive data	6ms max
T_{rv}: End of receive mode to Vcc disable	0 ms min

SYMBOL TECHNOLOGIES
PHASER RF MODULE
24-42507-01



MODULE INTERFACE:
+5V
GROUND
VCC_ENABLE*
TX_ENABLE*
RX_ENABLE*
SYNTHESIZER_DATA
SYNTHESIZER_LATCH
SYNTHESIZER_CLOCK
SYNTHESIZER_REFERENCE
RF_CARRIER_SENSE
TRANSMIT_DATA
RECEIVE_DATA

POWER SUPPLIES:
TXV = LAST OUTPUT STAGE POWER (ACTUALLY TRANSMITTING)
RXV = RECEIVER CIRCUIT POWER
SVCC = +5V, POWER CIRCUITS COMMON TO TX AND RX