

## 2481.92MHz Printer Radio – Theory of Operation

### System Architecture:

The radio is a half duplex OOK-modulated (On/Off Keying) heterodyned transceiver operating over a narrow band centered at 2481.92MHz. Operating only as a portable device, its antenna and ground plane are internal to the unit and inaccessible to users. Major functional blocks are listed below and a block diagram of their interconnection follows.

A 1024MHz (doubled) synthesizer;

A hybrid 433.92MHz OOK-modulated transmitter;

A hybrid 433.92MHz OOK-demodulating receiver;

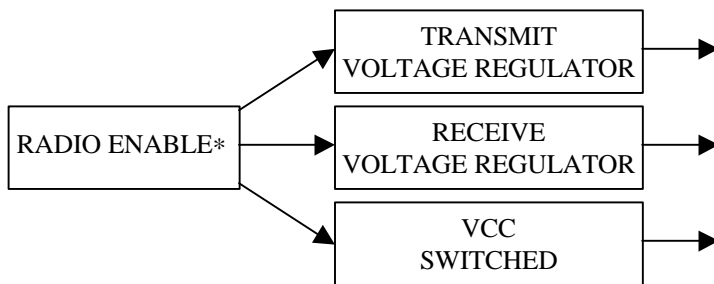
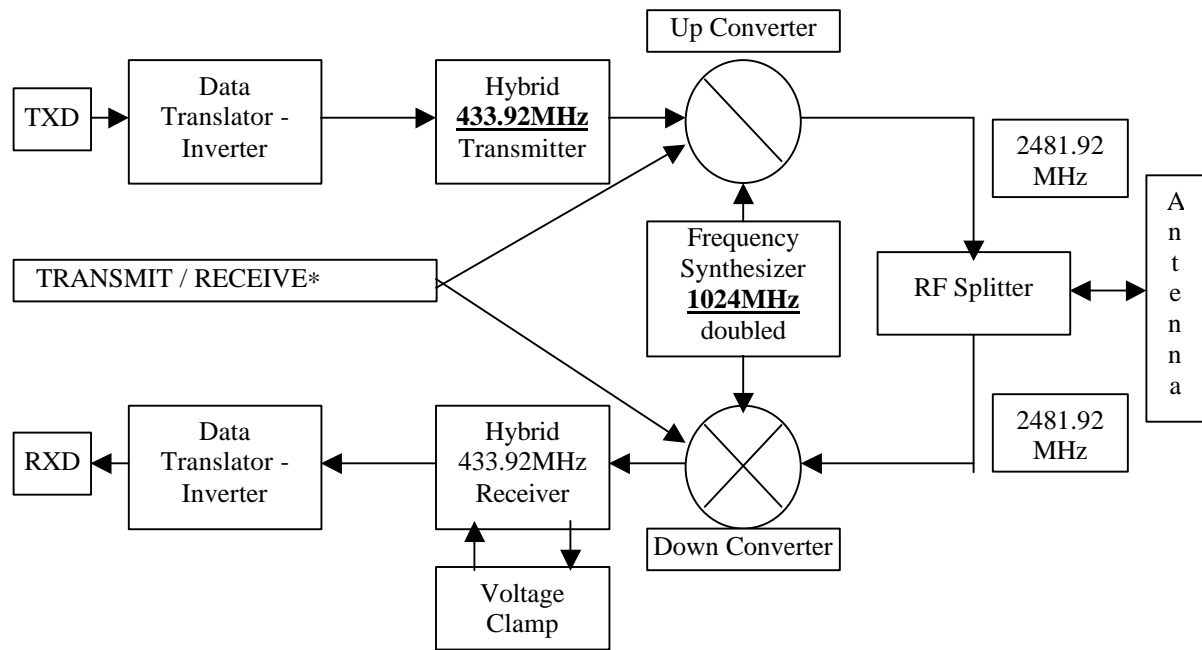
A voltage clamp circuit (proprietary to Symbol);

Up and down converters which implement the interface between the 2481.92MHz RF and the 433.92MHz hybrids;

An RF Splitter which connects the RF transmit and receive signal paths with the antenna;

Receive and transmit voltage regulators plus a voltage switch operating from a single 5V supply;

And miscellaneous control logic and data inverter/level translators.



\* Frequencies in the Block Diagram which are underlined and in bold typeface represent oscillators. There are no tunable sections in the transceiver.

## **Power Supplies, Control Logic and Data**

The Printer Radio board is provided with a single 5V supply. This supply in turn provides power for the Receive Data Translator–Inverter and the Transmit and Receive Voltage regulators, and is connected through a P-channel MOSFET switch to the VCC Switched supply rail. The Receive Regulator supplies 3V to the 433.92MHz Hybrid Receiver. The VCC Switched rail, at +5V, powers the Voltage Clamp and the MC12179 IC in the Synthesizer. The 4V Transmit regulator powers the remaining circuitry, which includes the Transmit Data Translator–Inverter, Hybrid Transmitter, Up & Down Converter, and the VCO portion of the Frequency Synthesizer.

Two control signals are supplied to the radio. The Radio Enable\* signal simply activates or de-activates the radio power supplies. The Transmit/Receive\* signal enables the Up Converter and disables the Down Converter in Transmit mode, and effects the reverse in Receive mode.

The TXD and RXD signals are serial data streams connected to a standard 8 data bit, one start bit, one stop bit asynchronous UART. Bit rates can vary up to 19.2KbpS.

## **Data Translator-Inverters**

These blocks are simple transistor circuits whose sole purpose is to provide logical signal inversion and a proper interface between the circuitry operating at different voltage levels at the DT-I inputs and outputs.

## **Hybrid 433.92MHz Transmitter**

This is a simple On/Off oscillator running at the indicated frequency and keyed by the transmit Data Translator/Inverter. The oscillator is SAW-based, and thus is stable with temperature.

## **1024MHz (doubled) Frequency Synthesizer**

The 1024MHz (doubled) synthesizer is a PLL whose active components are an MC12179 frequency synthesizer and the VCO amplifier portion of the HP MX5001 up/down converter. Major passive components include a 4MHz crystal used by the MC12179 to generate the reference frequency, an RC loop filter, and the VCO resonating components (capacitors, an inductor, and a varactor). The MC12179 contains the amplifier portion of the crystal oscillator, a divide by 256 counter, and a phase comparator. The buffered output of the 4MHz crystal oscillator drives one input of the phase comparator, whose other leg is driven by the divide by 256 counter. The counter is fed by the VCO which is running at 1024MHz. To close the loop, the phase comparator drives the varactor through the R-C loop filter so as to set the varactor capacitance to resonate with the inductor and remaining capacitors at 1024MHz. The VCO frequency is doubled internally by the MX5001 to produce a 2048MHz signal which is applied to that chip's mixer inputs.

## **Up Converter**

The Up Converter consists of one of the two mixers found in the HP MX5001 IC. Enabled by the Transmit/Receive\* control signal in transmit mode, the Up Converter mixes the outputs of the Frequency Synthesizer (doubled to 2048MHz) and the Transmitter Hybrid to produce a signal centered at 2481.92MHz. 2481.92MHz is the intentionally radiated frequency of this radio.

## **RF Splitter**

The job of the passive RF Splitter is to provide an interface between the antenna, the Up Converter output and the Down Converter input. This interface provides sufficient filtering to minimize out of band (2481.92MHz) energy both radiated by and received through the antenna.

### **Down Converter**

The Down Converter consists of one of the two mixers found in the HP MX5001 IC. Enabled by the Transmit/Receive\* control signal in the receive mode, the Down Converter mixes the output of the Frequency Synthesizer (doubled to 2048MHz) with the 2481.92MHz signal received by the antenna. The intentional output of the Down Converter is centered at 433.92MHz. This signal is passed on to the Hybrid 433.92MHz Receiver.

### **Hybrid 433.92MHz Receiver**

The Receiver is a homodyne. Manufactured by RF Monolithics, it incorporates a narrow band 433.92MHz SAW filter in its front end for RF selectivity. All of its pre-detector gain is provided at this frequency. Instability is precluded by a unique sampling design employing two cascaded and sequenced amplifiers. The first amplifier drives a SAW delay line and is turned on only for the time it takes a signal to propagate through the line. As the signal emerges from that line, the first amplifier is turned off and a second amplifier fed by the line is turned on. After the end of the sampled signal emerges from the second amplifier, that amplifier is turned off and the cycle repeats. Since the total amount of amplifier gain active at any one time is only the square root of the total gain provided, the ubiquitous stray parasitics are prevented from causing oscillation.

The remainder of the receiver design is unremarkable. The second RF amplifier drives a square law detector. The AC-coupled output of this detector is low pass filtered and eventually presented to a comparator, which slices the baseband signal and converts it to logic levels for the receive Data Translator-Inverter.

### **Voltage Clamp**

This circuit operates exclusively at baseband (under 100KHz) and is considered proprietary to Symbol Technologies.