**Processing Gain Calculation**
**Symbol Technologies LA-4121**
**WLAN PC Card**

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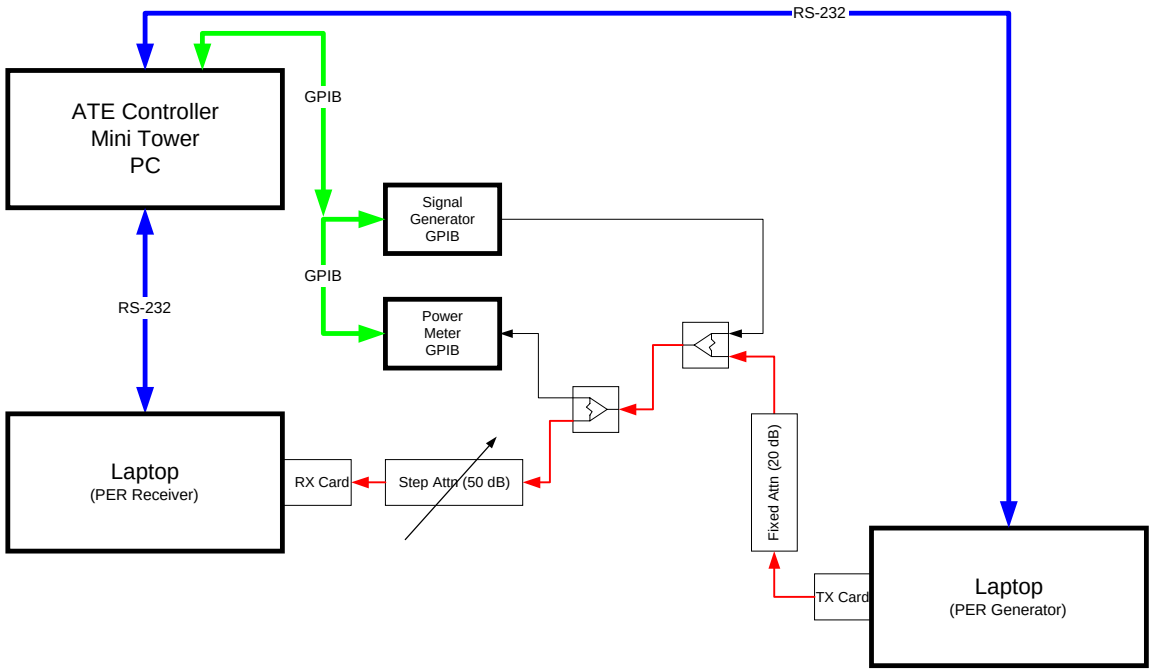
Symbol calculated the processing gain from the jamming margin of the LA-4121 transceiver as specified in 15.247 (e)(2).

## Test Setup

The purpose of the jamming test is to determine how effective the modulation, coding and decoding is at rejecting the corrupting influence of a CW jammer signal. Where as most setups us a BER to generate data and count errors because the modulator chip architecture prevents injecting data after chipping, Symbol chose to use another LA-4121 as the transmitter and data generator. A link between the transmitter and receiver is made and path loss adjusted so that the BER is 10E-5. The path loss is then reduced by 10 dB so that the BER approaches zero. Finally a jamming signal is combined with the transmitted signal to degrade the system performance. The jamming signal amplitude is then adjusted to the point that the BER is degraded to 10E-5.

The relationship between PER and BER is as follows. In order to get a good packet we need 8 x 1024 good bits. Stated mathematically. $1\text{-PER} = (1\text{-BER})^{(8*24)}$. Or $\text{BER}=1-(1-\text{PER})^{(1/(8*1024))}$.




**Jamming Margin Test Setup**

The major blocks of the jamming margin test are a transmitter, a receiver, and a jammer. The TX card formats and transmits packets of data consisting of 1024 bytes

each. The RX card then attempts to read each packet. The Signal Generator provides the jamming signal. The splitters combine the TX and jammer signals and provide a port to measure the power levels within the RF link. The PER Generator Laptop controls the transmit card and the PER receiver laptop controls the receiver. The ATE PC automates the test by controlling the two laptops, the Signal Generator, and the power meter.

**Software blocks**

The key to this test is three software programs Packet Generator (PG), Packet Counter (PC), and Jam Margin Controller (JMC). The first to work together to form the PER measurement system and the last to control the jammer, the power meter, and the other two software blocks.

Packet Generator runs on the PG Laptop and controls the transmit card. A trigger on the serial port line commands the TX card to generate and transmit 1000 packets of 1024 bytes at a specified data rate.

Packet Counter runs on the PER receiver laptop and queries the RX card for the number of packets it has received. A trigger on the serial port causes the Packet Counter to report the number of packets to the ATE Controller and reset the Packet Counter to zero. The Packet counter automatically detects the data rate of the incoming packet stream.

The other Jamming Margin Controller (JMC) runs on the ATE PC and controls the Signal Generator, the Power Meter, and PGAC running on the Dual Slot laptop.

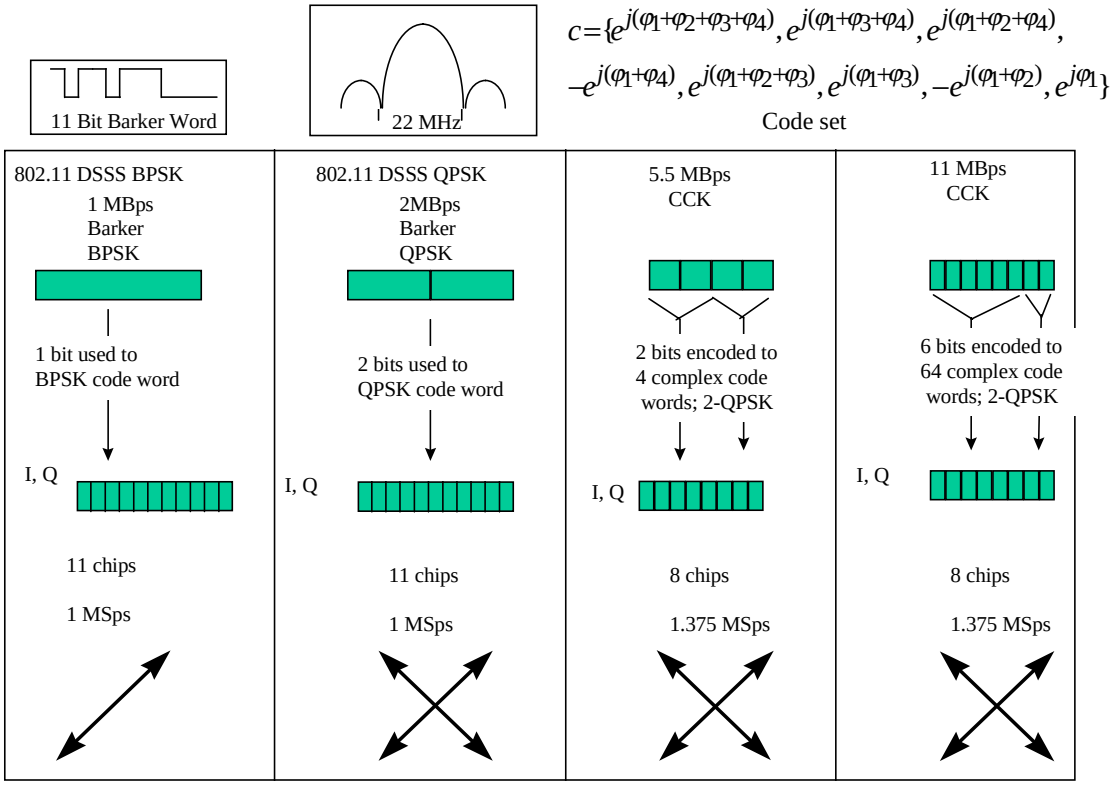
PG commands the TX card to transmit a set of 1000 packets of 1024 bytes of data. The RX card receives the packets and PC sends the number of good packets received to the serial port. The functional purpose is the same as a BER meter. A new set is run every time a new trigger is received on the serial port from JMC.

JMC controls the jammer, the power meter, and the Dual Slot program. JMC sets the frequency and level of the signal generator that acts as a jammer. JMC then sends a trigger to PG. The trigger causes PG to run another set of packets and PC reports the number of good packets back to JMC. The packet error rate is then converted to BER and JMC adjusts the Jammer level appropriately. A search algorithm is built into JMC to have the jammer converge to the right level for a 10E-5 BER. The jammer resolution is .1 dB.

When the jammer level causes a BER of 10E-5, the JMC program turns off the TX card and commands the power meter to read the jammer power level. JMC then turns off the jammer, turns on the TX card, and measures its power. Then S is offset for duty cycle and J/S is calculated from the two power measurements and recorded to disk. In this way as the test progresses and the TX card warms up power fluctuations due to temperature are referenced out.

The test is then repeated at the next jammer frequency. In this instance the test is conducted across the band of a single channel at 50KHz steps.

## Data Rate and Modulation Description




| Mode | Chip/Symbol |
|---|---|
| **1 MBps** | **11/1** |
| **2 MBps** | **11/2** |
| **5.5 MBps** | **8/2** |
| **11 MBps** | **8/8** |

## Gp Calculation from J/S data

Gp = $E_b/ N_0$ + J/S + $L_{sys}$ Where $L_{sys}$ <= 2 dB

| Mbps | $E_b/ N_0$ (dB) | Gp = J/S + |
|---|---|---|
| 1 | 10.6 | 12.6 |
| 2 | 10.6 | 12.6 |
| 5.5 | 15.6 | 17.6 |
| 11 | 16.6 | 18.6 |

**Test Results**

Attached are two plots of J/S and Gp vs F in MHz for 11 Mbps and 2 Mbps. The two plots are the worst case modes for each chipping rate. Theoretical calculations are given for the 1 and 5.5 Mbps modes.
The lower line shows the J/S as taken from the power ratios measured with the power meter. The upper line shows the processing gain $G_p$ as calculated from the Jamming Margin data. Note that the lowest 20% of the data points were discarded as specified in 15.247 (e)(2).

## Theoretical calculations

**1 Mbps mode using BPSK**

The processing gain is defined by:

PG = Wss/Rb1

Wss is the bandwidth (11.2 MHz min).
Rb is the data rate (1 Mbps)

PG = 11.2 MHz/1 Mbps
= 11.2
= 10Log10(11.2)
= 10.49 dB

**5.5 Mbps mode using CCK**

The processing gain is defined by:

PG = BW reduction + Coding Gain

BW reduction = Chip Rate / Symbol Rate

= 10Log10(11 MCps/1.375 MSps)
= 9.03 dB

Coding Gain
= 1.7 @ 11 Mbps
2.0 @ 5.5 Mbps

PG = 9.03 + 2.0
= 11.03 dB

[1] Simon Omura, Scholtz, and Levitt *Spread Spectrum Communications Handbook* (New York: McGraw Hill, 1994), p. 138

# Results Table

| Mode (Mbps) | Gp (dB) |
|---|---|
| 1 | 10.49 |
| 2 | 10.13 |
| 5.5 | 11.03 |
| 11 | 11.39 |

ead from JS File.vi
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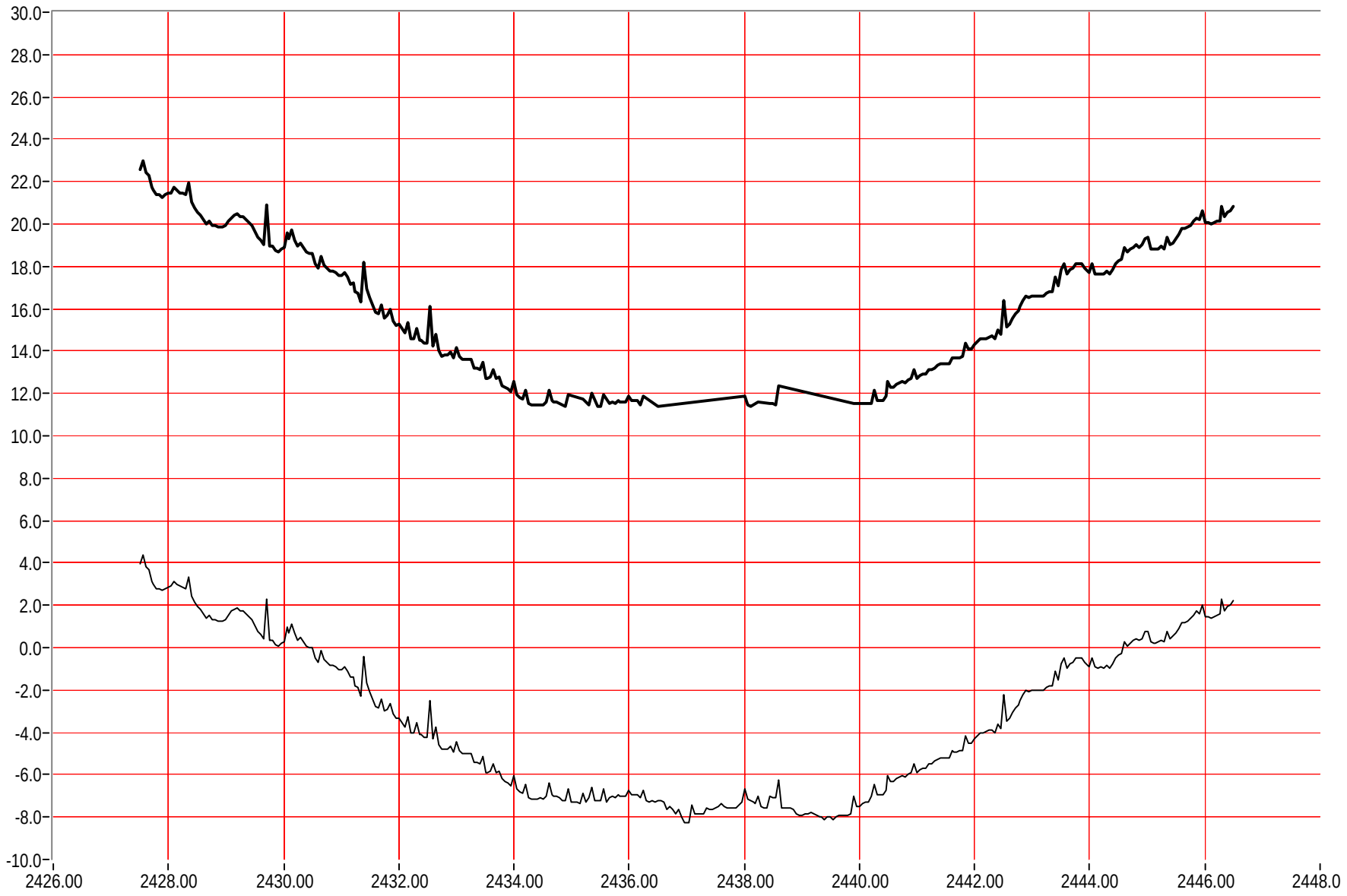
ast modified on 4/13/00 at 1:43 PM
rinted on 4/13/00 at 2:04 PM

File T2-11 Run 1 80 dB Attn.dat

# LA-4121 Processing Gain Plot: 11 Mbps




| | MHz | Gp |
|---|---|---|
| min value | 2434.90 | 11.39 |

Raw J/S
Gp

**Gp Offset** 18.60

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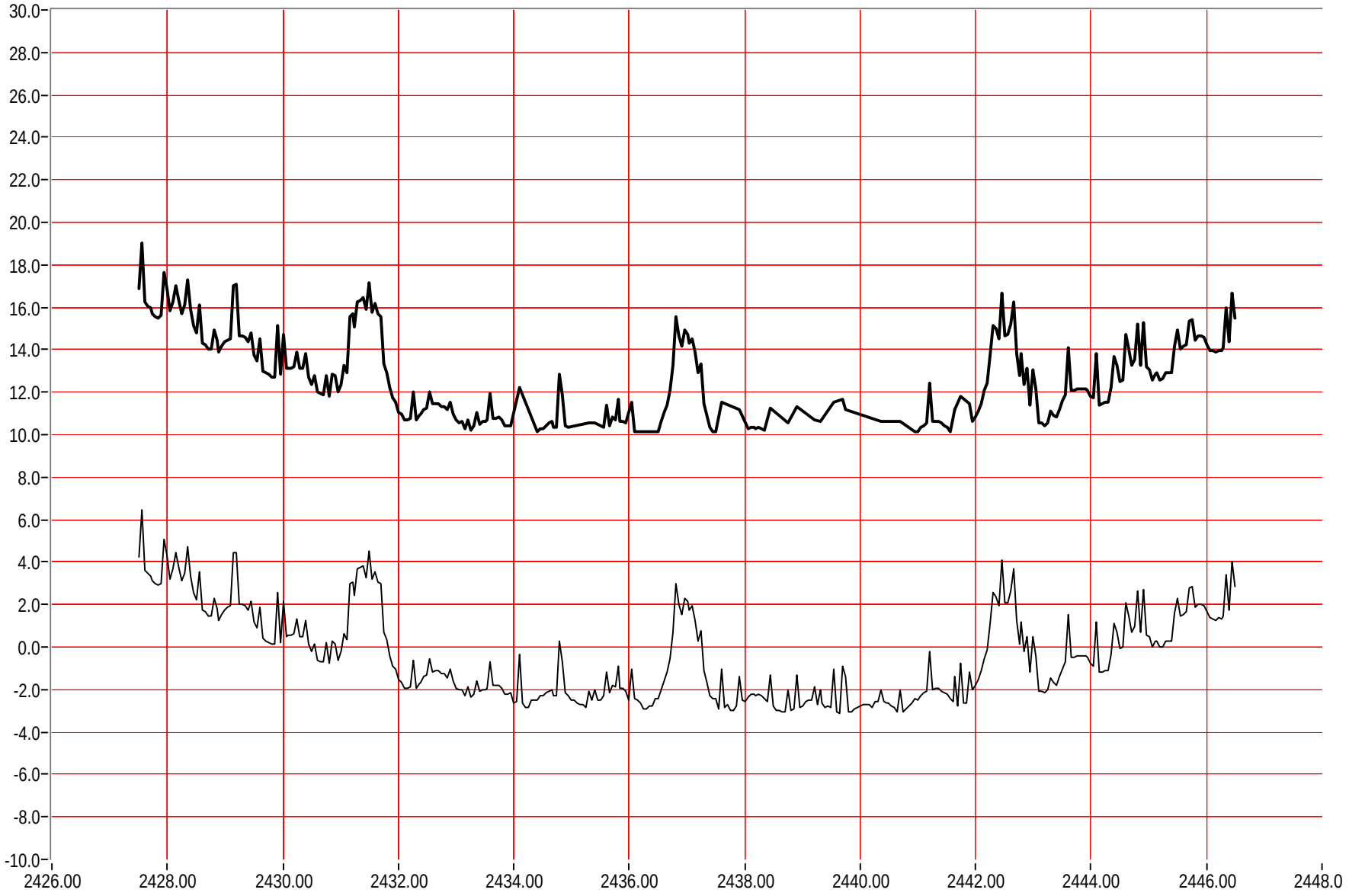
ast modified on 4/13/00 at 1:43 PM
rinted on 4/14/00 at 10:05 AM

File T2-2.dat

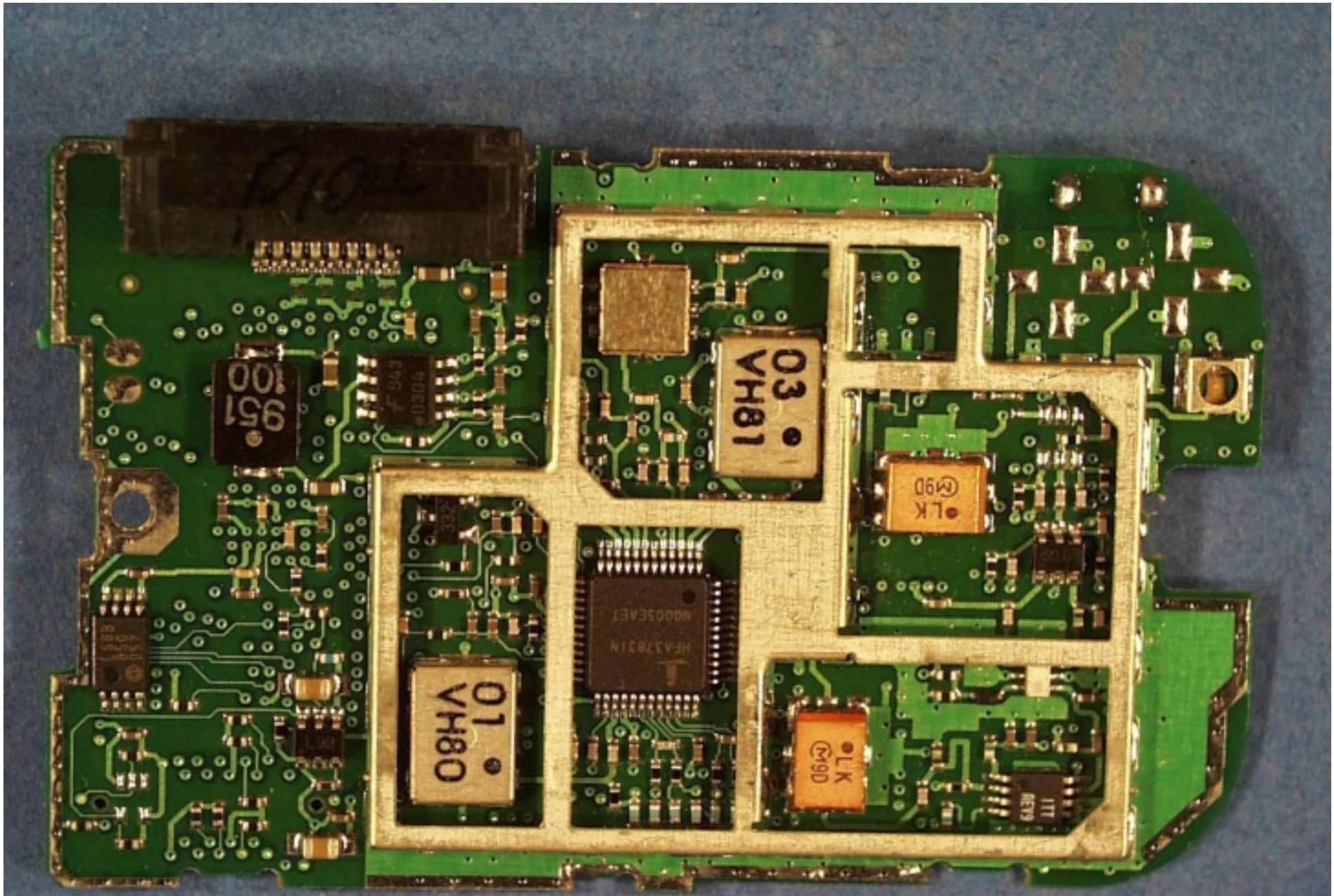
# LA-4121 Processing Gain Plot: 2 Mbps



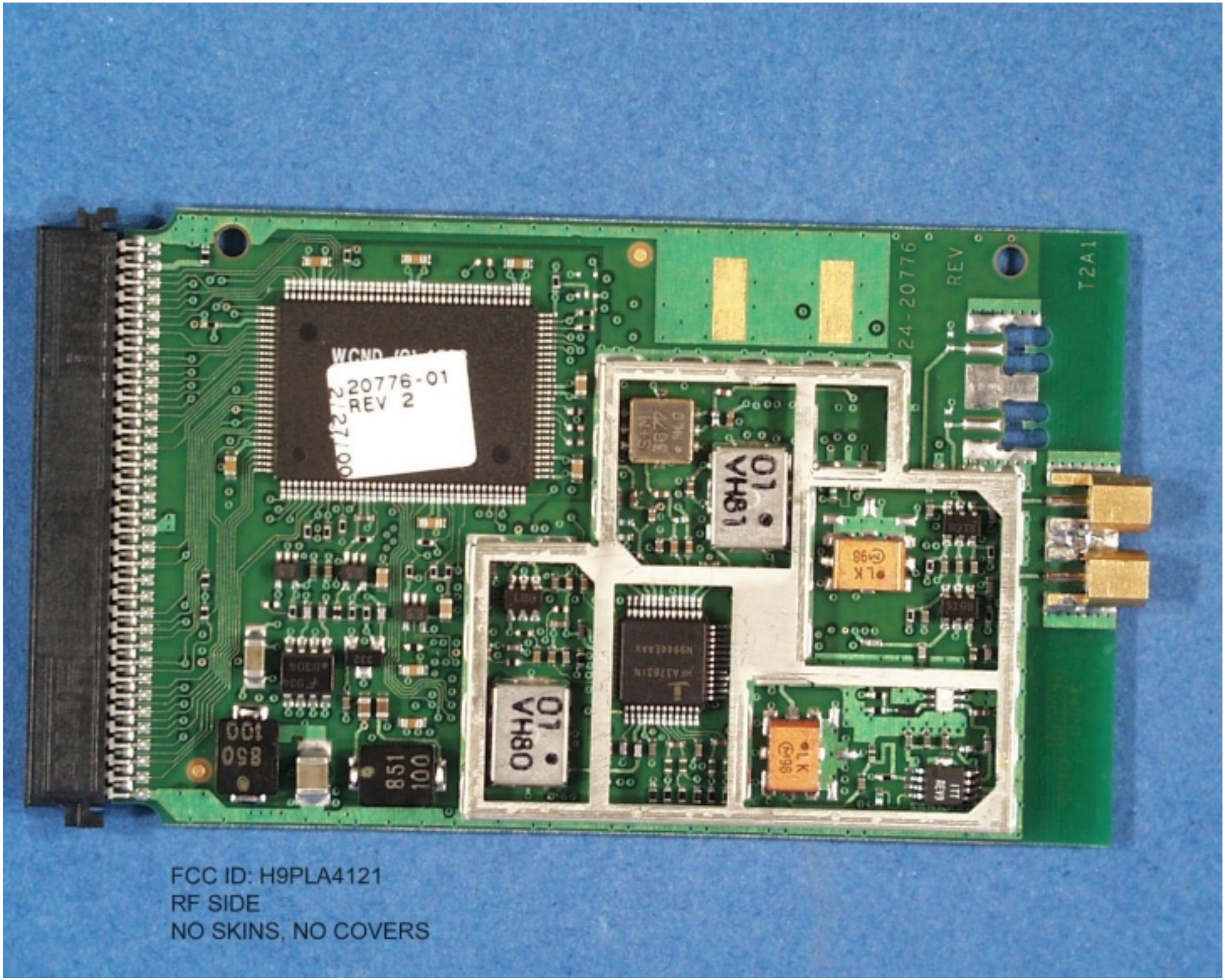

| | MHz | Gp |
|---|---|---|
| min value | 2441.00 | 10.13 |

Raw J/S
Gp

Gp Offset 12.60




DM4046
RF Side
Cover Removed
NP4046 Configuraton




FCC ID: H9PLA4121
RF SIDE
NO SKINS, NO COVERS