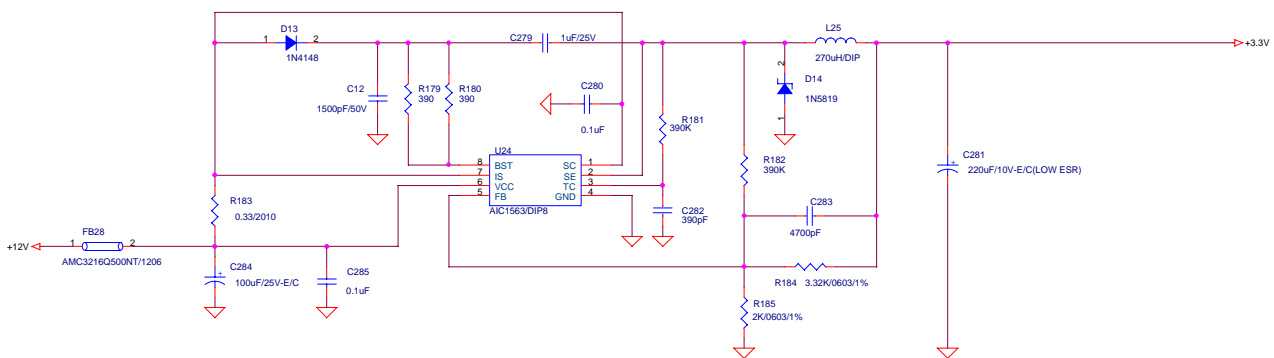
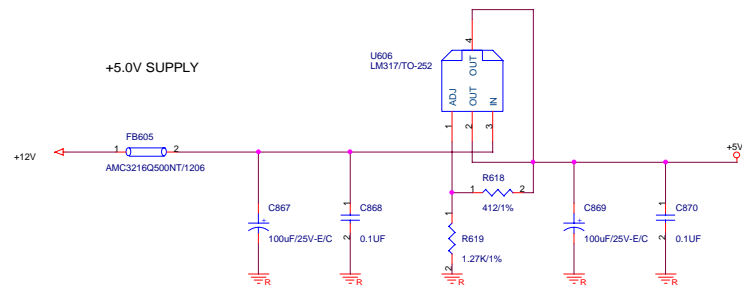
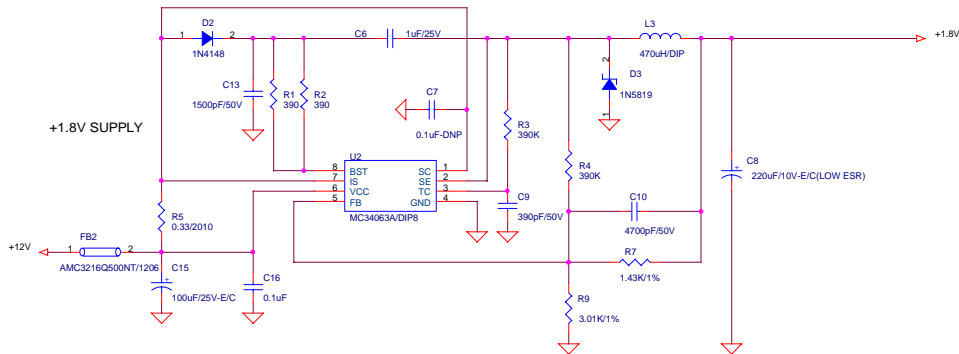
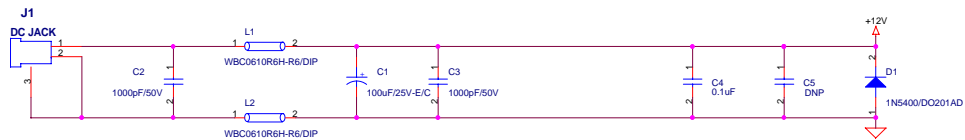
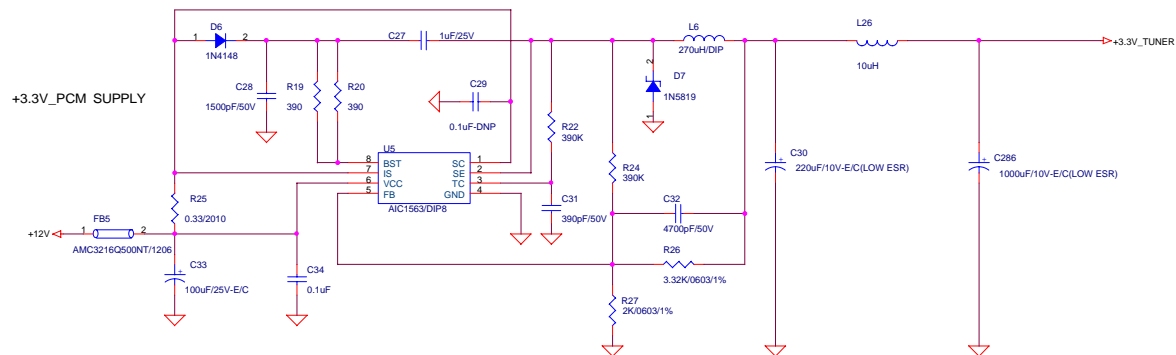
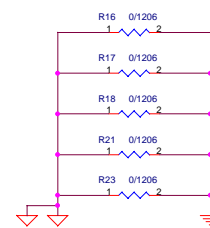


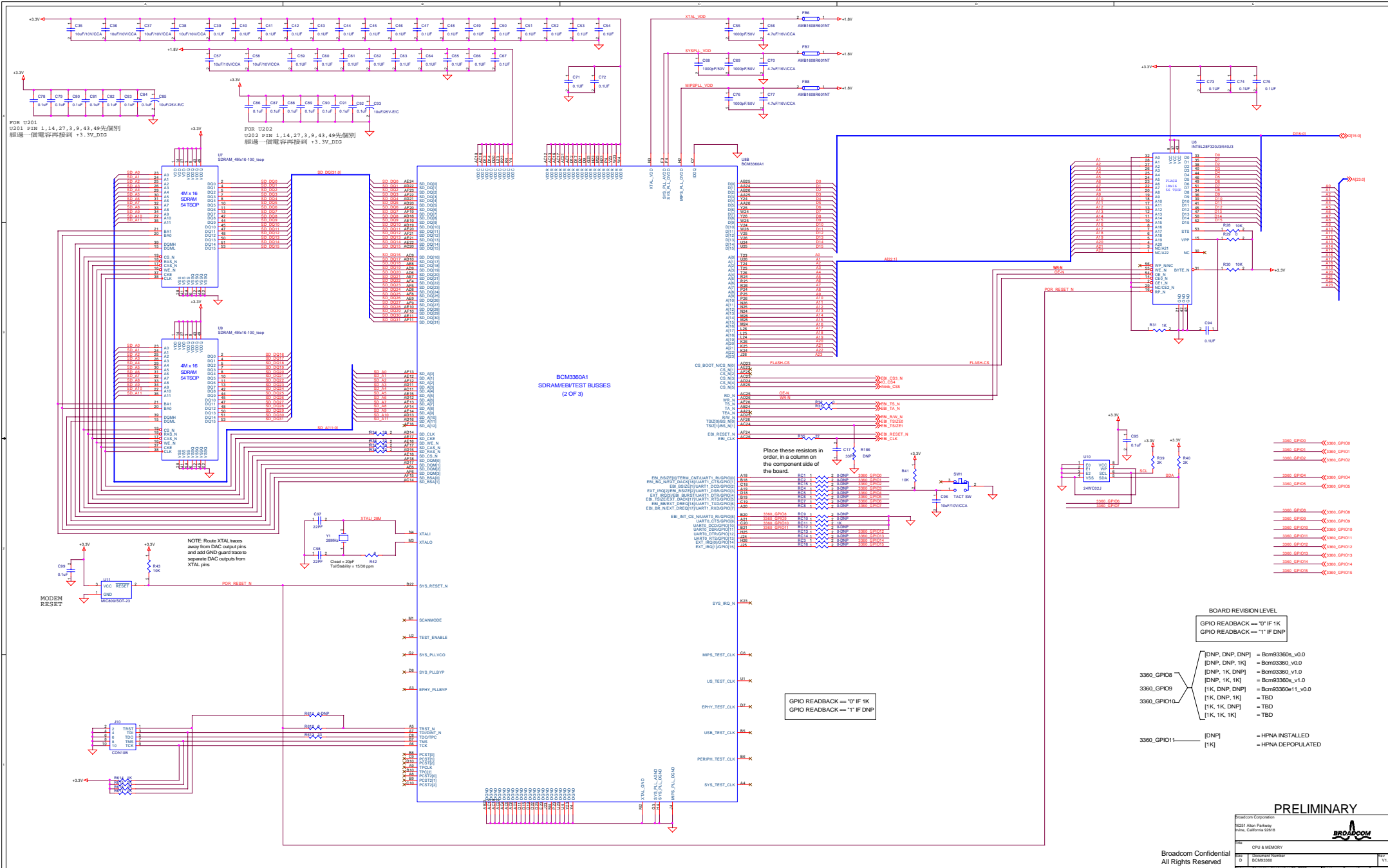
Locate power connector on rear panel as far from the diplexer as possible.



Straddle these resistors across the GND plane cutout between the RF and DIGITAL areas of the board.



Title		Power
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C	CME090	3
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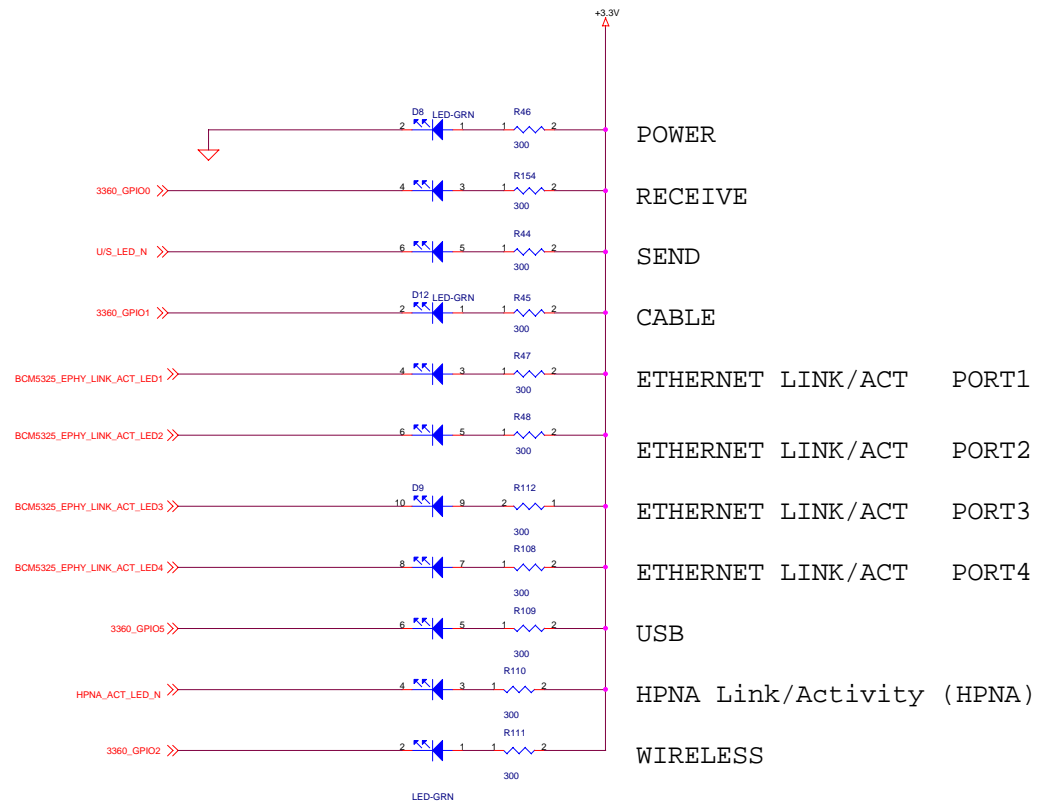
PRELIMINARY

Custom Configuration
 5251 Allen Parkway
 Irvine, California 92618



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POWER

RECEIVE

SEND

CABLE

ETHERNET LINK/ACT PORT1

ETHERNET LINK/ACT PORT2

ETHERNET LINK/ACT PORT3

ETHERNET LINK/ACT PORT4

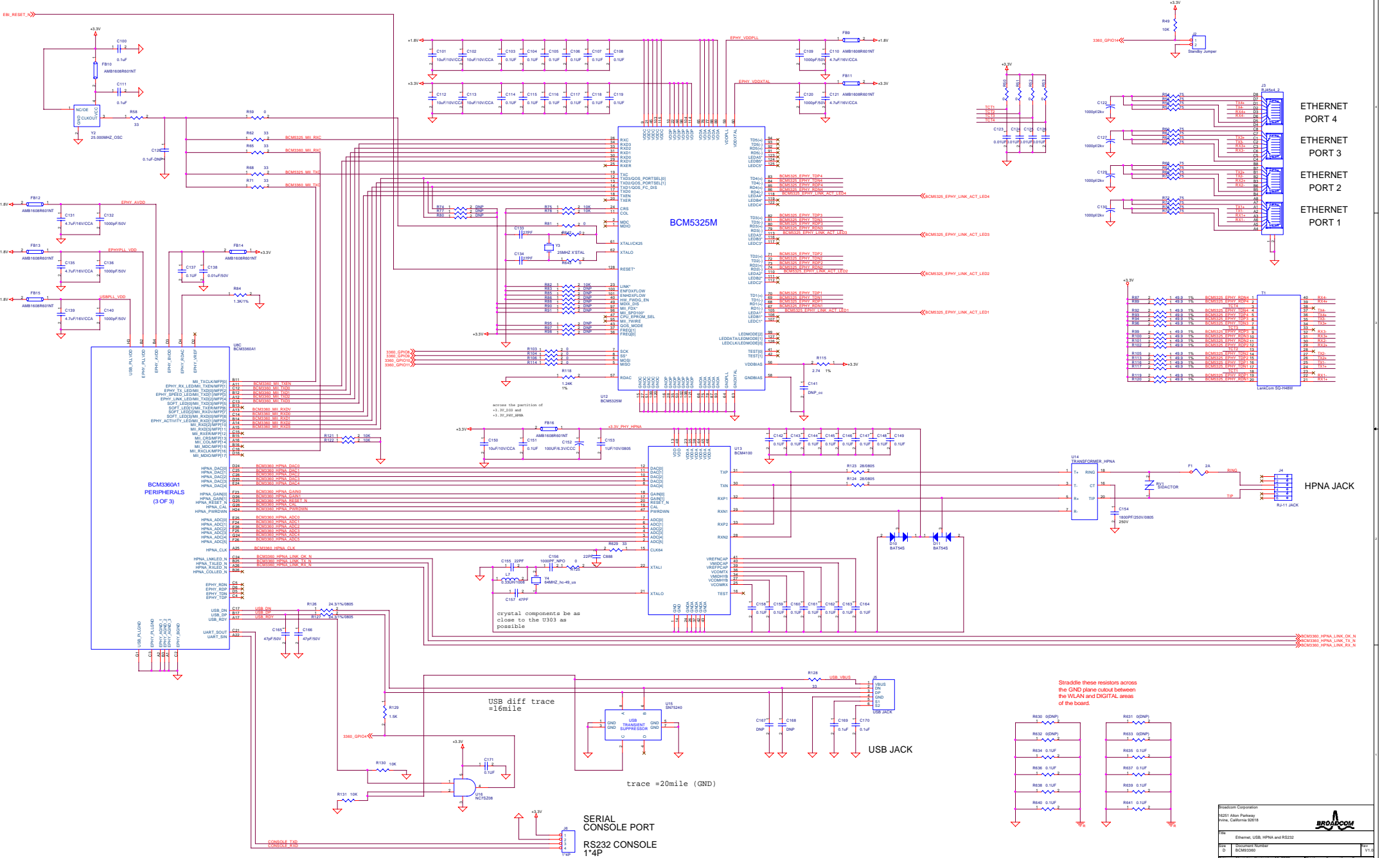
USB

HPNA Link/Activity (HPNA)

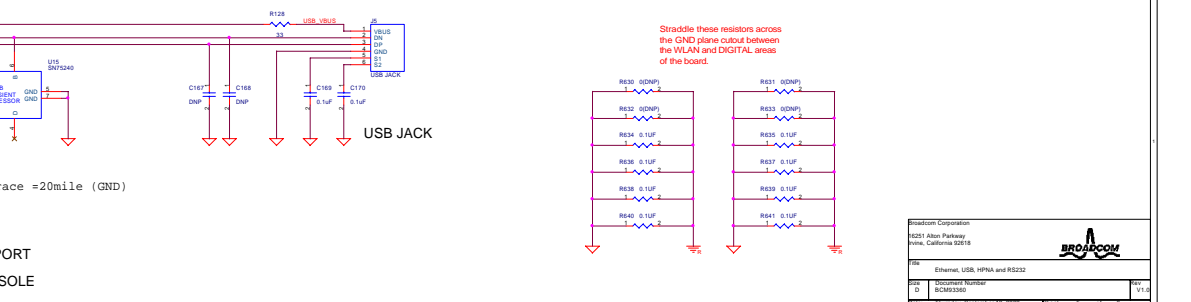
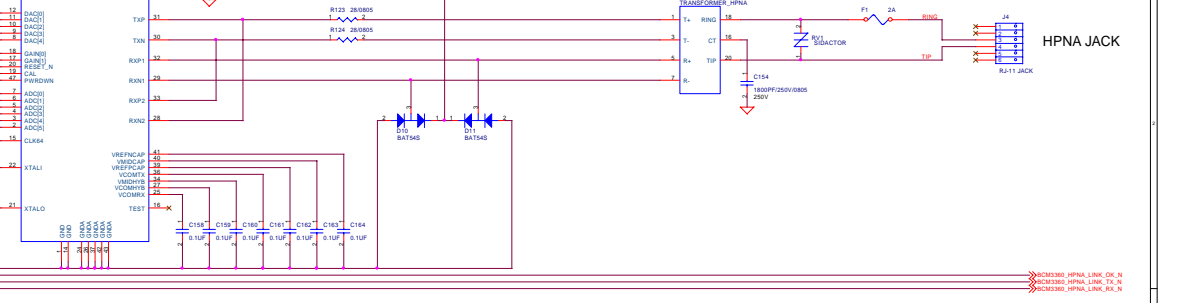
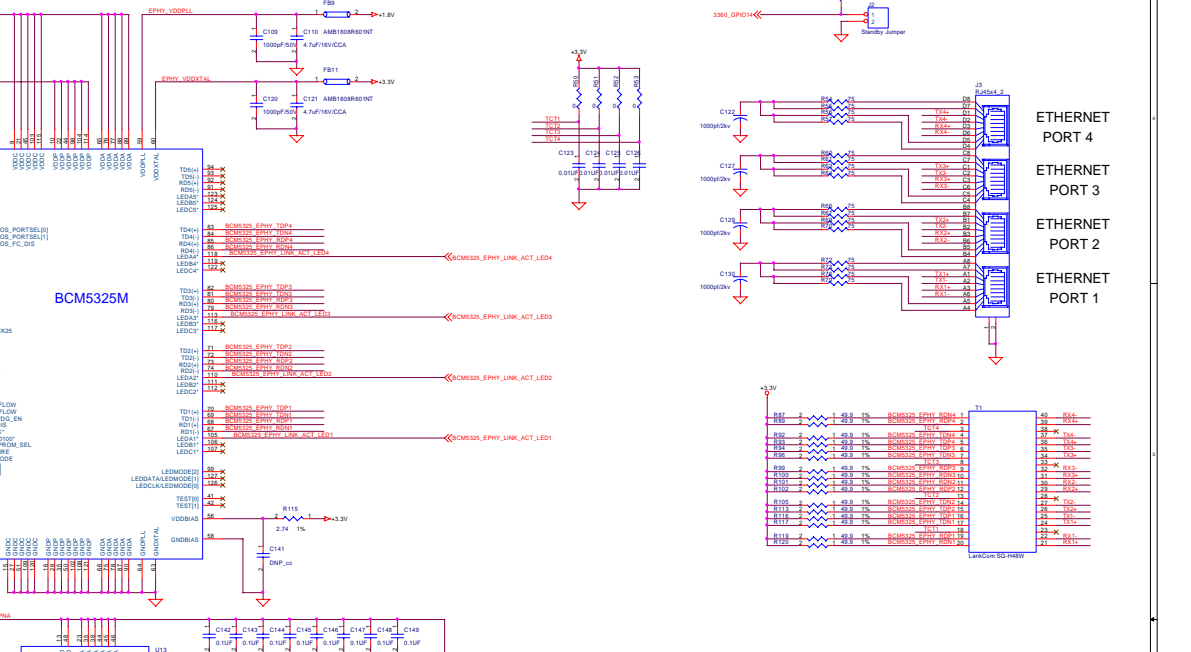
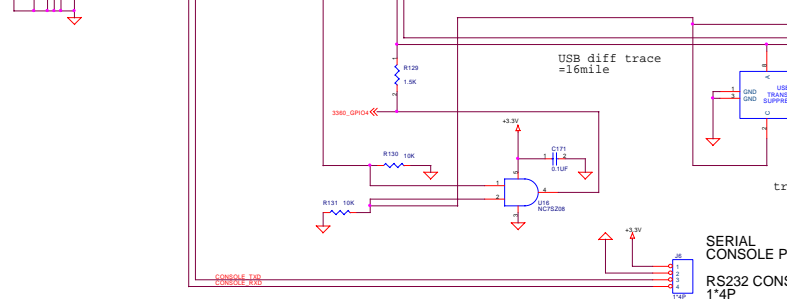
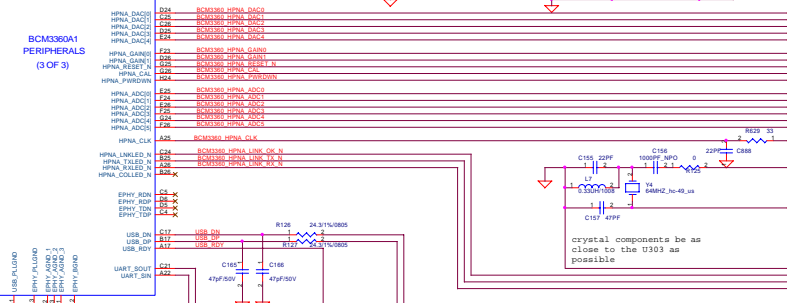
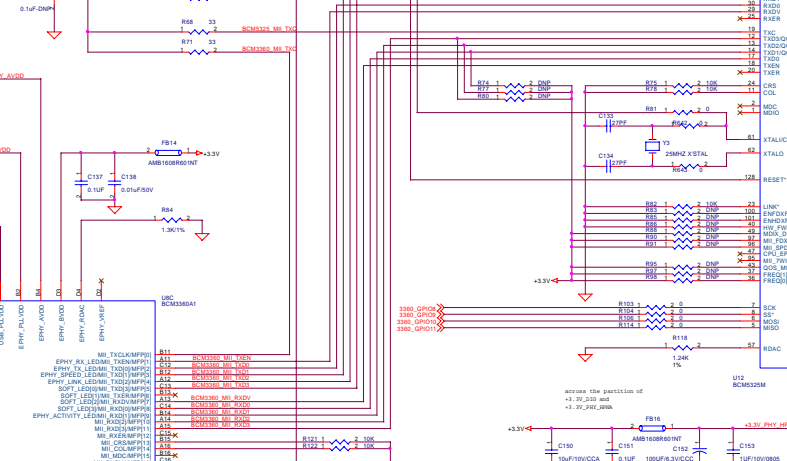
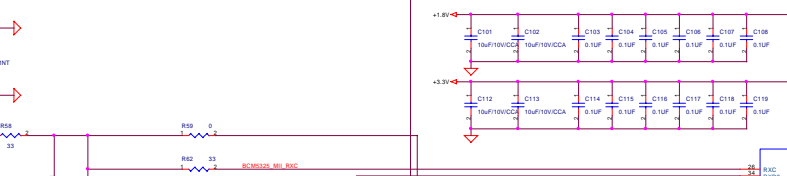
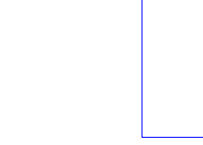
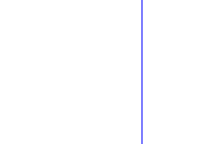
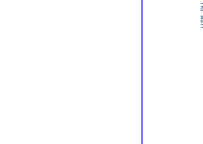
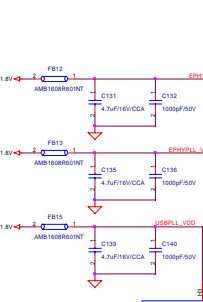
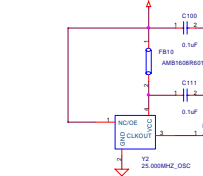
WIRELESS

PRELIMINARY

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Title	LED's	
Size	Document Number	Rev
C	BCM93345	V0.0
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EB_RESET

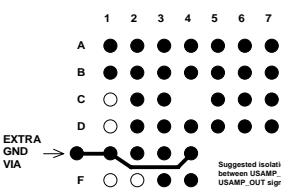
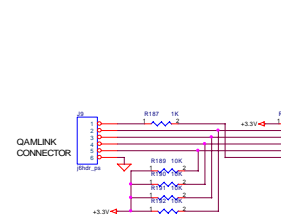
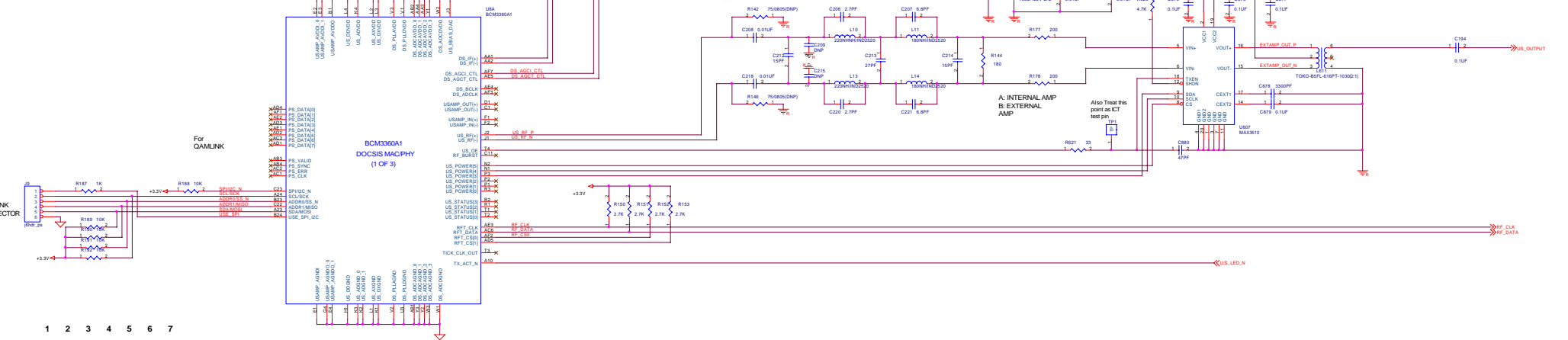
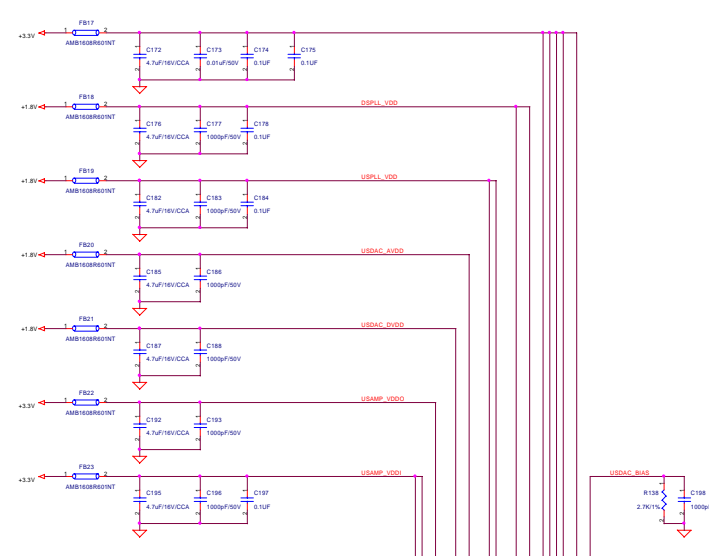


ETHERNET PORT 4
ETHERNET PORT 3
ETHERNET PORT 2
ETHERNET PORT 1

HPNA JACK

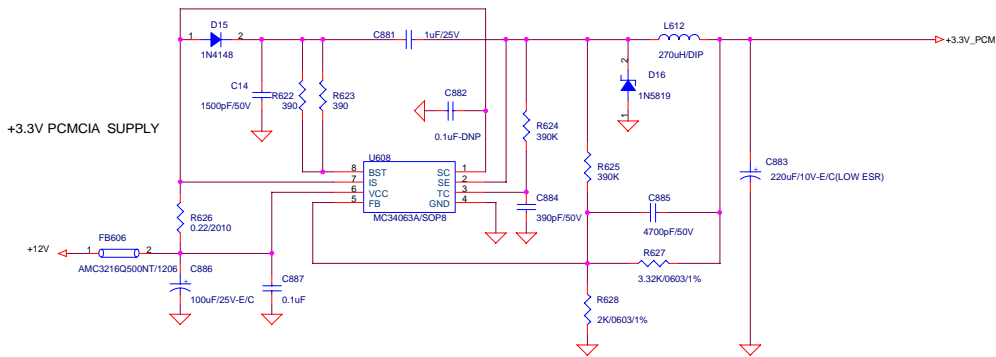
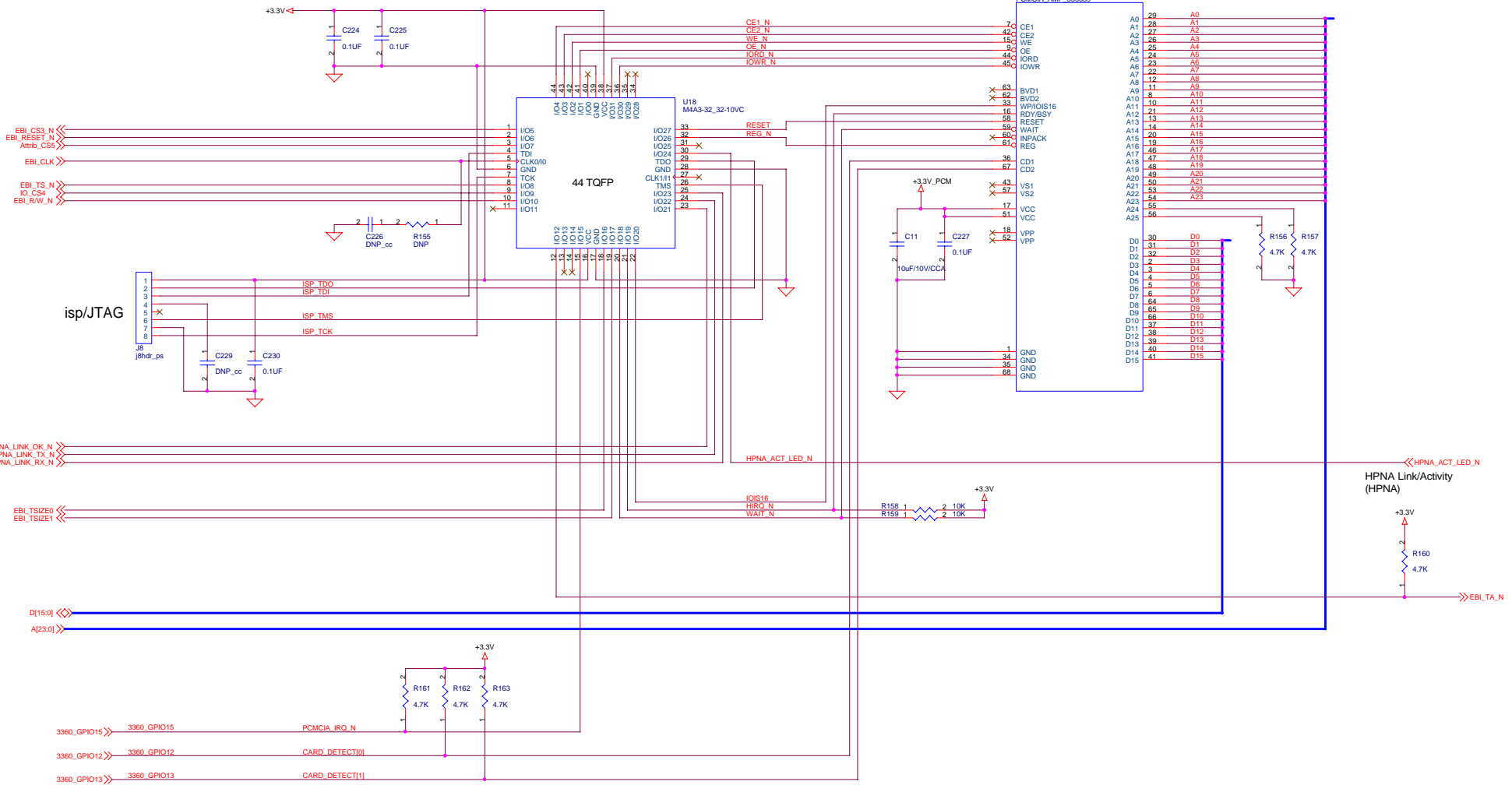
USB JACK

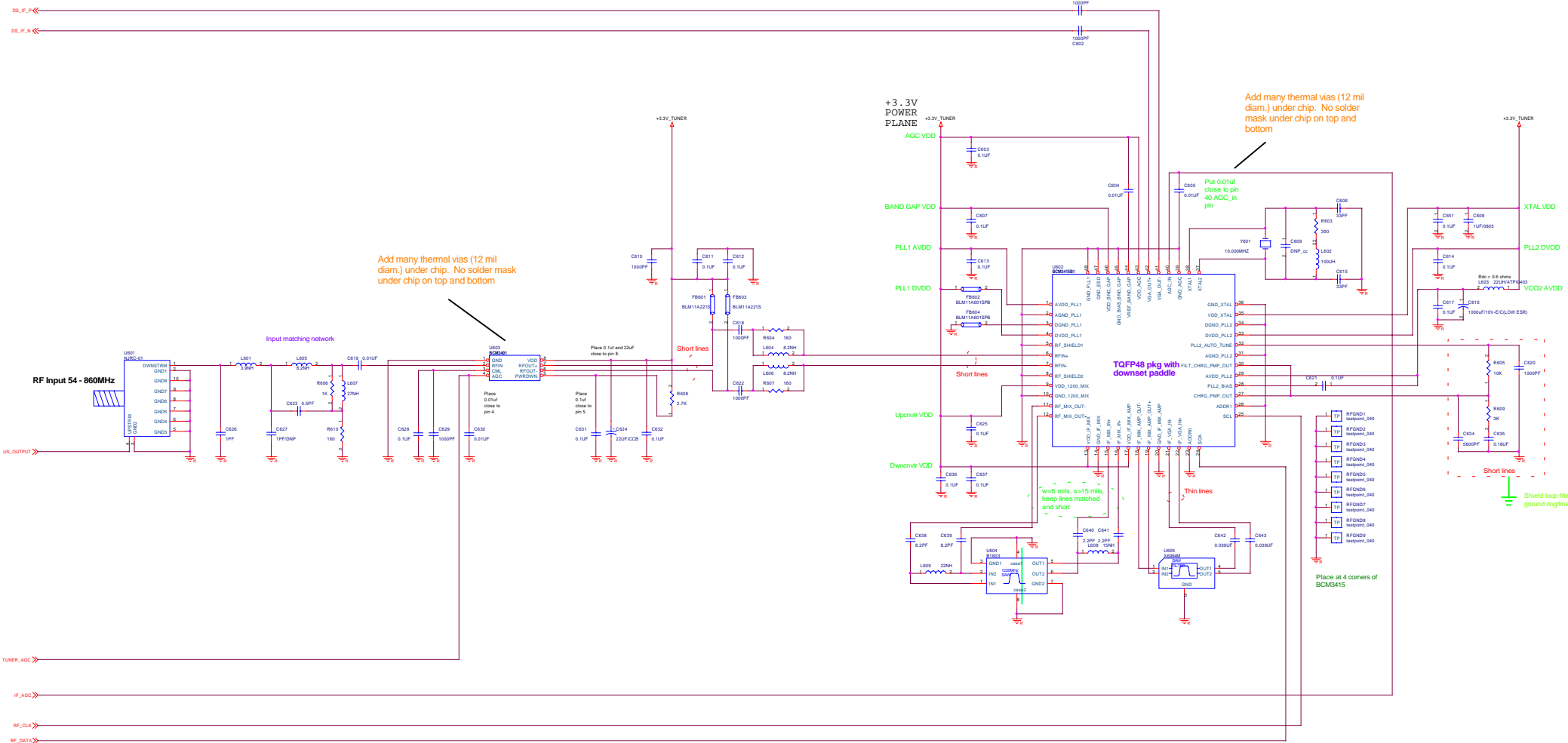
SERIAL CONSOLE PORT
RS232 CONSOLE
1*4P



EXTRA GND VIA →

Suggested isolation between USAMP_IN and USAMP_OUT signals.





DS_IF_P <<
DS_IF_A <<

US_OUTPUT >

TUNER_AGC >

IF_AGC >

RF_CLK >

RF_DATA >

Add many thermal vias (12 mil diam.) under chip. No solder mask under chip on top and bottom

Add many thermal vias (12 mil diam.) under chip. No solder mask under chip on top and bottom

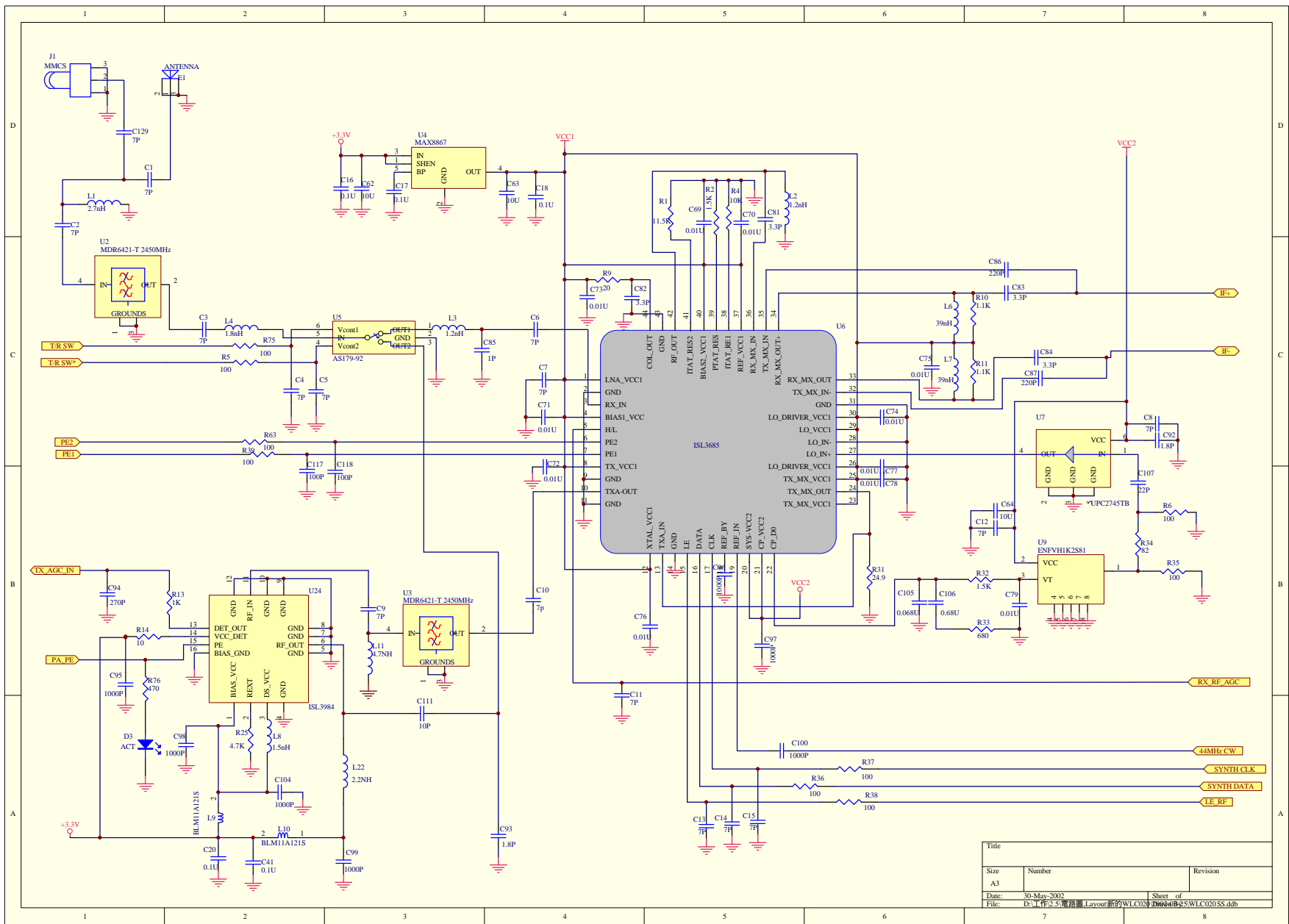
Put 0.01uF close to pin 40 AGC_in pin1

w=5 mils, s>=15 mils. Keep lines matched and short

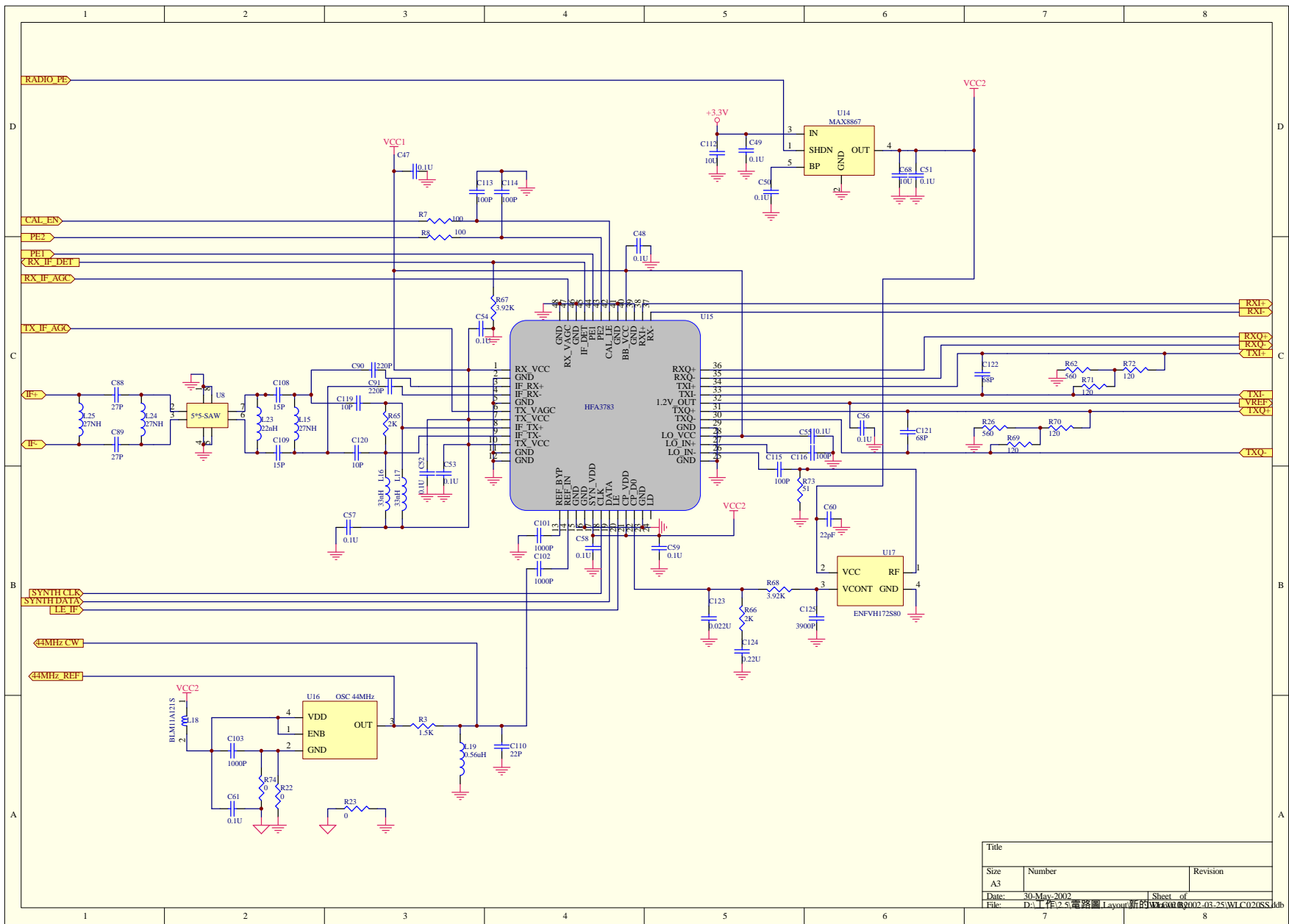
Place at 4 corners of BCM3415

Shield loop filter with ground ringlines

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ID	<Docment Number>	
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Size	Number	Revision
A3		
Date:	30-May-2002	Sheet of
File:	D:\工作区\电路\Layout新的\WLC020\06040B45\WLC020SS.ddb	06040B45



Title		
Size	Number	Revision
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Date:	30-May-2002	Sheet of
File:	D:\工作\2.5\電路圖 Layout\新的\W6600R002-03-25\WI C020SS.ktb	

