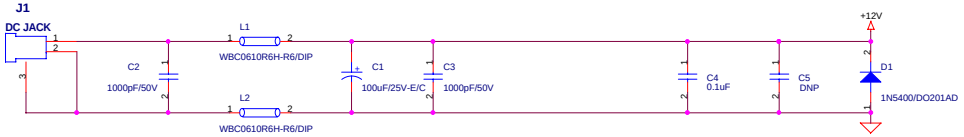
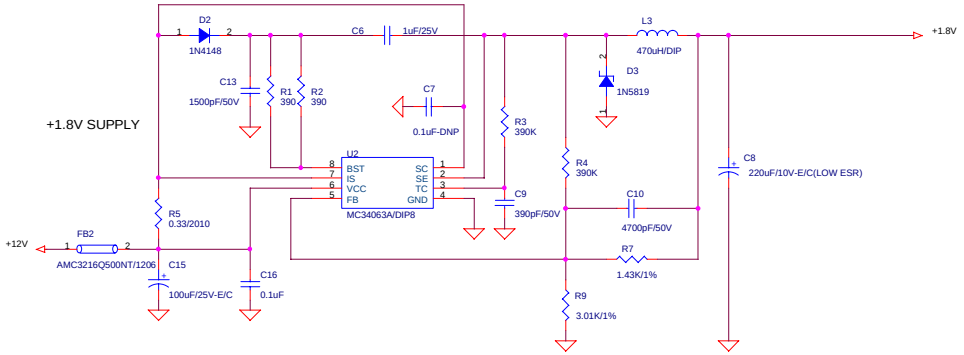
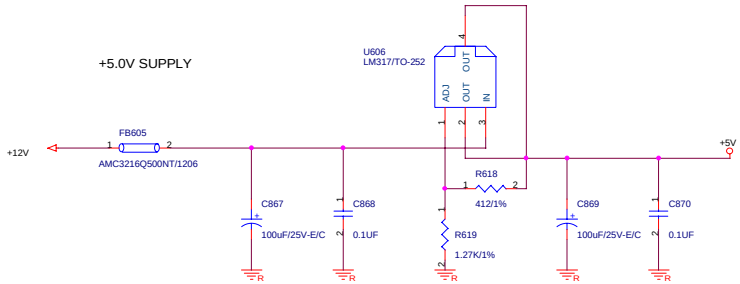
Locate power connector on rear panel as far from the diplexer as possible.

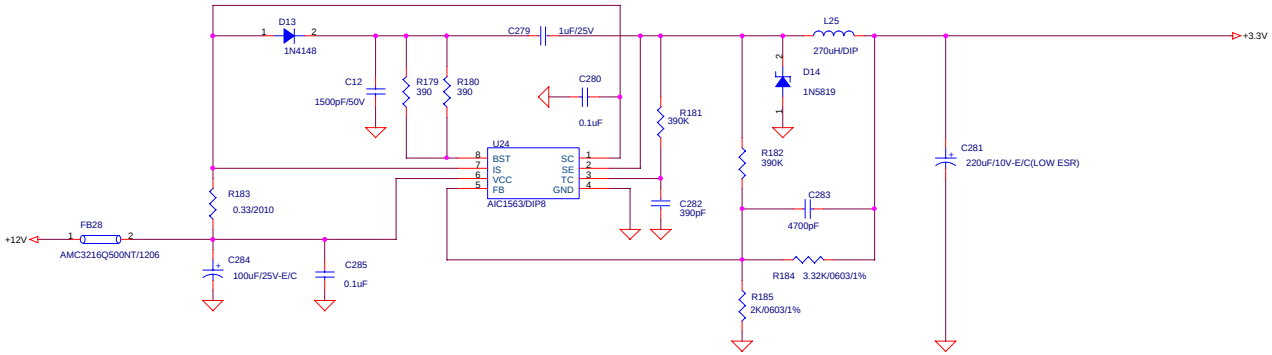


+1.8V SUPPLY

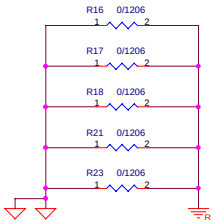


+5.0V SUPPLY

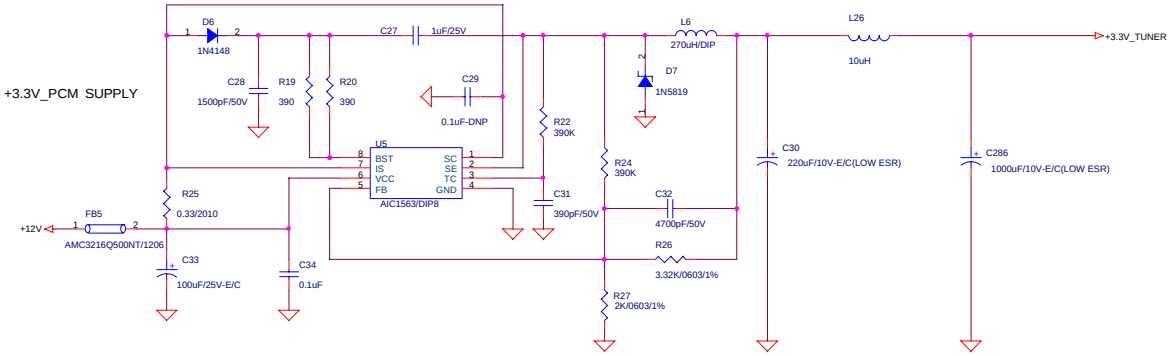




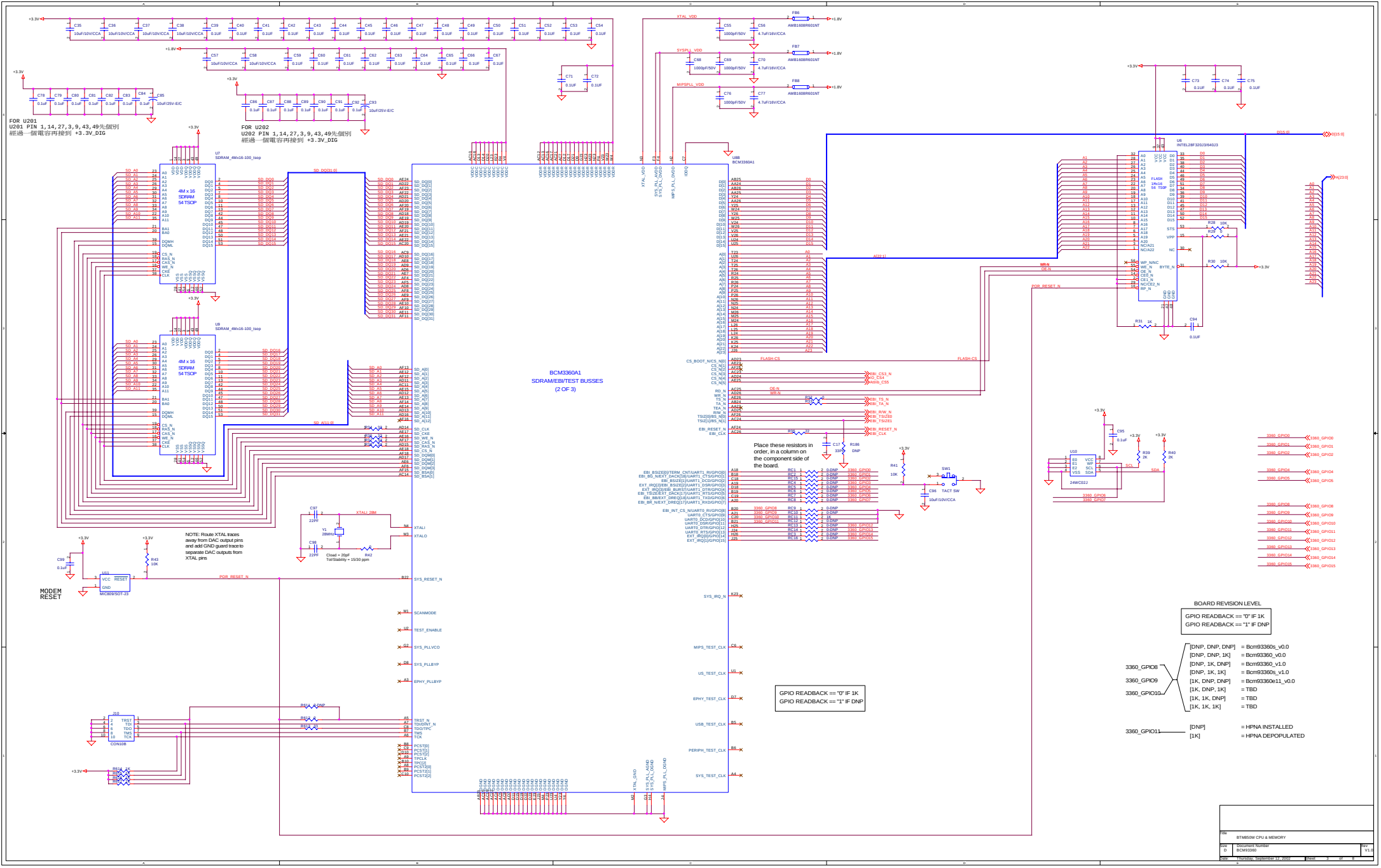
Straddle these resistors across the GND plane cutout between the RF and DIGITAL areas of the board.

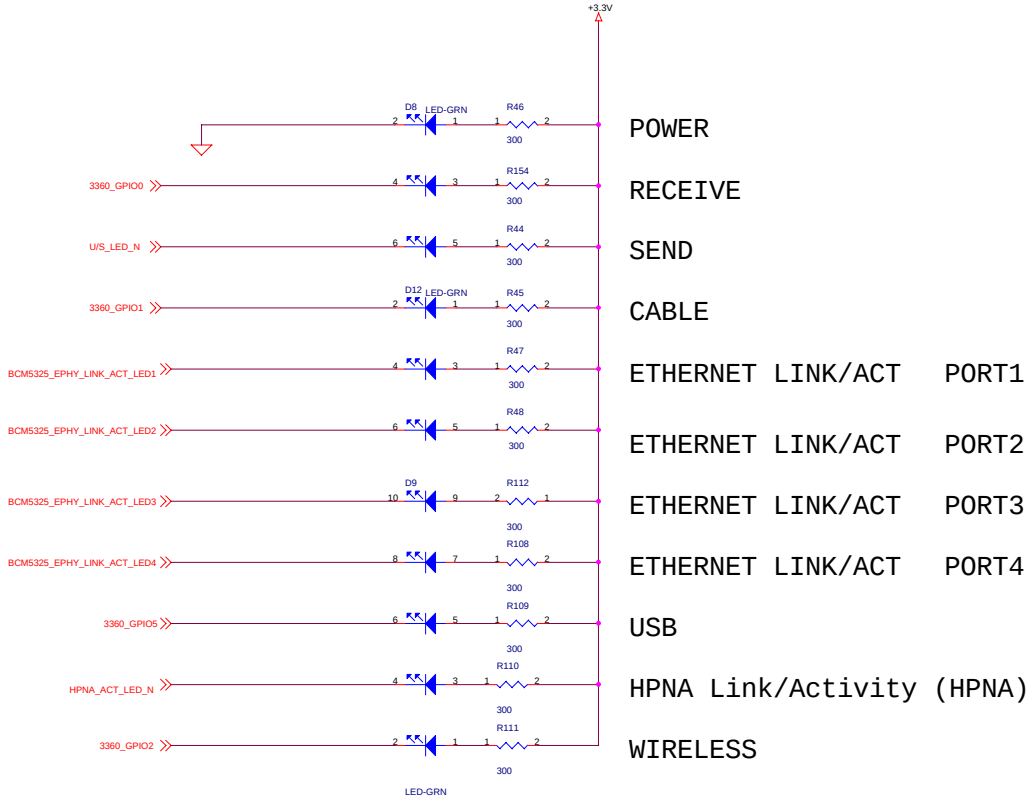


+3.3V_PCM SUPPLY

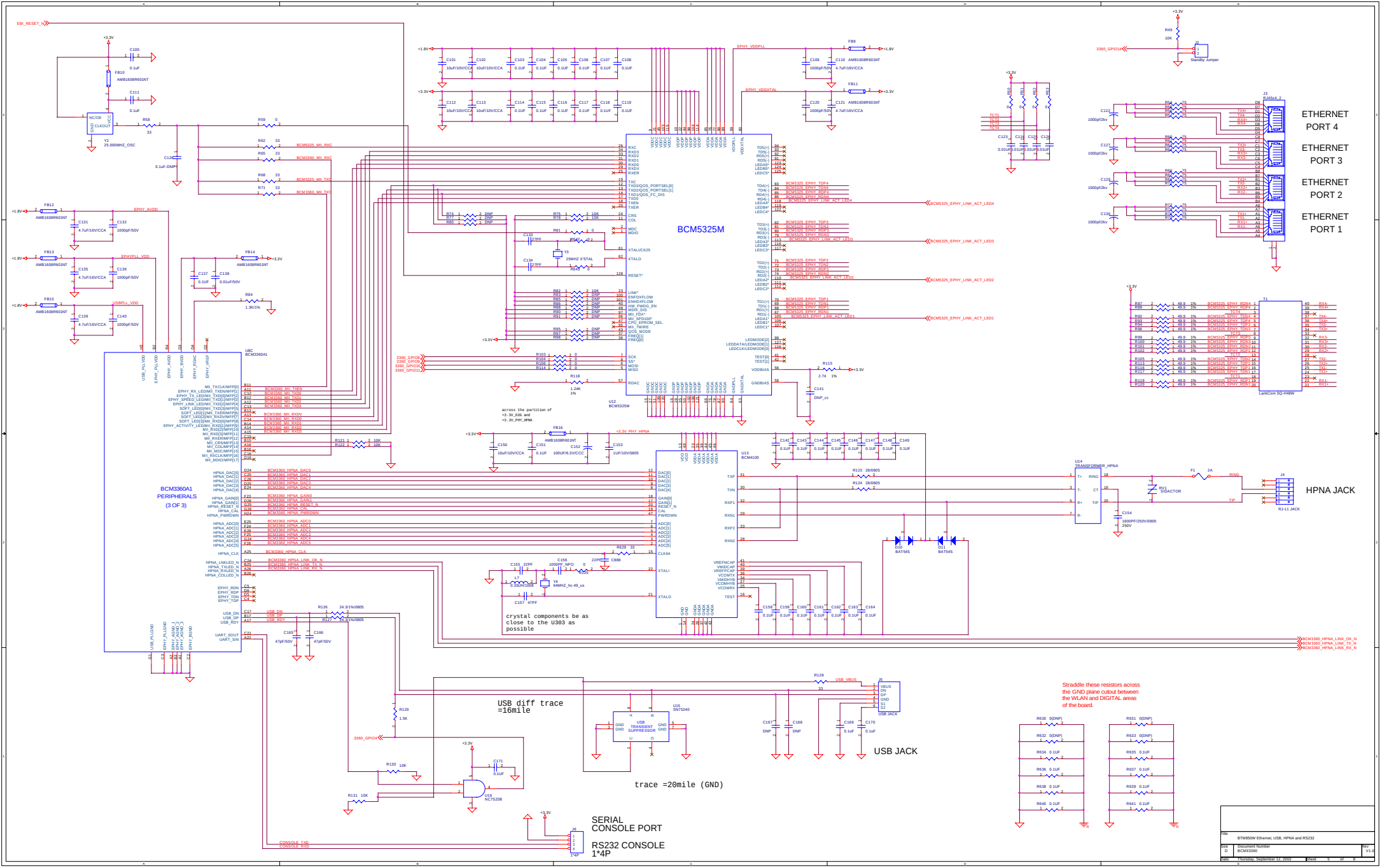


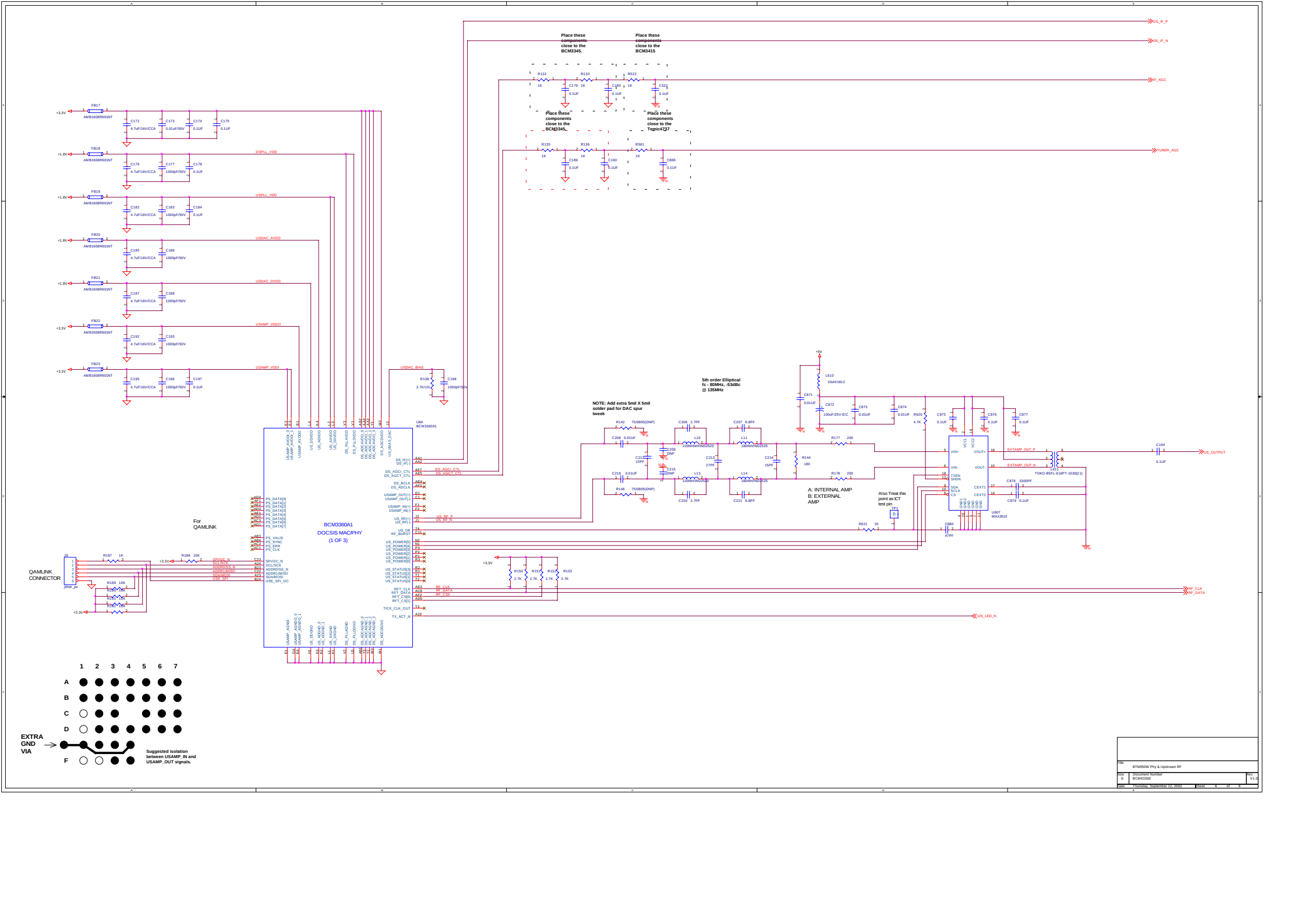
Title	Power	
Size C	Document Number BTM850W	Rev 3
Date: Thursday, September 12, 2002	Sheet 2 of 8	

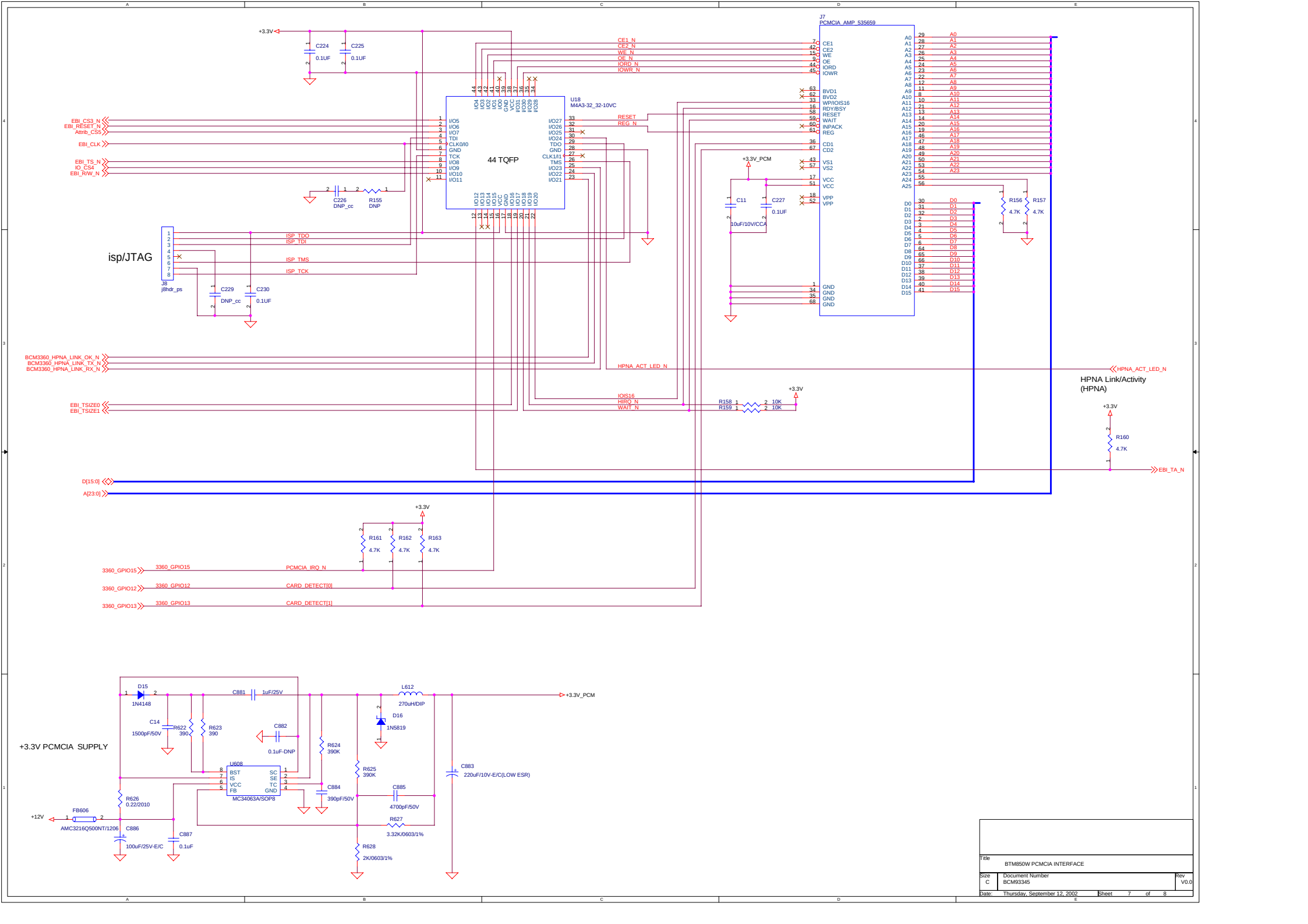

FOR U201
U201 PIN 1,14,27,3,9,43,49先個別
經過一個電容再接到 +3.3V_DIG
FOR U202
U202 PIN 1,14,27,3,9,43,49先個別
經過一個電容再接到 +3.3V_DIG
BCM3360A1
SDRAM/EBI/TEST BUSSES
(2 OF 3)
Place these resistors in order, in a column on the component side of the board.
NOTE: Route XTAL traces away from DAC output pins and add GND guard trace to separate DAC outputs from XTAL pins
MODEM RESET
BOARD REVISION LEVEL
GPIO READBACK == "0" IF 1K
GPIO READBACK == "1" IF DNP
3360_GPIO8
3360_GPIO9
3360_GPIO10
[DNP, DNP, DNP] = Bcm93360s_v0.0
[DNP, DNP, 1K] = Bcm93360_v0.0
[DNP, 1K, DNP] = Bcm93360_v1.0
[DNP, 1K, 1K] = Bcm93360s_v1.0
[1K, DNP, DNP] = Bcm93360e11_v0.0
[1K, DNP, 1K] = TBD
[1K, 1K, DNP] = TBD
[1K, 1K, 1K] = TBD
3360_GPIO11
[DNP] = HPNA INSTALLED
[1K] = HPNA DEPOPULATED
BTM850W CPU & MEMORY
Document Number
BCM93360
Rev
V1.0
Thursday, September 12, 2002
Sheet 3 of 8

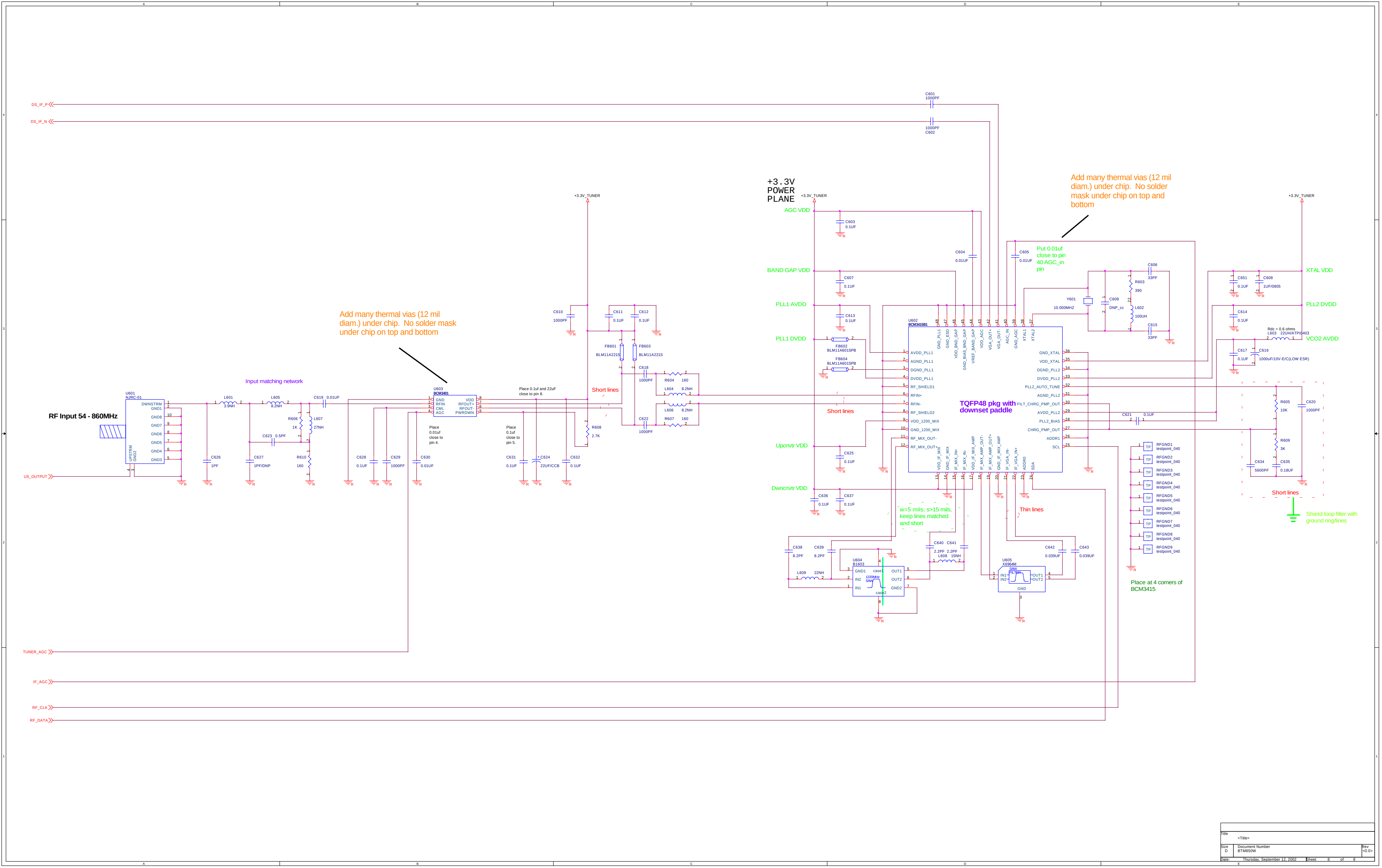


Title	BTM850W LED's	
Size C	Document Number BCM93345	Rev V0.0
Date: Thursday, September 12, 2002	Sheet 4 of 8	


BCM5325M
BCM3360A1
PERIPHERALS
(3 OF 3)
BCM4100
ETHERNET PORT 4
ETHERNET PORT 3
ETHERNET PORT 2
ETHERNET PORT 1
HPNA JACK
USB JACK
SERIAL CONSOLE PORT
RS232 CONSOLE 1*4P
USB diff trace =16mile
trace =20mile (GND)
crystal components be as close to the U303 as possible
across the partition of +3.3V_DIG and +3.3V_PHY_HPNA
Straddle these resistors across the GND plane cutout between the WLAN and DIGITAL areas of the board.
BTM850W Ethernet, USB, HPNA and RS232
Document Number
BCM93360
Rev
V1.0
Thursday, September 12, 2002
Sheet 5 of 8


Place these components close to the BCM3345.
Place these components close to the BCM3415
Place these components close to the BCM3345.
Place these components close to the Tepic4737
DS_IF_P
DS_IF_N
RF_AGC
TUNER_AGC
DSPLL_VDD
USPLL_VDD
USDAC_AVDD
USDAC_DVDD
USAMP_VDDO
USAMP_VDDI
USDAC_BIAS
FB17
FB18
FB19
FB20
FB21
FB22
FB23
AMB1608R601NT
U8A
BCM3360A1
BCM3360A1
DOCSIS MAC/PHY
(1 OF 3)
For
QAMLINK
QAMLINK
CONNECTOR
NOTE: Add extra 5mil X 5mil solder pad for DAC spur tweek
5th order Elliptical
fc - 80MHz, -53dBc
@ 135MHz
A: INTERNAL AMP
B: EXTERNAL AMP
Also Treat this point as ICT test pin
U607
MAX3510
TOKO-B5FL-6168PT-1030(2-1)
US_OUTPUT
US_LED_N
RF_CLK
RF_DATA
EXTRA
GND
VIA
Suggested isolation between USAMP_IN and USAMP_OUT signals.
BTM850W Phy & Upstream RF
Document Number
BCM93360
Rev
V1.0
Thursday, September 12, 2002
Sheet 5 of 8


J7
PCMCIA_AMP_535659
U18
M4A3-32_32-10VC
44 TQFP
isp/JTAG
J8
j8hdr_ps
HPNA Link/Activity
(HPNA)
+3.3V PCMCIA SUPPLY
U608
MC34063A/SOP8
AMC3216Q500NT/1206
1N4148
1N5819
Title
BTM850W PCMCIA INTERFACE
Size
C
Document Number
BCM93345
Rev
V0.0
Date:
Thursday, September 12, 2002
Sheet
7
of
8


DS_IF_P
DS_IF_N
US_OUTPUT
TUNER_AGC
IF_AGC
RF_CLK
RF_DATA
RF Input 54 - 860MHz
Input matching network
Add many thermal vias (12 mil diam.) under chip. No solder mask under chip on top and bottom
+3.3V POWER PLANE
+3.3V_TUNER
AGC VDD
BAND GAP VDD
PLL1 AVDD
PLL1 DVDD
Upcnvtr VDD
Dwncnvtr VDD
XTAL VDD
PLL2 DVDD
VCO2 AVDD
Put 0.01uf close to pin 40 AGC_in pin
Add many thermal vias (12 mil diam.) under chip. No solder mask under chip on top and bottom
TQFP48 pkg with downset paddle
Short lines
Thin lines
w=5 mils, s>15 mils, keep lines matched and short
Place 0.1uf and 22uF close to pin 8.
Place 0.01uf close to pin 4.
Place 0.1uf close to pin 5.
Place at 4 corners of BCM3415
Shield loop filter with ground ring/lines
Rdc = 0.6 ohms
U601 NJRC-01
U602 BCM3415B1
U603 BCM3401
U604 B1603
U605 X6964M
Y601 10.000MHZ
Title <Title>
Size D
Document Number BTM850W
Rev <0.0>
Date: Thursday, September 12, 2002
Sheet 8 of 8