1 Theory of Operation

The BSR100 transceiver consists of five major blocks:

- Receiver
- Transmitter
- Synthesizer
- Microcomputer
- Modem module
- Power supplies

The following is a description of operation for the five major blocks and their modules.

1.1 Receiver

The Receiver consists of four major blocks:

- VHF Front-end Circuits
- Double-Balanced Mixer
- 45 MHz IF Section and Back-end IF IC with RSSI meter and channel monitor functions.

1.1.1 VHF Front-end Circuits

The VHF Front-end circuit consists of tree blocks of circuitry: Pre-selector, RF amplifier, and Post-selector filter. The Pre-selector and Post-selector filters are fixed tuned designs and provide wide-band operation.

The pre-selector is a 3-pole, .01 dB Chebyshev band pass filter with capacitive coupled resonators .The 3 dB bandwidth is 19 MHz, centered at 145.5 MHz and the insertion loss is -1.5 dB. The pre-selector filter's output termination is connected to the RF amplifier that follows it.

The RF amplifier is a class A common-emitter amplifier with an active bias network. It has approximately +16 dB gain with 3 dB NF and is supplied by a +8V supply (+8 Vr).

The post-selector is a 4-pole, .01 dB Chebyshev band pass filter with capacitive coupled resonators .The 3 dB bandwidth is 19 MHz, centered at 145.5 MHz and the insertion loss is -2.5 dB. The post-selector filter operates with a 50-Ohm output termination. The input termination is connected to the RF amplifier. The output transmission is connected to the mixer that follows.

1.1.2 Double-Balanced Mixer

The Double-Balanced Mixer is JMS-1. DBM configuration consists of four diodes and two balanced mixers connected in a "ring" configuration. The Double-Balanced mixer uses two hybrids, which improve both the L-R and R-I ports. Because of its highly balanced and symmetrical configuration, this type of mixer theoretically suppresses 75% of possible IM products. The level mixer is +7 dBm and its conversion loss is -7 dB max.

1.1.3 45 MHz IF Section and Back-end IF IC

The Intermediate Frequency (IF) Section consists of: 45 MHz IF and back-end IF IC blocks. The first LO signal and RF signal mix with the IF frequency of 45 MHz and then enter the IF portion of the radio.

The signal passes through a diplexer network (DN) to optimize intercept point performance by not allowing any signals, especially local oscillator (LO) harmonics, to be reflected back into the mixer. The signal passes through a number of filters. The first crystal filter, 45M7.5A, provides selectivity; the second, 45M7.5A, image and intermodulation protection.

The 45M7.5A filter is a 2-pole filter with a 1 dB ripple, -2.5 dB insertion loss, -3dB bandwidth of ±3.75 kHz, -18 dB bandwidth of ±16 kHz, and ultimate rejection of -40 dB. The IF 45 MHz signal is amplified by the IF amplifier, MAR-6SM. The amplifier provides a +18dB gain with a 3 dB noise figure, draws 16mA of current, and is supplied by the +8 Vr.

The signal then passes through the second crystal filter, 45M7.5A, which provides further selectivity and second image rejection.

The filtered and amplified IF signal is then mixed with the second local oscillator at 44.545 MHz. The second LO is internal to the narrowband FM IF chip, an external crystal, and some external chip parts. The MC3372D chip consists of an oscillator, mixer, and limiting IF Amplifier, Quadrature Discriminator and Squelch Switch

The output mixing of the IF signal and the section LO produce a signal at 455 kHz. This signal is then filtered by external ceramic filter CFU455F and amplified. The CFU455F filter is a ceramic filter for communication equipment on 455.0 kHz ±1 kHz center frequencies, with a 1dB ripple, -6 dB insertion loss, -6 dB bandwidth of ±4.5 kHz and stop band att. of -25 dB.

The "Toko" 5PLC-A473HM low profile discriminator is used in the circuit of the demodulator. The resulting detected audio output is then sent to the external connector through the audio low-pass filter.

1.2 Transmitter

The VHF transmitter contains:

- Antenna switch
- Harmonic filter
- Power amplifier
- Synthesizer
- Two point modulation module

1.2.1 Antenna Switch

The Antenna Switch circuit consists of two PIN diodes and lumped elements to simulate the λ/4 section. When D1 and D2 are both ON, transmit mode is active. When D1and D2 are both OFF, receive mode is active. To activate receive isolation while transmitting, use D2 as a short-circuit termination for the λ/4 section.

PIN diode UM9401F provides high isolation, low loss, and low distortion, and can handle over 100W of transmitter power in VHF and UHF bands.

1.2.2 Harmonic Filter

The purpose of the low-pass filter is to attenuate the harmonics of the transmitted signal, but low-pass filter is reflective. This means that the undesired harmonics are reflected back into the device and remix. This effectively increases the level of harmonic output from the active device, and therefore, the low-pass filter should provide about 20 dB more rejection then appears to be required. The low-pass filter is of a Chebyshev design.

1.2.3 Power Amplifier

The power amplifier consists of an output power amplifier, drive, and predrive. The Output power amplifier contains one-transistor stages: n-p-n silicon RF VHF power transistor 2SC2539.

The 2SC2539 transistor, purchased from Mitsubishi, has Pout = 14 Watt, Pin=0.5Watt, Vcc = 13.5V, power gain ≥8 dB/F = 150 MHz, and is designed for RF power amplifiers on VHF band mobile radio applications.

The drive is class C amplifier and it use the MRF4427 transistor, purchased from Motorola, has Pout =1.0 Watt, Pin=30mW and is designed for VHF large-signal class C amplifier applications.

The predrive is a MMBR 5179(7H) high frequency transistor with high

gain 15 dB/200 MHz and low noise NF=4.5/200MHz.

1.3 Synthesizer

The serial input PLL frequency synthesizer consists of the following blocks:

- MB1501 chip (Fujitsu Microelectronics Inc.)
- TXO 225B
- VCO/ Rx
- VCO/Tx
- Tx/buffer amplifier: MAR7SM
- Rx/buffer amplifier: MAR8SM
- Feedback buffer amplifier: MAR7SM
- Control signal generator
- 16-bit shift register
- 15-bit latch
- 1-bit switch counter
- Phase comparator
- Charge pump
- Crystal oscillator
- 19-bit shift register
- 18-bit latch
- Programmable divider

1.3.1 MB1501 Chip (Fujitsu Microelectronics Inc.)

The Fujitsu MB1501series chip contains: 1 The Fujitsu MB1501series contain: a 1.1GHz two modulus prescaler that can select either 64/65 or 128/129-divide ratio, control signal generator, 16-bit shift register, 15-bit

latch, 1-bit switch counter, phase comparator, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, and programmable divider This chip has major electrical characteristics: the power supply current typ Min 15mA,Vcc +5V,Vp +8V.

1.3.2 TXO225B

The synthesizer uses a 12.8 MHz reference from the VCTCXO-5DSL 12.8 MHz. It provides operating temperature stability of synthesizer ±2.5ppm -30°C to 75°C. The SSB phase noise on 10 kHz is -145 dBc/Hz, the power supply is +3V ±5% and its current is 2 mA. The VC port is used for the 12.8MHz reference frequency external modulation.

1.3.3 Passive loop filters

The passive loop filters provide the DC steering voltage for the VCO/Rx &VCO/Tx as well as filtering of spurious signal from the phase detector.

1.3.4 VCO/Tx- Rx

The Clapp circuit configuration is used for high stability oscillation in the VCO/Rx* and VCO/Tx mode with which the VCO resonator is isolated from the load.

*Rem. VCO Rx is oscillate the high side band frequency's relative to carrier frequency.

1.3.5 Tx/Buffer Amplifier

The Tx/buffer amplifier, MAR7SM, provides isolation VCO/Tx from load .The amplifier specification has the frequency range DC-2 GHz. The gain is 16 dB, the 1 dB output compression is +5.5 dBm, the input no damage is +13 dBm, the NF is 5 dB and DC power at pin 3 is 22 mA, + 3.5V.

1.3.6 Rx/Buffer Amplifier

The Rx/buffer amplifier, MAR8SM, provides isolation VCO/Rx from the load and raises gain to level +13 dBm. This amplifier has the following specification: frequency range DC-2 GHz, the gain is 22 dB, the 1 dB output compression is +12.5 dBm, the input no damage is +13 dBm, the NF is 3.3 dB and DC power at pin 3 is 36 mA, + 7.8V.

1.3.7 Feedback –3dB resistive pad.

The feedback –3dB resistive pad provides additional isolation from the Rx/Tx VCO to the input 8 "Fin" of the MB1501.

1.3.8 Two-point modulation module.

The proliferation of computers in today's society has increased the demand for transmission of data over wireless links. Binary data, composed of "one to zero" and "zero to one" transitions, results in a spectrum rich in harmonic content that is not well suited to RF transmission. The Differential Raise Cosine Minimum Shift Keying modulation technique have a place in BSR100D modem.
Data patterns consisting of several consecutive ones or zeros have a spectral

response extending down to near DC. Most frequency synthesizers will not respond to this low frequency signal. The modulation method which help considerably where the non-linear behavior of the synthesizer is concerned, is " Two-Point modulation ".

Two-Point modulation circumvents pattern sensitivity synthesizer effect by splitting the Differential Raise Cosine filtered signal; one portion is directed to the VCO modulation input thought U19B,U19C instrumental amplifiers , the other portion is used to modulate the VCTCXO.

The VCTCXO is not in the frequency control feedback loop. Hence, the VCTCXO can be modulated by the low frequency portion of the signal, and its output is effectively summed with the signal modulation the VCO in the synthesizer. The composite signal has response extending down to DC.

1.5 Modem Module Circuit Description

The Loader/Modem board, Part № 03280-xxx, is a plug-in circuit board.

The Loader/Modem board connects to the radio through connector P/J201.

Transmit Data from RS-232 port is level-shifted to TTL by U1 then gated through U6 and converted from asynchronous to synchronous format by U2.

The PLCD modem, U6 takes the digital data stream and synthesized to the constant-amplitude analog base band signal, which is filtered by U12, buffered by U10B then applied to transceiver at P1-6

The modem IC is a CPLD based on a Philips extended Programmable Logic Array (XPLA, PZ5812)which, with a programmable Raise-Cosine filter (U12),operates in DRCMSK mode at 9600 bit/sec.

Received signals are applied to pin P1-13 and amplified by U7A then filtered by U12 .The filter U12 cut-off frequency is programmable by the CPU, based on the data rate. The analog signal is then fed to Peak Detectors U7C,D to the slicer circuit .The resulting synchronous bit stream is converted to asynchronous at U2 and shifted to RS-232 levels by U1.

Voltage Regulator U14 (DVCC) provides 5V for the CPU and other digital logic, While U13 (AVCC) provides 5V for analog modem circuits.

1.6 Power Supplies

The following voltage levels are necessary for major blocks of the BSR100D:

- +12.5 Vb for the output power amplifier, the driver and antenna switch feeds.
- +8V for the driver and predriver feeds.
- +5V for the digital block, modulator chip, and active audio filter supply.
- +8 Vs and +5Vs for the synthesizer feed.
- +8 Vr and +5 Vr for the RF, IF amplifiers, and MC 3372D chip feeds.

To provide the noise junction between the electrical feed circuits of the transceiver blocks, and so that the supply voltage is sufficiently clean and stable, the Power Supply contains five LP2951 low-dropout micro power-voltage regulators.

The following voltages come through switch transistors to the cascades of BSR100: +8V, +8 Vv (from the 8 Vv and 8V regulators), and +12.5 Vb (from VB port).

Under the following conditions, BSR100D operations stops:

- When there is an error in the output voltage from the regulators (bus error), an error signal is sent to the micro-controller and operation stops.
- When the battery output voltage is at a low Vb voltage level, the +8 Vv voltage regulator sends a “dead battery” signal to the micro-controller and operation stops.

In Tx mode, the +8v voltage is sent through switch transistors to the driver and predriver cascades of the transmitter .The +VB voltage through switch transistors is sent to the antenna switch. The voltage +8Vv is sent through switch transistors to VCO\Tx and to the buffer amplifier.

1.7 Micro-Controller

The micro-controller, AT 89C52, is the original member of the MCS@-51 family. The main features of the AT 89C52 are:

- 8-bit CPU optimized for control applications.
- Extensive Boolean processing (single-bit logic) capabilities.
- 64K program memory address space.
- 8K bytes of on-chip Data Memory.
- 256 bytes of on-chip Data RAM.
- 32 bi-directional and individually addressable I/O lines.
- Two 16-bit timer/counters, full duplex.
- UART
- 6-source/5-vector interrupt structure with two priority levels
- On-chip clock oscillator

The micro-controller operates with an external E2PROM. The Gup10™ external computer program is used to change the receiver, transmitting frequency, time out timer, and PTT Delay.

The input serial data (from the laptop/PC) is sent to the micro-controller through the external communication connector. The micro-controller produces Clock, Data, and Load Enable signals on pins: 9,10, and 11 of the MB1501 chip. It uses the lock detection signal to determine phase comparator output. When level on its port is low, the phase is locked. While the phase difference of Fr and Fp exists, the output level goes high.

The PTT1 external signal is used to configure the Tx/Rx modes. If the PTT1 level is “0,” Tx mode is active. When the Lock Detector bus is “0,” the micro-controller through ~ 15 msec shows PTT2 = ”0,” and the transmitter is in Tx mode. Conversely, if the PTT1 level is “1,” Rx mode is active. When the Lock Detector bus is “0,” the micro-controller shows PTT2 ”1,” and the transmitter is in Rx mode.

The micro-controller uses the Channel monitor signals for the channel busy determination. It makes signals for the Led indications (see description of self-test LED’s).

2.1 The basic testing, adjustment and maintenance procedures

This document outlines the basic testing, adjustment and maintenance procedures required for initialization BSR100D wireless radio modem in manufacture condition.

2.2 Equipment Requirement

- 12.5VDC (nominal) 5A regulated power supply's
- Radio Service Monitor (IFR COM-120A or equivalent)
- Digital oscilloscope
- RF Signal generator
- Spectrum analyzer
- Sinadder
- Multimeter
- The BSR100D external repair adapter
- Assembly cables
- RF attenuators kit.
- T-96SR digital modem module
- 486 PC or better (with two RS-232 port COM)
- T-96SR Radio Service Software
- BSR100 GUP10 Software
- Normal radio shop tools.

2.3 BSR100D Testing

2.3.1 GENERAL

This section of the instruction is intended for testing, adjustment and maintenance BSR100D modem procedures in manufacture conditions.

Only the qualified personnel given examination and past training can be admitted to performance of works specified in this instruction.

The deviation from the given instruction can result in damage of the verifying equipment and to infringement of a BSR100D function.

2.3.2 Basic testing maintenance and adjustments

1. The BSR100D preparing for the first voltage power feeding.
2. Tx mode transmitter alignment procedure.
3. Rx mode receiver alignment procedure
4. Tx mode modem alignment procedure
5. Rx mode modem alignment procedure
6. Final Tx/Rx BSR100D modem testing
7. The modem results testing form completion.

2.3.2.1 The BSR100D preparing for the first voltage power feeding.

- Connect the measuring and auxiliary equipment for the Tx mode BSR100 transceiver alignment procedure in accordance with the manufacture testing setup diagram.
- Prepare the BSR100 transceiver for the first voltage power feeding, as follows:
  a) Visually inspect the PS and CS sides of the BSR100 board to eliminate short circuits, breaks, and other defects.
- Power ON the 12.5 VDC power supply, as follows:
  a) Check the current consumption of the BSR100 transceiver.
  It must be near 80 mA DC.
  b) Power OFF the 12.5 VDC power supply.
  c) Insert the micro-controller chip in its circuit.
  d) Power ON the 12.5 VDC power supply.
  e) Check the following:
  1. Current consumption of the BSR100 transceiver (it must be 140mA).
  2. Self-test LEDs diagnostic.
  g) Power OFF the 12.5 VDC power supply.

2.3.2.1 The Tx mode transmitter alignment procedure:

a) Connect the plug of the T96SR module to the BSR100D on board connector.

b) Power ON the 12.5 VDC power supply.

c) Check the following:
- Current consumption of the BSR100 transceiver must be180mA.+/- 10%
- Self-test T-96SR module LEDs diagnostic.

d) Using the modem setup cable, connect the T-96SR to PC
***Do not use this cable to connect a user application**
The green modem's LED flashes to indicate the unit in setup mode.

e) By PC T96SR Lab Setup Software program to write necessary parameters to T-96SR module.

f) Using the radio setup cable, connect the BSR100D to PC and by Use the Gup10 utility program to write the Rx/Tx frequency of the BSR100D transceiver to middle frequency band.

g) Connect the measuring and auxiliary equipment for the Tx mode BSR100D transceiver alignment procedure in accordance with manufacture Tx mode testing setup diagram.

h) Screw on cooling radiator to output power transistor

l) Power ON the 12.5V DC power supply.

i) Short for 10 sec. and release the self-test external PTT button.

k) Check DC voltage +2.5V+/- .01V (fulfill a requirement i.) on Tp22 by DVM and adjust it by P5 potentiometer.

l) Measure the output power of the BSR100 transceiver. Maximum power reading 12W±15%. *(See m.)

m) Adjust trimmer capacitor C159 to receive equal output power on the low and high frequency's of a working band. Nominal power reading is 12W±15%.

n) Check Tx mode current consumption. Current should be 2.4A ±5% on the middle frequency of the working band and ±15 %, accordingly on the low and high frequency's of a working band.

o) Using the modem PC DATA cable, connect the BSR100D Data port to COM PC

p) By PC SIMPTERMINAL Software program (previously having determined all COM ports parameters) send RTS (PTT) command to BSR100D.

r) Check DC voltage +2.5V+/- .01V on Tp22 by DVM and adjust it by P5 potentiometer.

s) Adjust by P4 for the desired modulation, 2.2 kHz +/-5% carrier deviation

t)Check the synthesizer out put frequency (fulfill a requirement r.). It should be +/- 0.1ppm. Using a trimmer capacitor on the body of the VCTCXO-5DSL, adjust the synthesizer output frequency.

u)Check the spurious/harmonics, requirements: Power 50+10log (Pout) or 70 dB, hichever is less.

v) Observe by digital oscilloscope the audio signal on "DEMOD OUT"
IFR COM-120A CON. It must be look enough clear and do not have a pattern sensitivity effect,
in case of need if ,necessary repeat § r,s and t.

w) Power OFF the 12.5 VDC power supply.

1.3.2.2 Rx mode receiver alignment procedure

a) Power ON the 12.5 VDC power supply.

b) Using the radio setup cable, connect the BSR100D to PC and by Use the
Gup10 utility program to write the Rx frequency of the BSR100D transceiver to the middle frequency band.

c) Power OFF the 12.5 VDC power supply.

d) Connect the measuring and auxiliary equipment for the Rx mode BSR100D transceiver alignment procedure in accordance with manufacture Rx mode testing setup diagram and execute (a).

e) Set the IFR COM 120A RF generator output to frequency that was written in b), to signal level -80 dBm with 2.2 kHz-frequency deviation and internal sine wave modulation 1kHz.

f) Observe by digital oscilloscope and sinadder audio signal DATA OUT on he BSR100D external repair adapter.

g) Adjust trimmer capacitors C2029, C2030 and L72 tunable RF discriminator and try to get audio **sine** wave 1 kHz distortion 3 %. +/-1.5%

h) Set the RF generator output to signal level –117dBm with 2.2 kHz-frequency deviation and internal **sine** wave modulation 1 kHz.

i) If necessary, adjust trimmer capacitors C2029, C2030 and L72 until that sensitivity run up <-117dBm (12 dB SINAD)

j) Repeat § **e, f, g** so long as it necessary to obtain audio sine wave 1 kHz distortion 3 % +/-1.5% at signal level -80 dBm and sensitivity <-117dBm (12 dB SINAD).

k) Set the RF generator output to signal level -80 dBm with 2.2 kHz-frequency deviation and internal **square** wave modulation 1kHz.

l) Observe by digital oscilloscope square wave audio signal DATA OUT. If necessary, adjust trimmer capacitors C2029, C2030 and L72 until that square wave
will have enough steep slope front and rear with minimum roof ripple.

m) Repeat § e, f, g, h, i, j.

n) The modem PC DATA cable connect to the BSR100D Data port (DCE1) and to COM PC (DTE1).

o) Audio in signal from T-96SR module connect up to RF signal generator to "CON MOD INP/OUT" (DCE2) and set the external AC signal for the RF frequency FM modulation level 2.2kHz . RF signal generator set to amplitude level -113 dBm.

p) PC "SIMPTERMINAL" Software program (previously having determined all COM ports parameters) ON for the DTE1 and DTE2.
From DTE2 PC by "SIMPTERMINAL" Software program send massive data file by DCE2 to DCE1,DTE1

q) Adjust red/green light CM. LED response with help of the P2 potentiometer by RF generator output level variation from -113 dBm to -114 dBm.

r) Observe on DTE1 PC display receive digital massive file on -108 dBm (0.89μV) RF signal level. It must be clear and have not noisy characters.
BER must be better than 1*10^-6 (-107dBm) at 1μV at 9600 b/s half channel

s) Power OFF the 12.5 VDC power supply.
t) Assemble all mechanical parts and power ON the 12.5 VDC power supply.
u) Repeat § n, p, q, r and execute § s.

1.3.2.3 Final Tx/Rx BSR100D modem testing

a) Assemble testing equipment for the Final Tx/Rx BSR100D modem testing accordance with manufacture Rx mode testing setup diagram.

b) To install "RF modem tester" Software program (previously having determined all COM ports and other parameters) for the DTE1 and DTE2.
From DTE2 PC by "RF modem tester" Software program send testimage.jpg file by DCE2 to DCE1, DTE1
The testimage.jpg file must be received without video distortion on DTE1.
c) From DTE1 PC by "RF modem tester" Software program send testimage.jpg file by DCE1 to DCE2, DTE2.
The testimage.jpg file must be received without video distortion on DTE2.

2.3.3 The modem final testing results form completion.

On the ending **2.3.2.1** … **2.3.2.4** to fill in the form given below

BSR100D
Final testing results form

BSR100D **Serial № …**
Cust. name:
Order mber:

Micro

Tx mode						
№	**Electrical test**		**Result**			**Notes**
1.0	The Tx V and I Consumption		U DC (V)	I load on (A)		DC Power Supply
			12.95			
1.1	The output power Pout		F low	F middle	F high	IFR COM-120A
		MHz				
		Watt				
1.2	Spurious harmonics max K (dBc)					Spectrum analyzer
1.3	Modulation level (KHz)					IFR COM-120A
1.4	The transm. freq (MHz)					GUP10 IFR COM-120A
	Pout					
	Tx frequency error ΔF(KHz)					
	Modulation level (KHz)					
Rx mode						
2.0	The Rx mode V and I Consumption		U DC (V)	I (mA)		DC Power Supply
			12.95			
2.1	Receiver sensitivity (12db sinadd)		Flow	F middle	F high	RF Signal Generator, 1kHz sine internal sig.
		MHz				
		(dBm)				
	Audio distortion	%				
2.2	Receiver –108dBm input level pattern sensitivity	+/-				RF Signal Generator, Ext.modul. signal (digital massive)
2.3	The receiver working frequency f Rx (MHz)					GUP10
2.4	Channel monitor K dBm		ON	OFF		RF Signal Generator, Ext.modul. Signal (digital massive)
3.0	**Final Tx/Rx BSR100D modem testing**					
3.1	DTE1 to DTE2 Transfer testimage.jpg file			+/-		BSR100D (DCE1) BSR100D (DCE2)
3.2	DTE2 to DTE1 Transfer testimage.jpg file			+/-		

Engineer:
Date :