Selecting "Yes" exits the factory calibration menu. The menu will also be automatically exited, and normal operation restored if no calibration function is ongoing, and no keypad activity has been detected for three minutes.

7.3 Module Replacement

The recommended field service procedure for out of warranty OFR repair is to localize the problem to a specific module, and make a replacement at the module level. OFRs are designed with a modular architecture that makes such replacement fast and easy. Defective modules can be returned to Kaval Telecom for repair or replacement. Contact you Kaval Telecom Customer Service Representative to discuss a service plan to meet your requirements. All returns must be accompanied by a Returned Materials authorization number that can be obtained by calling Kaval Telecom.

7.4 Module Alignment

All module alignment procedures assume that the circuit has had power supplies and active device bias points checked out with a DC voltmeter.

7.4.1 Front End

See Appendix A-1 for a front end alignment procedure. This text will be merged in, in the final document.

7.4.2 Local Oscillator

See Appendix A-2 for local oscillator alignment procedure.

7.4.3 IF/Transmitter

IF/Transmitter alignment proceeds stage-by stage from input to output. Helical filters must be rough-tuned before installation in factory

+9.6VDC is applied to the unit under test, OSCEN is tied to ground and AGCLIM is tied to +9.6VDC.

Temporarily remove R41 and R43. Disconnect AGC voltage between TP2 and U3B. (Test jumpers will be provided in next revision). Apply a variable clean DC signal at TP2.

Connect a network analyzer at the IF input and at TP9. Adjust AGC voltage to get a clean output sweep that is not clipping. Adjust C1 and C2 to get best flatness and lowest loss in IF filter shape. Verify 1 dB BW between 35 and 37 kHz. Verify ripple less than 1 dB.

Reconnect AGC. RF input is applied at the IF input terminal, unmodulated, at 21.4 MHz and at an initial level of -40 dBm.

Observe TP9 with a spectrum analyzer. Adjust R53 to get –10 dBm +/- 0.5 dB at TP9. Switch OSCEN to 9.6V. Verify output signal level is –10 dBm +/- 1 dB. Adjust C29 value to trim if required.

Vary input signal between –75 and 0 dBm. Verify that output level stays within 1 dB of –10 dBm.

Vary AGCLIM down with input at –75 dBm. Verify that output level drops at least 60 dB.

Apply a signal at –35 dBm at ID input and chop it using a high isolation electronic RF switch at 100 Hz.

Observe AGC voltage (at interface connector). Adjust R60 for maximum risetime of AGC voltage. Aim for critical damping (minimal overshoot). Verify risetime less than 1 ms. Repeat at –55 and –15 dBm. Adjust for best attack shape compromise at all levels.

Disable chopper. Vary input from –75 to 0 dBm. Observe AGC voltage. Verify it changes from about 4.5V to 1V.

Adjust R72 to get 5V at TEMP line.

Apply 24VDC to PSU input from a power supply limited to 500 mA. Turn TXEN high. Adjust R90 to get 14.5V at TP35. Adjust R82 to get 2.5V at TP17

Verify current is less than 450 mA in 24Vsupply.

Turn OSCEN high. Ground TXLEVEL. Raise PREEN to 9.6V. Observe output spectrum (through a 20 dB attenuator). Adjust FL2 for maximum signal. Then adjust FL! And FL2 for maximum signal. Use 1 dB/div range for fine tuning. Verify output level, when done, is greater than +30 dBm. If output exceeds +33 dBm at any step, raise TXLEVEL to reduce level to below +30 dm and continue optimizing.

Verify PFWD and PREV are greater than 0.25VDC.

Remove output load (remember to current limit PA at 500 mA). Verify PREV rises at least 0.25V

With power adjusted to +30 dBm, observe harmonics and any L.O. in output spectrum. Verify to be less than –20 dBm. Look for any unusual spurs in output.

Adjust TXLEVEL upward. Verify signal drops at least 30 dB before voltage reaches 3.0V.

Apply two unmodulated test signals at IF input at a level of –40 dBm each at 21.395 and 21.405 MHz. Use a low intermod combining network. System intermod must be < -65 dBc. Turn PREEN and TXEN on. Adjust TXLEVEL to get +27 dBm per carrier at output. Adjust R90 to minimize third order intermod. Verify intermod is less than –20 dBm absolute level. You may need to fine adjust IF level (R53) or further optimization. Also, minor adjustment of FL2 and FL3 may be helpful.

7.4.4 Control Unit

The control unit is factory tested by an automatic test fixture which analyzes operation of digital and analog signal lines. There are only two potentiometer adjustments required on the control unit.

1. The control unit is powered up by applying 12VDC at J4. The microcontroller will power up properly even if no external modules are connected. Use a current limited bench power supply.

2. Verify that all LEDs illuminate momentarily.

3. Verify that the software revision momentarily displayed at power up is the correct version.

4. Adjust contrast control R31 for best LCD contrast when viewed head on. Verify backlight illuminates.

5. Press the user buttons to scroll through a few functions to verify operation.

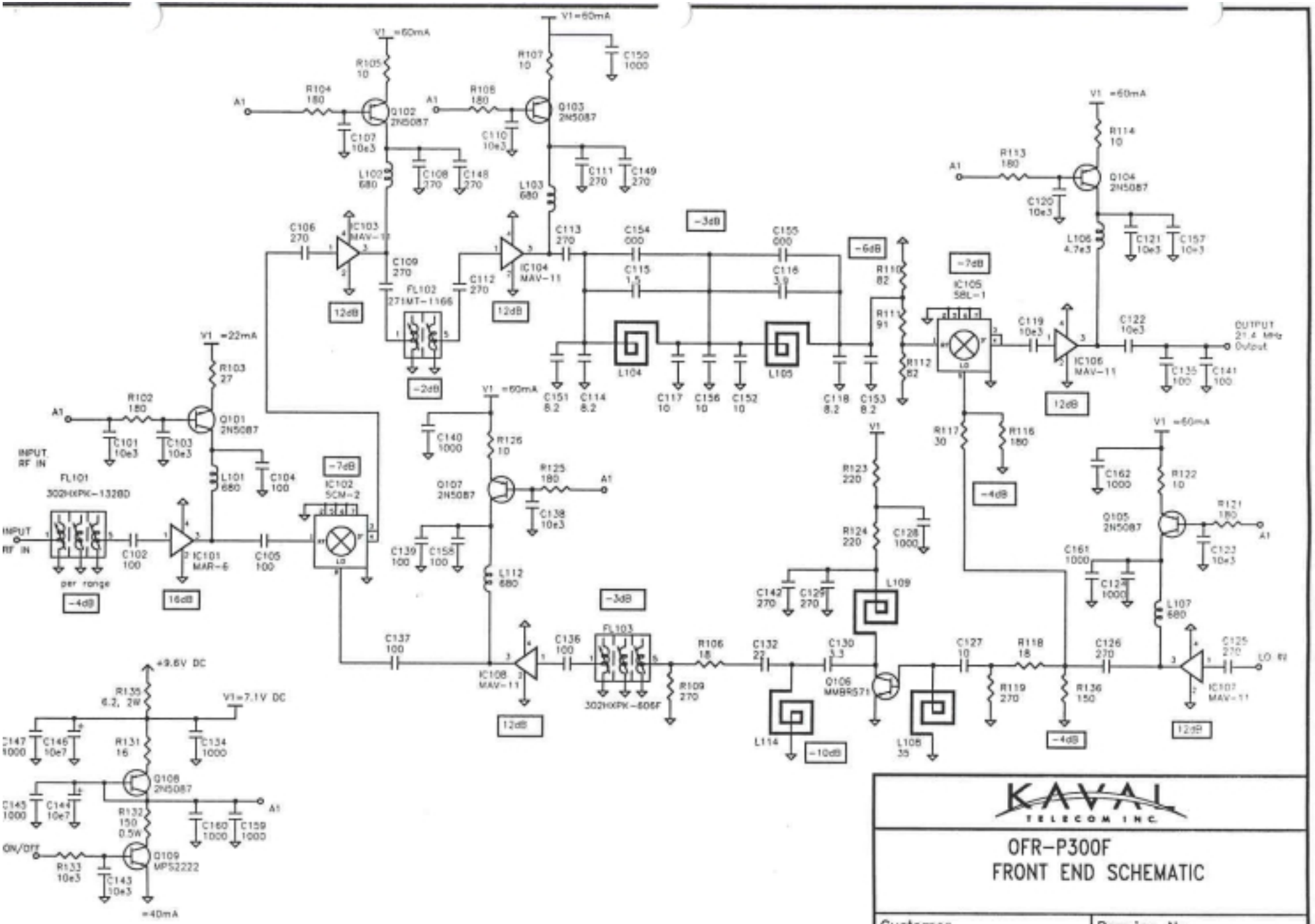
6. Adjust R2 to achieve 9.6VDC+/- 0.1 VDC at either pin of J5.

7. Alignment and basic check now complete

8 Drawings

8.1 Front End

8.1.1 Schematic 00M1C030.DWG

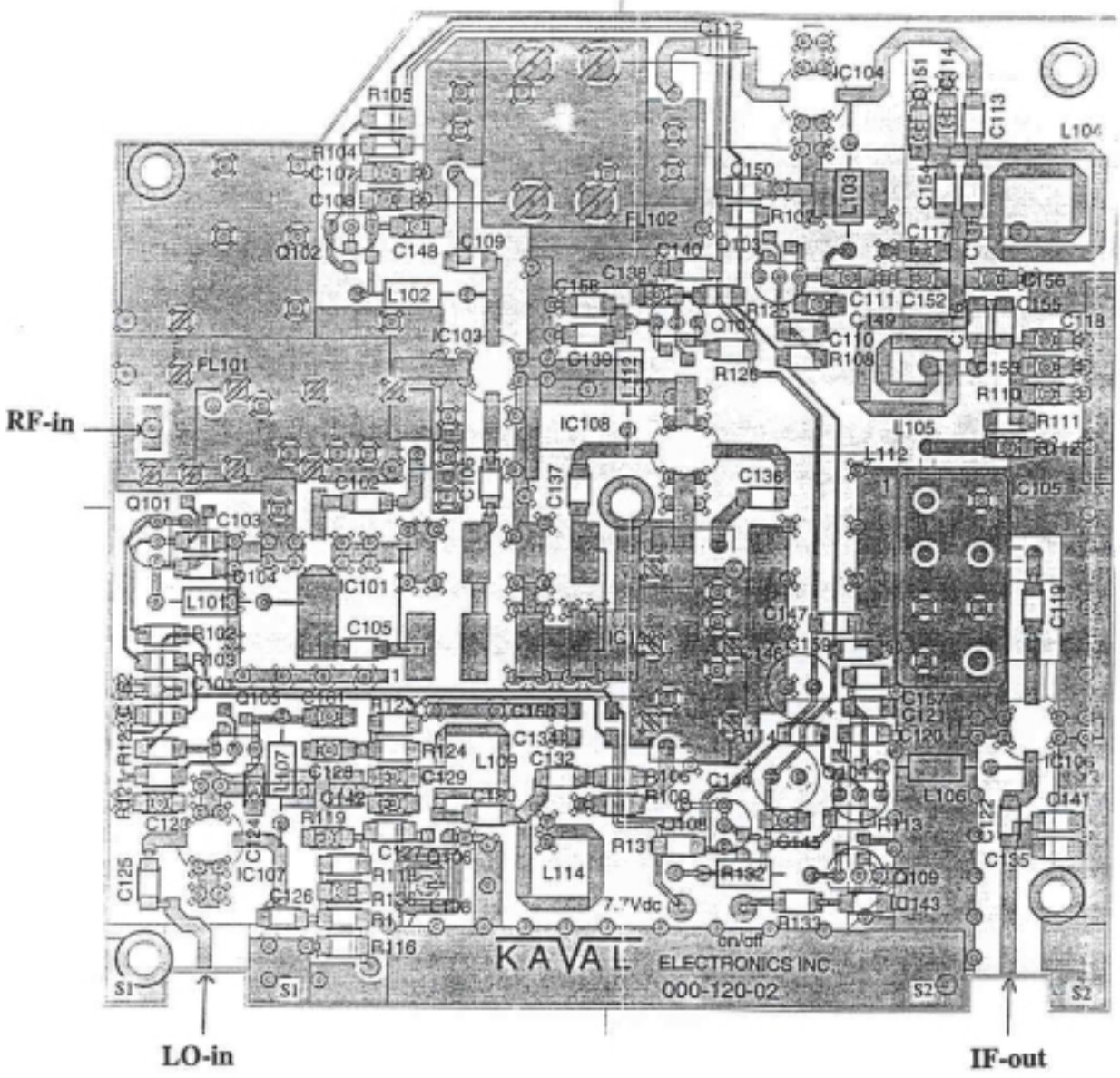


KAVAL TELECOM INC.

OFR-P300F
FRONT END SCHEMATIC

Customer		Drawing No. 00M1C030.DWG
Drawn E.C.	Checked E.C.	Issue Date Dec 8, 1998

8.1.2 Component Layout 00M02B050-9



KAVAL TELECOM INC.		
OFR-P300F Front End Module Component Layout		
Customer		Drawing No. 00M02B050-9
Drawn E.C.	Checked E.C.	Issue Date Dec 8, 1998