6.6.5 Reset

The RC network C22/R16 provides a startup delay to ensure that clocks and analog circuits have stabilized from power on transients before the computer attempts operation. D7 ensures that power supply dropouts promptly reset the MCU to prevent erratic operation that may result from low operating voltages. The RC time delay thus operates only on turn-on, and does not delay turn-off.

SW4 allows manual reset in case of system failure or computer disruption caused by power surges or static discharges.

6.6.6 Lamp Drivers

Transistors Q1, Q2, Q3 and Q5 are used as open-collector drivers for the front panel LEDs. LED supply is +12V.

6.6.7 Keypad

SW1, SW2 and SW3 are three user control buttons at the front panel. Each causes the state of a port line to change from high to low upon switch actuation. The microcontroller debounces any possible switch chatter to prevent multiple closure interpretations.

6.6.8 Serial EEPROM

U3 is a 16 k-bit serial EEPROM. It is accessed via a two-wire synchronous serial interface implemented by "bit-banging" port lines in the MCU. Data is clocked at pin 6 (clock source always the MCU). Data can be either input or output at pin 5 depending upon whether a read or write operation is in progress. This IC retains memory contents in the absence of power. It can tolerate 100,000 write cycles of any particular memory location.

6.6.9 PWM D/A

Outputs PLMA and PLMB of the MCU provide pulse width modulated digital waveforms that are integrated by U6A and U6B. The pulse rates at PLMA and PLMB are approximately 2 kHz. Pulse width resolution is 8 bits, providing 256 possible steps. A zero voltage results in these output staying at 0V. A full scale voltage (255) results in a constant +5V at PLMX. Intermediate settings result in a digital waveform of positive duty cycle proportional to the 8 bit word written to the PWM.

U6A and U6B are two pole lowpass filters used as integrators. Integrators have sufficient filtering to ensure that signal droop during any 0.5 ms PWM cycle is less than ½ bit of resolution, or $1/512^{th}$ of the full scale integrator output voltage. As a result, these outputs can only be varied very slowly.

U6A has an overall DC equivalent gain of 1.43, resulting in an output voltage range of zero to 7.15VDC. U6 generates the AGC limit control voltage. This is used to limit the AGC excursion to prevent self-oscillation when input RF signals are absent, or below the minimum safe gain margin of the OFR installation. A self-calibration of the RSSI function (see service chapter) allows the MCU to calibrate AGCLIM voltage against actual input level in dBm. This allows the user to set AGC limit by dialing up the appropriate AGC limit level in dBm. The microcontroller ensures that the user cannot set receive threshold below the AGC limit threshold plus the programmable threshold hysteresis.

Higher AGCLIM voltages mean higher AGC gain settings are allowed. Lower voltages clamp the AGC voltage at higher input levels hence reducing available sensitivity.

AGCLIM voltages are determined by reading a user setting command and using it to look up a voltage in a EEPROM table generated during factory calibration.

An automatic AGC limit setting function is available, which allows the user to automatically set up the OFR to ensure self-oscillation cannot occur. This is described in section 5.

U6B generates the transmit level control voltage. Lower voltages correspond to higher transmit chain gains and higher output power. U6B is essentially a voltage follower with an output voltage range of zero to 5 volts.

6.6.10 8 Channel A/D

The MCU can read up to 8 voltages in the range of 0 to +5VDC with 8 bit resolution. The parameters that are monitored are:

- Transmit forward power
- Transmit reverse power
- AGC voltage (system gain/input level)
- Transmitter internal temperature
- Transmitter final stage current
- +24V supply voltage.

Two A/D inputs are used to sense external control digital inputs. These are:

- Transmit Defeat
- External Fault (reserved for future use)

These various signals, along with actual or remembered user settings are used as inputs to the MCU's decision algorithms.

6.6.11 RS-232 Interface

U2 converts 5V serial logic signals to and from the MCU to +/-12V industry standard RS-232 levels. U2 includes internal charge pumps to create the necessary local +/- 12V supplies. RS-232 interface is available at J1, a 9 pin D-sub connector. Interface is configures as DCE (Data Communications Equipment) and has pin assignments similar to a modem. It is suitable for connection to a PC. If connected to a modem, a null-modem adaptor is required.

Table 3RS-232 Connector DCE

Pin	Description
1	CD (not connected)

2	TD (data to PC)
3	RD (data from PC)
4	DTR (connected to DSR)
5	GND
6	DSR (connected to DTR)
7	RTS (connected to CTS via driver)
8	CTS (connected to RTS via driver)
9	RI (not connected)

6.6.12 Fault Relay

A single dry relay closure connects the rear panel fault line to ground when any fault occurs. Exact nature of fault is displayed at the front panel.

The default state of the fault relay is closed. This ensures that primary power failure, total failure of the MCU, or a stuck reset condition result in a fault being indicated. The microcontroller must initialize successfully and deliberately turn the relay on to clear a fault. Transmitter is de-energized if any fault occurs. Since certain faults are inherently self-clearing upon transmitter de-energization, the fault indication will persist until the transmitter is keyed off and keyed on again.

Signaled faults are:

- Primary power failure (no front panel indication)
- MCU failure (no front panel indication)
- System uncalibrated
- Excess reverse power
- Insufficient transmit power.
- Excess transmit power
- Input overdrive
- Transmitter overtemperature.
- +24V supply failure
- Transmitter undercurrent
- Transmitter overcurrent.
- External fault.

The front panel fault LED duplicates the fault relay status for easy viewing.

6.6.13 LCD Interface

The MCU communicates with a controller local to the LCD module via an 8 bit parallel bus. This includes 8 data bits, a data strobe, read/write line and a reset signal. The LCD module connects to the control unit at J6.

R31 adjusts LCD contrast.

R32 current limits voltage used for LCD backlighting.

6.6.14 IF/Transmitter Interface

J2 provides interconnection to the IF/Transmitter module. This interface uses a 16 pin dual row header at the control unit and a 15 pin d-sub connector (filtered) at the IF/XMIT end.

Table 4 Radio interface (0.100 dual row)

PIN	SIGNAL	FUNCTION
1	+24	Final stage high current supply to TX
2	GND	Ground return for final stage from TX
3	PATEMP	Module temperature sense from TX
4	PREV	Reverse power level (voltage) from TX
5	PFWD	Forward power level (voltage) from TX
6	TXCURR	Transmitter supply current sense from TX
7	PABIAS	Transmitter gain (output level) control voltage
8	TXEN	Transmit enable to TX
9	PREEN	Preamplifier enable to TX
10	GND	Signal ground to TX
11	AGC	AGC voltage from IF
12	AGCLIM	AGC limit clamp voltage to IF
13	OSCEN	Internal test oscillator enable to IF
14	+9.6V	Main supply to IF and transmitter
15	GND	Main supply ground return from IF/TX
16	NOT USED	

6.6.15 Rear Panel Interface

This interface provides diagnostic signals and remote access to the fault signal.

Table 5 Rear panel interface connector (8 pin Weidmuller at rear, 0.100 single row at PCB)

Pin	Name	Description
1	VBATT	+12V
2	GND	GND
3	AGC	AGC voltage
4	CAL	Calibration pulse, requests next test generator step
5	RX	High when RX LED on
6	PABIAS	PA Bias (leveling) voltage
7	\FAULT	Fault relay connection to GND
8	\TXDEF	Transmit defeat input, connect to GND to defeat

6.6.16 Software Operation

This section briefly explains the control units software operation, or "thought process".

6.6.16.1 Initialization

Upon application of power or actuation of the manual reset, the microcontroller remains idle as its main clock oscillator stabilizes. After that, all I/O ports are configures and set to safe values. The internal timer and serial communications peripherals are initialized and any pending interrupts are cleared. The MCU then performs a brief internal self check and then checks for presence of the external EEPROM (nonvolatile memory). It then checks if the EEPROM has been previously initialized. If initialized, the MCU obtains operating parameters and settings from the EEPROM and stores them in RAM. Otherwise, the EEPROM is initialized and filled with default settings from internal ROM.

The A/D and PWM subsystems are then started and allowed to stabilize. The hardware watchdog function is also initialized.

If the EEPROM indicates that system calibration has occurred , then normal operation begins. Otherwise, the unit will remain in the "Uncalibrated fault state and await factory calibration.

When computer power up is complete, all panel LEDs light momentarily for testing purposes, the software revision is displayed briefly, and operation begins. The interrupt driven AGC, Transmit and fault monitor processes are initialized and spawned, and control is passed on to the main loop. User menu features are now available.

6.6.16.2 Watchdog

Because an OFR may need to operate for several years without human interaction, special hardware is used to ensure that operation continues even if the microcontroller encounters a software failure. As part of normal operation in the main program loop, the microcontroller periodically writes to a specific register that automatically counts down to zero. If due to program operation disruption, perhaps caused by static

electricity, a power surge, or even a hidden software defect, the main operating program does not attend to this "watchdog" or deadman function within the specified time, the hardware automatically initiates a reset, and normal operation will resume if no permanent hardware damage has occurred. If the watchdog restarts the MCU, then a fault is momentarily triggered.

6.6.16.3 Main Loop

The OFR operating software controls several internal functions simultaneously by use of a simple multi-tasking software structure. The main operating module searches for user keypresses and responds in accordance with required user interface flow as described earlier. System I/O is adjusted in real time as the user manipulates adjustable settings. The main loop also updates LEDs and the LCD display, as well as updating the EERPOM upon request by other processes.

Since user interface operations are infrequent and slow-moving, the main loop operates at the lowest priority level and can be interrupted by more hardware-related processes.

The main loop operates as a state machine which is driven by user inputs. If no user inputs occur, then it serves as a slave task to the other processes.

The main loop suspends normal operations and transfers to separate state machines when self-calibration functions are executed. The other processes continue to operate as before.

6.6.16.4 AGC Control Process

The AGC, or IF control process is driven by an internal 500 microsecond timer interrupt. The AGC system is monitored at this rate. This guarantees adequate response time to new received signals.

The AGC control process monitors the AGC voltage and determines if it is above or below the receive threshold and keys the transmitter on or off as required. It calculates the necessary hysteresis factors and converts voltages to dBm levels. The current AGC setting is stored in a register available to the main loop process so that it can update the LCD to show current signal strength as required. It should be noted that as a result of this software architecture, actual hardware operation is much faster than what the LCD is indicating. If the OFR gets busy attending to AGC or power amplifier control, LCD updates are deferred until the work is done. Any such delays are generally imperceptible to the user.

6.6.16.5 Transmit Power Leveling Process

Within a second 4 ms usec timer interrupt, at a lower priority to the AGC control loop, the transmitter control process performs its tasks. Forward power is sampled and compared to the current user command level. The TXLEVEL PWM is updated up or down to bring the transmit power within range if required. This process includes an autocorrelation digital filtering algorithm that ensures that the transmit power leveling loop remains stable and does not try to update the PWM voltage faster than half the PWM cycle rate.

The transmit leveling loop operates on a state-machine principle.

6.6.16.6 Fault Monitor Process

To ensure the OFR hardware is protected from dangerous fault conditions, the fault monitor process runs on a 500 usec interrupt. All internal states related to possible faults are checked 500,000 times per second. Some fault states take longer to be detected because the A/D converter has a minimum cycle time of 16

microseconds. It can be safely said that fault detection will reliably occur within 50 microseconds. This ensures that the circuitry can be protected form any serious fault before permanent damage occurs.

6.6.16.7 Serial Communications Process

Any serial date activity on the UART is subject to its own interrupt. Commands are queued and passed on to the main loop to ensure serial communications overhead does not disrupt vital functions.

6.7 Power Supplies

Two compact open frame switchmode power supplies are used to convert AC mains power to +12VDC and +24 VDC. The supplies have maximum current ratings of 1.2 and 0.6 A respectively. These supplies are UL and CSA recognized. They include full thermal and short circuit protection. A rear panel fuse is used to limit 115 VAC input current in case of a PSU or mains wiring fault.

These supplies are purchased assemblies that should be replaced at the complete module level. No detailed schematics or component layouts are provided. There are no alignment points in these circuits.

7 Service

7.1 Problem Determination/Performance Tests

THIS SUBSECTION NOT INCLUDED IN PRELIMINARY VERSION

7.2 Service Menu

The service menu contains functions used during factory calibration and certain service procedures. Use of these functions requires use of an HP8920A radiocommunication analyzer with specific proprietary Kaval software and interface kit. These functions are not required for normal field operation or setup.

Transmit power and AGC calibration require that the radiocommunication analyzer be connected to the RF output or RF input respectively and that the appropriate interface cable be connected between the OFR rear panel interface connector and the radiocommunication analyzer microphone jack. This interface cable passes digital signaling between the OFR and test set. The radiocommunication analyzer must be running Kaval OFR service software. Details are provided in the documentation accompanying the calibration software kit.

7.2.1 Entering Service Menu

The service menu is called up by pressing the menu button while holding down both the up and down keys.

7.2.2 Calibrate Transmitter Power

Tx Pwr Cal: YES

This function sets the target forward power detector voltages used by the control unit as target setpoints for the 10 available power output levels.

If the OFR is in an uncalibrated state, the display will default to "Yes" when the transmit calibration function is called up. Pressing the menu key starts the operation. If the unit has already been calibrated, the display defaults to "No" and the state must be toggled using the up/down keys followed by actuation of the menu key. An LCD message indicates successful completion of the operation. During calibration, LCD messages indicate progress and the particular power level being calibrated.

When started, the radiocommunications analyzer first waits a 15 second warm-up period while the OFR energizes its transmitter at a low power level. After this warm-up, the radiocomm analyzer outputs pulses to the OFR requesting increased output power until the maximum rated power of +30 dBm is reached. The process aborts if no change in out put power occurs after 10 pulses, or if the final output power is not reachable.

After reaching maximum power, the radiocomm analyzer requests lower power levels and the OFR ramps to each 1 dBm setting. When the target power level is reached, the radiocomm analyzer outputs a confirmation pulse. Power levels between +20 and +30 dBm are calibrated in this manner.

Calibration accuracy is +/- 1.5 dBm.

During the transmitter alignment, the OFR switches on an internal signal source so that no external RF input need be applied. The RF input should be terminated by a 50 Ohm load.

7.2.3 IF Output Level

```
AGC Align:   YES
```

This operation requires no external equipment. With a –60 dBm input carrier applied at the operating frequency, the service technician adjusts R53 on the IF/Transmitter to make the AGC output level match the level of the internal test oscillator used in transmitter calibration. The LCD display shows the difference between the current IF level and the target level. R53 is adjusted to yield 0 on the LCD display. The user must manually exit the function when done by pressing the menu button.

This function can only be performed after transmit calibration is completed.

7.2.4 Calibrate AGC (RSSI)

```
AGC Cal:     YES
```

After transmitter and IF level have been calibrated, the external radiocomm analyzer is used to calibrate AGC voltages against actual dBm levels. The radiocomm analyzer is connected to the RF input, and the RF output must be terminated by a 50 Ohm load.

This function is called up in a similar manner to transmitter calibration.

Once initiated, the radiocomm analyzer applies RF input signals to the OFR input. The OFR reads the resulting AGC voltage and stores it in memory for the level currently being received. When the reading is complete, the OFR signals the radiocomm analyzer to increase the input level by one dB. The system sequences through all 1 dB steps from –95 dBm to –20 dBm.

When the AGC calibration is complete, the OFR then performs an internal self calibration of the AGCLIM voltage used for AGC clamping.

The LCD display indicates successful completion of AGC calibration. At this time, any "Uncalibrated!" fault message will be cleared and normal OFR operation can begin.

7.2.5 Special Calibration Functions

The following settings should not be adjusted except at the instruction of Kaval service technicians. These settings default to the required setpoints during factory setup.

7.2.6 Set PA Temperature Limit

```
PA Max Temp:  128
```

The internal threshold for temperature fault detection can be manually set. The LCD display indicates a value between 0 and 255, with 0 corresponding to the lowest temperature, and 255 corresponding to the highest. 128 corresponds to 90C. The digits do not represent a linear temperature curve. This function

can be used to clear a spurious temperature fault detection to allow continued OFR operation until a possible faulty temperature sensor can be replaced.

This function should normally e set to 128 for the OFR-P300F

7.2.7 Set PA Maximum Current

```
PA Max Curr:  100
```

This function adjusts the trigger point for PA overcurrent detection. It should normally be set to 100. Allowable entries range from 0 to 255. 255 corresponds to zero current and 0 corresponds to maximum measurable current of 1A.

7.2.8 Set PA Minimum Current

```
PA Min Curr:  237
```

This function sets the PA undercurrent fault threshold. A 0 to 255 range of entries is allowed. Higher number correspond to lower currents on a scale identical to that for maximum current setting.

7.2.9 Set Minimum 24V Supply Voltage.

```
Min Volt:     100
```

This function allows adjustment of the trigger level for detection of failure of the 24V PA supply.

7.2.10 Set Maximum Reverse Power

```
Max Rev Pwr:  153
```

This function sets an absolute limit for reverse power above which a fault will be triggered.

7.2.11 Set Defaults

```
SetDefaults:  NO
```

This function sets all calibration functions to a safe set of factory programmed values that, although not necessarily within full specification, will allow minimal operation. The function should be toggled to "Yes" followed by pressing the Menu button.

7.2.12 Exit Factory Menu

```
Exit?         NO
```