6.5.2.1 Crystal Filter

PT1 implements the necessary frequency selectivity of the system. The 1dB passband is approximately 36 kHz with rejection of more than 40 dB at adjacent channels. Group delay is less than 55 microseconds.

At the filter input, R2 and R1 convert the signal impedance to 3kilohms which is required for proper filter match. This network has a loss of about 18 dB. Due to this very high impedance and the large amount of gain in the IF chain (65 dB), the underside of the PCB requires a metal shield under the filter.

Because this filter terminal impedance is slightly capacitive, the input and output must be matched using LC resonators resonant at the passband frequency of 21.4 MHz.

6.5.2.2 Variable Gain Amplifier

The IF filter output is fed to the variable gain amplifier stage. Q1 is a dual gate MOSFET which operates comfortably at the crystal filter impedance at its input. R3 provides input match at gate 1, the RF input.

Gate 2 is used for gain control. The DC voltage at gate two is generated by the ACG control loop. R4 and C6 decouple RF signals and also form a tuned pole in the 4^{th} order control loop. Higher voltages correspond to higher gains, and occur when lower RF input levels occur. Therefore, higher AGC voltages correspond to lower input levels. AGC voltage range at gate two range from 1V to about 5V providing almost 80 dB of gain control range.

Because the gate 2 voltage needs to go below the source voltage for maximum attenuation, a local DC pseudo-ground is generated by Q2. The source voltage is maintained at about 2.1 VDC. The source is RF decoupled by C3.

L2 provides bias to the drain and with C8 and L3, provide RF decoupling.

The gain of the variable gain amplifier ranges from +27 dB to a minimum of –45 dB.

C2 resonates with L2 and the output capacitance of Q1 to provide a gain peak at 21.4 MHz.

It should be noted that the RF impedances around this amplifier are so high that it is impossible to probe signals directly without seriously disrupting the circuit.

6.5.2.3 First IF Amplifier

Q4 is another dual gate MOSFET operated in a fixed gain configuration. Its gain is approximately 30 dB and this stage has been biased for superior intercept point.

As with the preceding stage, the output is LC resonant (L2 and C7), and of high impedance (3.3 kilohms).

R15 and R18 apply fixed gain bias to gate 2.

6.5.2.4 Emitter Follower

Q5 is used to impedance convert the output of Q4 to approximately 50 Ohms so as to effectively drive the following stage, and to bring impedances down to manageable levels to avoid radiatively induced self-oscillation.

6.5.2.5 Second IF Amplifier

Q3 is a standard common-emitter amplifier with a high intercept point. R13 and R12 provide base bias and in parallel with the R-pi of Q3 form a relatively resistive input match. R13 also provides negative feedback for stabilization. R8 provides additional negative feedback. This stage has approximately 25 dB of gain. Its output is fed through a diode switch to the IF output at a level of approximately –10 dBm. In-band intermodulation products are –50 dBc at this point. Output intercept point is +20 dBm for this stage. The same output is also connected to the AGC detector preamplifier for further amplification

6.5.2.6 Test Oscillator

Q9 (PNP) is a 21.4 MHz Colpitts oscillator which is switched-in instead of the IF output for test and automatic alignment purposes. Y6 is a crystal used to stabilize the frequency at 21.4 MHz. When OSCEN is high, inverter Q8 draws current through R139, turning the oscillator on by applying base bias.

L5 and C29 couple the oscillator signal to the output and form a lowpass filter to eliminate harmonics. The filter corner is below the operating frequency deliberately so as to attenuate the signal to the desired –10 dBm level.

6.5.2.7 Diode Switch

D1 and the dual diode D2 are used to switch between the normal IF output signal and the 21.4 MHz test oscillator signal. When OSCEN is high, Q8 saturates. This draws current through R33 which turns on D1. D1 shunts the IF output signal into the RF load presented by R33 to ensure stable operation of the preceding amplifier stage, and to maximize switch isolation. Q8 supplies bias to Q9 which, when on, supplies current through L5 to turn on the top half of D2 when the oscillator is selected. D2 conducts oscillator RF to the output. D2's lower half is reverse biased by the lower voltage at the anode of D1.

When OSCEN is low, D! and the top half of D2 are off and R30, R29 and R25 forward bias the lower half of D2 to allow IF signal to reach the output. The switch has a loss of less than 1 dB and an isolation of over 40 dB.

6.5.2.8 AGC Detector Preamplifier

A –10 dBm level is insufficient to drive a simple diode detector directly, for this reason, a further amplifier stage is added after the second IF amplifier. Q7 provides about 15 dB of additional RF gain. Its configuration is similar to the second IF amplifier. The output of Q7 is the highest RF level in the circuit, and must be carefully shielded from the input. A second shield canon the top of the PCB is used for this.

6.5.2.9 Peak Detector

The peak detector formed by Q2, R21 and C21 half wave rectifies the amplified IF output signal to produce a DC control voltage. As RF level increases, so does the DC output voltage. After integration filtering and linearization, it is applied to Gate two of the variable gain amplifier Q1 with inverted signal sense. As detected voltage increases, the gate voltage decreases. This decreases RF chain gain and stabilizes output level at –10 dBm. Q6 is used as a conventional emitter-follower peak detector. Positive signal excursions at its input result in charge being dumped into C21, the detector filter capacitor. With R21, it has a basic RC response pole well outside the loop bandwidth.

R23 and C22 add the second significant pole in the AGC loop and pass filtered detector output to the integrator.

6.5.2.10 AGC Loop Integrator

U3C forms a classical pure inverting integrator. It adds or removes charge from C36, the integration capacitor to try and bring the voltages at the inverting and non-inverting inputs to the same level, thus stabilizing the loop once the output target RF level has been reached. The integrator ads a third pole to the 4th order loop filter function.

The IF target level is set by potentiometer R53. It is adjusted while observing the output level at TP9 to achieve –10 dBm.

R59 and R60 set the integrator gains for positive going input signals (attack) and falling signals (decay). For falling signals, D5 conducts thus putting R59 in parallel with R60 to provide additional integrator current for decay. Although the input resistance for decay is less than that for attack, attack is still faster because the input error function, or voltage offset between inverting and non-inverting signals, is greater for positive going signals. The IF level setpoint voltage at pin 5 of U3C is closer to ground than the positive rail. Because of this, when the detector voltage falls to ground, the current through R60 is less than when the input signal saturates at the positive rail.

R60 is adjusted while observing the output signal envelope (or AGC voltage), to obtain close to critically damped loop response. The pole formed by R60 and C36 is dominant in the loop response and sets the damping factor. Underdamped (resistance too low) response results in IF level overshoot and possible saturation of the power amplifier during attack. Excessive resistance results in overdamped response in which case attack time is too slow. The circuit is designed for an attack time of about 2ms. When added to the transmitter ramp time of 1ms, we achieve the specified 3 ms attack time for the system.

The output of the integrator is further filtered by an RC network formed by R64 and C37. These parts provide the fourth pole in the loop response.

6.5.2.11 AGC Clamp

A unique circuit in this design is implemented by U3D and D6. This circuit clamps the positive excursion of the AGC voltage to hardware limit it to a user specified gain setting. This prevents the AGC from commanding gains beyond what the system antenna isolation can allow. A voltage, AGCLIM, is generated by the control unit. This voltage corresponds to an AGC gain setting that must not be exceeded, generally corresponding to an input RF level 10 dB above the self-oscillation margin.

In a steady state condition with AGC gain below the AGC limit threshold, the voltage at the inverting input of U3D (pin 9) is below that of the non-inverting input (pin 10). The output of the opamp is then driven to the positive rail, and D6 is reverse biased.

As the AGC voltage at TP13 rises and brings the inverting input to the same level as the non-inverting, the opamp output will swing low and turn on D6. D6 will clamp the AGC voltage at the level set at AGCLIM and prevent it from increasing.

By placing the clamp diode within the opamp feedback loop, we avoid having any net voltage offset in the clamp.

C5 stabilizes the loop when the clamp is in effect to prevent oscillations arising from nonunilateral loop gain when the clamp is on the verge of operating.

When AGCLIM is set to maximum voltage, the clamp can be effectively defeated.

It is important to not that when the clamp is in effect, the AGC voltage cannot rise above a fixed level. For this reason, it is impossible to get RSSI information for signals that are below the AGC limit threshold. Thus, AGCLIM acts as an input sensitivity control.

6.5.2.12 AGC Buffer Amplifier

U3E is used to condition the AGC voltage which swings between about 1.5V and 8V at TP13, to a range of 0 to 5V which is compatible with the control unit A/D input voltage range. R54 and R51 form a voltage divider that reduces maximum voltage from about 8V to about 5V. The network R97 and R98 provide a pseudo-ground at about 4.8V.

The DC gain of this buffer is about 1.5.

6.5.2.13 AGC Linearizer

Because the transfer function of the variable gain amplifier Q1 is highly nonlinear, the loop gain varies by an order of magnitude over the full operating range. The different slopes at different gain settings result in wide fluctuations in loop gain, and hence, damping factor. Gain settings that are adequate at some gain settings may result in loop oscillation at other settings. To achieve stability with the required extremely fast attack time, a linearizer was needed in the control loop.

A stepwise approximation of the roughly exponential gate 2 voltage to transconductance transfer function of Q1 was implemented using U3B. The networks R48/R49 and R47/R52 set "corner" voltages at which additional resistors are switched in parallel at the inverting amplifier input.

At low voltages, D4 and D3 are off and R55, R57, R47, R48, R49, and R52 are out of the circuit. U3B, in such case acts as a voltage follower with a voltage divider at input, resulting in a DC gain of approximately 0.27. As the voltage rises at the output to about 1.22V, D4 starts to conduct, adding the resistance consisting of R57 in series with the parallel combination of R48 and R49, to the inverting input. The gain is now the original follower gain plus the ratio of R61 to the resistance added to the inverting input, or about 0.81. Due to the high impedances used, the onset of diode conduction is gradual, leading to a very smooth linearizer response without obvious corners.

Similar to the first gain variation step, at about 1.4355V, D3 begins to conduct, adding more admittance at the inverting terminal, increasing gain to about 6.2.

The final result is a DC transfer function with increasing slope with increasing input voltage. This is the inverse to the gain vs. voltage function of the variable gain amplifier.

An added benefit of the linearizer is that the AGC voltage fed to the control unit can remain log-linear as an RSSI indication.

6.5.2.14 AGC Loop Filtering

4^{th} order loop response was required in this design. The four lowpass rolloff networks are R4/C6, R23/C22, R60/C36 and R64/C37. Such a high order loop response was necessary to allow sufficiently fast attack, while adequately filtering any "beat frequencies" arising from the close carrier spacing. We require strong suppression of loop response at 10 kHz. If the loop has any appreciable gain at 10 kHz, then the IF will be AM modulated by the difference frequency between the 4 carriers in the passband which are spaced 10 kHz apart. This sort of AM would result in sidebands at 10 kHz intervals that look exactly like 3^{rd} order and 5^{th} order intermodulation products. If such sidebands are observed at the IF output, they are not necessarily a sign of insufficient intercept point, but are rather the result of the AGC loop acting on the

multicarrier AM envelope arising from the combination of sine waves. Adjustment of R60 can minimize these sidebands to –50 dBc.

While 10 kHz response is to be minimized, the loop still requires a response corner frequency of about 5 kHz in order that it can respond quickly enough to allow a 1 ms attack time.

6.5.3 Upconverter/Exciter

The upconverter/exciter subsystem takes the IF output signal, mixes it up to the final 940.225 MHz frequency and amplifies it to a level sufficient to drive the final output power amplifier module. Along the way, the various mixer image products and local oscillator signals must be filtered to prevent spurious emissions. At each step, sufficient intercept point must be maintained to ensure intermodulation is not introduced.

Most of the upconverter runs off the 9.6V supply. It consumes about 400 mA.

6.5.3.1 IF Attenuator

R26, R27 and R28 form a 12.5 dB pi attenuator which conditions the IF output signal to a level suitable for the mixer's linearity requirements, and to provide a good lossy 50 Ohm match to minimize mixer spurious products.

6.5.3.2 First Upconversion Mixer

The first mixer mixes the 21.4 MHz IF signal with the 229.7063 MHz L.O. signal to output the desired 251.1063 MHz second IF frequency at a level of approximately –30.5 dBm. Mixer loss is about 8 dB.

6.5.3.3 First Upconversion IF Strip

The local oscillator and image frequency resulting from the first mixer operation are filtered by two two pole helical filters FL1 and FL3 before being applied to the second mixer. These filters are hand-modified filters with 1.25 turns removed from each filter bobbin.

An MMIC internally matched 50 Ohm gain block, (U5, ERA-4SM) is used to compensate for some first mixer and helical filter losses to result in the input signal being applied to the second mixer being approximately –23 dBm.

6.5.3.4 Second Upconversion Mixer

The second upconverter mixer U7, identical to the first mixer, uses tripled L.O. signal at 689.1188 MHz to convert the 251.1063 MHz first IF frequency to the final transmit frequency of 940.225 MHz. Conversion loss is about 8 dB resulting in an output level of –31 dBm.

6.5.3.5 L.O Buffer

The local oscillator signal is applied to the upconverter module at about +6 dBm. It is attenuated by the Pi network R41-R43 by 9 dB. It is then buffered by U1, to a level of approximately +10 dBm. A resistive

splitter applies some of the output to the first mixer, U2, at a level of about +7 dBm. The remainder of the energy goes to the LO tripler.

6.5.3.6 L.O. Tripler

Q10 is operated in class C mode with L7 acting as the base ballast. The circuit match at input is optimized for 230 MHz. The output match, L8, C44, L9 and C46 are resonant at three times that frequency, or 689.1188 MHz. The tripler output is about +3 dBm. It is important to note that overdrive of the tripler can lead to reduced output, so careful control of L.O. output is necessary.

6.5.3.7 L.O. Filter and Buffer

FL2, a three pole helical filter, selects the desired third harmonic of the L.O. and suppresses other products. The filter has a loss of about 6 dB. The filter output signal is amplifier by another MAV-11 MMIC amplifier to the required mixer drive level of +7 dBm and applied to U7.

6.5.3.8 Variable Attenuator

U11 is a Gallium Arsenide MMIC which is used as a voltage variable attenuator. The attenuation control voltage is sourced from the control unit and applied to the voltage control pin after being ranged from a 5V scale to a 3.3V scale suitable for this device. Higher voltages at the control pin of the attenuator correspond to higher attenuation, and lower transmitter output power. The active range of the control voltage is about 1 to three volts which results in an attenuation range of 1.5 to 45 dB.

The attenuator must run at a voltage less than 5VDC. D7 is used as a local voltage regulator for the attenuator supply.

6.5.3.9 Exciter Chain

The attenuator output is amplified by three identical MMIC gain blocks, U10, U9, U8, all ERA-4SM. Interspersed within this chain are two three pole dielectric filters that remove L.O. and image products. The overall gain of the exciter chain is 32.5 dB. Final exciter output level is approximately 0 to +2 dBm with an output intercept point of +32.5 dBm. Due to the high amount of gain in the exciter and power amplifier tandem combination (>62 dB), it is imperative that the PA output be well shielded from the exciter input. It is impossible to energize this entire chain unshielded without encountering self-oscillation. An aluminum bar with EMI gasketing is used for this purpose.

6.5.3.10 Exciter Power Switch

Because the power amplifier must be keyed on with a timed envelope ramp, it is important that the RF input to the PA be at full power before it is energized. For this reason, the exciter chain, which consumes about 35 mA per stage, must be energized before the PA. The PREEN signal from the control unit turns on the exciter before the transmitter is keyed. Q14 is an RTL inverter which applies base bias to Q13 which acts as a saturating power switch that connects the exciter to the 9.6V supply. The exciter must be keyed off when the transmitter is de-energized to ensure that no output signal leaks past the PA module.

6.5.4 Power Amplifier

6.5.5 Power Amplifier

Final linear transmit amplification is provided by Motorola hybrid amplifier module. This is an LDMOS class AB linear device rated at 16W. This unit must be operated well below its rated power to achieve the necessary intermodulation performance, which does not necessarily follow normal linear amplifier mathematics.

U13, the final power amplifier is supplied with 24 VDC. It consumes approximately 450 mA when producing full power. Its overall gain is typically 30 dB, resulting in a final output power level before filtering of about +31.5 dBm

The power amplifier is mounted perpendicular to the printed circuit board and heatsinked through the module housing cover into an extruded aluminum heatsink. Total device dissipation is about 11W. The heatsink is rated for continuous operation in ambients up to 60C. At extreme temperatures, the heatsink may be too hot to touch, about 90C.

6.5.6 Directional Coupler

A microstrip edge coupler with approximately 20 dB coupling is used to sense forward power for transmitter leveling, and reverse power for load VSWR detection. Diode detectors in the coupled arm provide 50 Ohm termination and detect RF power traveling in each direction.

6.5.7 RF Detectors

D8 is the forward power detector. R116 coupled with the resonant circuit C90/L17 provide a good 50 Ohm match to the coupler line. D8 rectifies the RF signal and presents a relatively constant DC voltage proportional to average power across C91.

D9 similarly detects reverse power

These diodes have normal temperature dependence. At higher temperatures, they will read higher voltages causing transmitter power to back down slightly.

6.5.8 Detector Buffers

U4D and U4E are non-inverting DC amplifiers that buffer the forward and reverse detector voltages respectively. The forward detector amp has a gain of 4.5 and the reverse detector has a gain of about 6.

The control unit monitors the forward power signal and adjusts the variable attenuator control signal TXLEVEL to maintain constant PFWD over temperature, system gain and load variations. The control unit is factory calibrated using an automated routine to make an EEPROM table of required PFWD voltages for every power output level, at 1 dB intervals between +20 and +30 dBm. The software uses these table entries as the target points for a closed loop power control algorithm.

The control unit calculates the ratio between reverse power and forward power to determine if the load VSWR is indicating an antenna failure. In such case, a fault is signaled, and the PA is turned off to prevent possible system self-oscillation. The PA is sufficiently rugged to survive an open or shorted load, but may draw excessive current if it goes into self-oscillation with the exciter chain after the attenuator.

6.5.9 Harmonic Filter

A dual PI lowpass filter is used to reduce output harmonics by at least 60 dB. The series inductive elements are printed microstrip transmission lines. High Q porcelain capacitors are used in the filter to minimize losses. Total losses in the directional coupler and filter are about 1.2 dB. The final output is fed to a type N female connector at the rear panel.

6.5.10 Transmit Ramp Generator and Bias Control

The transmitter is keyed on by the TXEN signal from the control unit. TXEN is asserted high when the control unit detects input RF above the user programmed receive threshold. TXEN makes Q12 conduct which discharges C50 through R87 and turns Q11 on. Collector base capacitor C50 acts as an integrator resulting in a roughly constant voltage ramp with a risetime of 1 ms. The voltage at the collector of Q11 is a linear ramp from 0 to +24 V. An adjustable resistor divider consisting of R90 and R93 reduces the PA bias voltage to about 14.5VDC, which is near the optimum bias point for best intermod. R90 must be adjusted during a multicarrier test for best intermod.

6.5.11 Current Sense

The power amplifier supply current is monitored by the control unit to both detect a power amplifier failure, or a fault condition that results in excessive current draw, such as a bias circuit failure or self-oscillation.

R73 is a high wattage resistor in the final stage supply line that is used for current sensing. U4C is a differential amplifier that measures the voltage across R73 to determine current. A normal supply draw results in a voltage of slightly less than half a volt across the sense resistor.

The differential amplifier ranges the current to voltage conversion to yield an output voltage that swings from +5V to zero as current increases from zero to up to 1A.

R82 is used to set the differential amplifier quiescent setting to yield 0V output for a sense current of 1A. A test resistor of 24 Ohms can be used in lieu of the power module for this alignment.

The control unit senses both over and under current conditions and signals the appropriate faults.

6.5.12 Temperature Sense

A PTC thermistor, U12 changes resistance with temperature. Resistance goes up with temperature with greatest slope at about 90C, the desired fault trigger point. R72 is adjusted to yield 2.5V on TEMP for a temperature of 90C, or a thermistor resistance of 100K.

The control unit shuts down the PA if the temperature limit (programmable) is exceeded.

6.6 Control Unit

6.6.1 General

The control unit is the "brains" of the OFR. It interprets user inputs and internal states of the device and controls all internal functions, as well as user front panel indicator lights and LCD display. The control unit also contains voltage regulators for the internal 12V and 9.6V supplies.

The control unit centers about an OTP (One Time Programmable) single chip microcontroller (Motorola MC68HC705B5), operating at a clock frequency of 4 MHz. This microcontroller implements the user interface of the OFR. All program settings and calibration information is stored in a serial nonvolatile electrically erasable ROM. Such information is retained during power outages up to 10 years. An optional RS-232 interface can be installed to allow remote control and diagnostics. It is possible the connect this interface to a standard telephone modem.

The control unit monitors internal operations and signals fault conditions by placing a suitable text message on the front panel display, and actuates a relay closure which can be connected to external monitoring apparatus via the rear panel interface connector.

The control unit is mounted at the front of the OFR using a sheet metal bracket with suitable printed nomenclature to designate buttons and lamps.

6.6.2 Power Supply Regulators

+12VDC and +24 VDC are applied at J4. The control unit operates on the 12V supply. It primarily provides a convenient feedthrough of the +24V supply to the IF/Transmitter final stages. However, the +24V supply is monitored by an A/D converter to detect failure of the +24V power supply module. The PWM D/A buffers are also powered from +24V for maximum dynamic range.

F1 limits current in the +12VDC line to 2A. L1, C2 and C3 provide filtering of switching noise on the power supply input which may disrupt sensitive RF circuitry and cause spurious sidebands in the output RF signal.

U5 produces a regulated +5V supply that is used to power the digital circuitry on in the control unit only. High current loads such as the

U4, an adjustable low-dropout linear regulator, produces a regulated +9.6V supply that is used to power most of the RF circuitry of the OFR.

J5 feeds +9.6V to the front end and local oscillator. J2 provides +9.6V and +24V to the IF/Transmitter (along with other signals).

6.6.3 Microcontroller

The central microcontroller, U1, is a Motorola MC68HC705B5. It contains 6k bytes of program ROM, 176 bytes of RAM, parallel I/O, internal timer, serial communications interface, 8 channel A/D converter, two pulse width modulation D/A converters and internal self-monitoring hardware. It is installed in a socket which allows for field-upgrades of software.

Table 2: MCU Port Assignments (ports not listed are not used)

PORT	PIN	SIGNAL	I/O	DESCRIPTION
PA0	31	DB1	I/O	LCD data bus
PA1	30	DB1	I/O	LCD data bus
PA2	29	DB2	I/O	LCD data bus
PA3	28	DB3	I/O	LCD data bus
PA4	27	DB4	I/O	LCD data bus
PA5	26	DB5	I/O	LCD data bus

PA6	25	DB6	I/O	LCD data bus
PA7	24	DB7	I/O	LCD data bus
PB0	39	PREEN	O	Enable preamplifier, active high
PB1	38	TXEN	O	Enable final stage, active high
PB2	37	\FAULT	O	Turn on fault LED and release relay, active low
PB3	36	TXLED	O	Transmit LED, on when current and RF detected, active high
PB4	35	RXLED	O	Receive LED, on when input signal above trigger, active high
PB5	34	RS	O	LCD Register select
PB6	33	R/W	O	LCD Read/Write
PB7	32	E	O	LCD data strobe
PC0	49	\FCN	I	Function button, active low
PC1	48	\DOWN	I	Down button, active low
PC2	47	\UP	I	Up button, active low
PC3	46	SPARE2	?	Spare I/O, possibly for extra button
PC4	45	CAL	(I)/O	Rear panel strobe line for calibration process. Pos. pulse requests next level
PC5	44	OSCEN	O	Enable IF test oscillator, active high
PC6	43	ECLK	O	EEPROM clock
PC7	42	EDAT	I/O	EEPROM DATA
AN0	14	PFWD	AI	Forward power detect 0V= no power, 5V=full scale, 2.5V=nominal
AN1	13	PREV	AI	Reverse Power detect 0V=no power, 5V=full scale, 2.5V=alarm threshold
AN2	12	AGC	AI	AGC Voltage 0V=max input signal, 5V=min input signal (-95 dBm)
AN3	11	PATEMP	AI	PA thermal sense. 2.5V = danger point.
AN4	9	TXCURR	AI	PA current sense. 5V=no current, 0V=full scale, 2.5=nominal
AN5	5	\EXFLT	AI	External fault force. <2.0V=fault 1V hysteresis
AN6	4	\TXDEF	AI	Transmit defeat. <2.0V commands transmit defeat 1V hysteresis
AN7	3	24V	AI	24V supply monitor. 5V=32V full scale
PLMA	20	PABIAS	AO	PA gate bias. 0V=no bias, 5V=18.4Vbias. 15 nominal
PLMB	21	AGCLIM	AO	AGC Limit. 0V =least sensitive, 5V=most sensitive
TCMP1	2	POWER	O	Power LED, timer clocks or forces high after all initialization complete.
TDO	52	TDO	O	Serial data out to RS-232
RDI	50	RDI	O	Serial data from RS-232

6.6.4 Clock

The microcontroller reference oscillator is stabilized using a 4 MHz ceramic resonator, Y1. C20, C21 and R15 provide proper load capacitance and guaranteed startup. This clock is divided by two inside the MCU, to provide an internal bus speed of 2.0 MHz.