Active Device List and Theory of Operation:

Reference Designator	Device Type	Function
U6,10	comparator	DC switching
Q1,3	P-channel FET	DC switching
U1,7	AGC IC	audio level control
U4,9	op-amp	audio gain stage
D1,3	silicon diode	audio clipper
U2,8	op-amp	audio low pass filter
U3,11	PLL IC	audio subcarrier PLL controller
D2,4	varactor diode	audio subcarrier VCO tuning
D11,12	silicon diode	audio subcarrier limiting
U6,12	CMOS gate	audio subcarrier amplifier
U24	regulator IC	dc regulator
Q5,6,7,10	P-channel FET	DC switching
Q9,11	N-channel FET	DC switching
Q12	PNP silicon transistor	DC switching
D17	voltage reference IC	voltage rerference
U21	op-amp	voltage clamp circuit
D15,19,18,9,20,16	schottky diode	DC switching
D7,13	schottky diode	DC switching
U20	switching regulator IC	step down regulator controller
U25	switching regulator IC	step up regulator controller
D8	silicon diode	DC switching
U13	microprocessor	system controller
U14	CMOS gate	control logic
U18	PLL IC	main carrier PLL controller
U23	video op-amp	video summing amplifier
U19	VCO	main carrier VCO
U17	RF amplifier IC	RF buffer amp
U15	RF amplifier IC	RF driver amp
Q13,14	PNP silicon transistor	driver amp current source
Q8	LDMOS FET	RF power amplifier
U22	CMOS gate	9.600 MHz system clock

Theory of Operation:

The transmitter consists of a primary frequency VCO that is modulated by up to two subcarriers and a processed video signal. The modulated carrier is then amplified prior to transmission.

The two subcarrier circuits are identical and consist of a VCO operating in the range of 6.0 to 7.5 MHz. At system power-up, the subcarrier PLL controllers (and the main carrier PLL controller) are all powered-up and programmed via a common bus. The subcarrier VCOs are activated when a microphone is connected to the unit. The subcarrier VCO output signal is amplified by a CMOS gate and then lowpass filtered before being applied to the video amplifier.

The video input signal is pre-emphasized according to the prescribed standard NTSC curve and applied to the video amplifier. The video amplifier sums the video signal and the audio subcarrier signals together to form a combined modulation signal. This combined modulation signal is then applied to the main carrier VCO via the PLL loop filter.

The main carrier PLL is programmed when the system is powered up. Power to the final amplifier stage is withheld until the carrier PLL attains lock. A fixed attenuator acting as an isolator protects

the phase locked carrier signal from the VCO. The carrier signal is then amplified by two linear gain stages to attain sufficient level to drive the class B power amplifier. The power amplifier consists of a single discrete FET, which is impedance matched with discrete and distributed elements. The output impedance match is lowpass in form and provides the required filtering. RF power control is accomplished by varying the bias voltage on the gate terminal of the final amplifier transistor. The amplified and lowpass filtered carrier signal is connected directly to the chassis mounted antenna connector.