Operational Description

The H25DSS900TX is a 900 MHz, low power, spread spectrum audio surveillance transmitter used for law enforcement applications. The transmitter employs digital modulation with direct sequence spread spectrum on one of three factory-selected channels in the 902-928 MHz range.

The H25DSS900TX has a power output of 50mW to an integral patch antenna built into the housing which meets the requirements of Part 15.203.

Two microphone modes are supported, internal and external. The microphone audio is processed by an amplifier equipped with an automatic gain control (AGC) which may be turned ON or OFF with an external switch. Audio is processed with a continuously variable slope delta-modulation (CVSD) speech coder at a rate of 32 Kbps.

The H25DS900TX is a portable device; DC powered by five AAA batteries, which supply a nominal 7.5 VDC. All critical circuits are regulated.

Intended Use

This device is intended to be used by government law enforcement entities for short-term undercover surveillance operations.

Specifications

Input:	FET-Electret Mic. (internal and external with 24“ cable-auto. switching)
Controls:	Power ON/OFF, AGC ON/OFF
Antenna:	Linear Patch
Power Output:	50 mW
Audio Coder Rate:	32 Kbps
AGC Range	45 dB
Modulation:	Direct Sequence Spread Spectrum
Chip Rate:	704 Kilochips per second; 357.1 Kilochips per second effective
Spreading Ratio:	11 dB
Spreading Code	Proprietary 37-chip code (Factory fixed)
Spurious Radiation	Less than –45 dBc:
Frequencies:	A = 905.5 MHz; B = 915.0 MHz; C = 924.5 MHz (3 Channel capability; single channel factory selected)
Battery:	7.5 VDC with 5 AAA batteries
Battery Life:	3 Hours Minimum
Dimensions:	2.3” X 4.2” X 0.7” (60mm X 105mm X 18mm)
Weight:	8.7 oz (240g) including external microphone and batteries

Description of Circuitry

The active RF circuitry generates a digitally modulated DSSS signal on a single channel in the 902 – 928 MHz band. The heart of the system is an AT90S1200 microprocessor controller IC, U6 and the 14.336 MHz clock which performs many functions including: serial programming a phase locked loop (PLL), U3, which generates the on-channel carrier and chipping the data stream with a spreading function.

Audio enters the transmitter circuit via a biased internal or external electret microphone and is amplified and processed by AGC/limiter hybrid circuit U9. This device acts to compress the audio dynamic range to a level and bandwidth acceptable for the CVSD audio coder IC, U7. Limiter clip level is set by R13. The data stream out of the coder is then sent to the microprocessor.

A buffered 14.336 MHz clock formed by sections of U8, an inverter IC, acts as a clock for micro. The micro. further divides the clock to 1.024 MHz for the CVSD audio coder, U7.

The 32 Kbps data-stream coming out of the CVSD audio coder is sent into PLD where it is “chipped” and sent to the inverter IC for buffering. The buffered data-stream, which is now at a rate of 704 Kcps, is pre-filtered by L4 and L5 in conjunction with C20 and C21 is the modulation for the BPSK generator, U4.

The micro. also “loads” the serial programmed PLL IC, U3, based on internal hardware channel jumpers. Three channels are accommodated with jumper settings.

The on-frequency local oscillator signal is produced by a phase locked VCO in association with D1, a varactor diode. The PLL circuit consists of a serial programmed PLL IC, U3, in conjunction with a VCO IC, U2. The output of the VCO chip is sent to the BPSK generator, U4. The spread spectrum output of the BPSK generator is amplified by U5, a linear amplifier MMIC to the 50 mW peak level. The RF signal is then filtered by FL1, a ceramic dielectric lowpass filter.

Finally, the 900 MHz CW signal, generated by the frequency synthesizer is binary phase shift modulated by the coded and chipped data-stream based on microphone audio and a fixed pseudorandom code also generated by the micro. The resulting wide BPSK signal is then linearly amplified by two microwave monolithic integrated circuits (MMIC’s) and filtered before being connected to the integral antenna.

The transmitter output impedance is 50 Ohms into the patch antenna.

All circuits are regulated by U1, a 5 VDC regulator IC, with the exception of the AGC hybrid, which has its own on-device regulator. D2 and D3 provide Battery polarity protection.