



מעבדות לתקנים בינלאומיים בישראל

APPROVED TO ISO/IEC 17025

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To: Timco Engineering Inc.

From: Shaike Raz

Att: Reviewing Engineer

Reference No: L71720.00

Date: 28 May 2007

Subject: Duty Cycle Plot for WPK 215 FCC ID: GSAWPK250

To Whom it May Concern,

The attached Visonic response concerning the Duty cycle plot is based on an analysis, since implementation of the actual worst case condition for a plot was not practical.

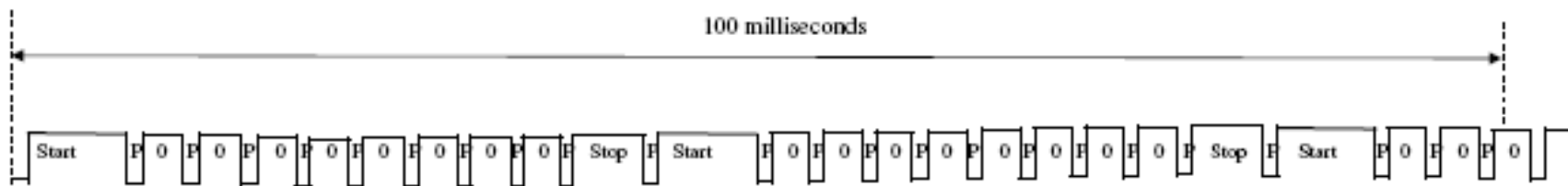
Regards

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WPK 215 transmitter timing

BIT	Transmitter		Bit shape
	Pause (P)	Pulse duration	
"1"	1.0ms	2.0ms	
"0"	1.0ms	3.5ms	
"Stop"	1.0ms	5.5ms	
"Start"	1.0ms	8.0ms	

Maximum duty cycle theoretical message



The maximum duty cycle message has only logical zeros ("0"). In 100 milliseconds period the minimum number of 1 millisecond pause is 23 (23%). Therefore, the maximum theoretical duty cycle is 77%. We declared the duty cycle is <85% in order to have some "spare" margin and be on the safe side during the tests.

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