RA1001 Narrowband PC-Card Radio

Functional Description

The RA1001 is a half-duplex digital packet radio supporting Psion Teklogix' proprietary narrowband wireless networking system. It has the following basic specifications:

- Frequency bands: 403-422MHz, 419-435MHz, 435-451MHz, 450-470MHz, 464-480MHz, 480-496MHz, 496-512MHz
- Output power: 30dBm
- Modulation types and baud rates: 2-FSK (9600, 4800), 4-FSK (19200, 9600)
- Receiver sensitivity (≤1% BER): -112dBm (19200 4-FSK)
- Frequency stepping increment: 6.25kHz, 10kHz, or 12.5kHz
- Power requirements: 5V ±5%, 1A peak, 150mA receive or transmit standby
- Form Factor: PC-Card Type III, cast magnesium enclosure

Receiver:

The receiver is a dual-conversion superheterodyne architecture with a first IF at 45.000 MHz and a second IF at 455kHz. Low-side local oscillators are used at both downconversion stages. The main reference is a 24.000 MHz VCTCXO.

Limiter

Protects LNA and first SAW filter from damage due to large AC signals. Anti-parallel Schottky diode pair.

RF SAW Filters

Surface Acoustic Wave bandpass filter passes desired frequency band and rejects out of band signals including those at the image frequency, f_{RF} – 90MHz. Provide 3.5dB of insertion loss.

LNA

Provides 16dB of RF gain. SiGe HBT technology.

Main TCXO

24.000 MHz Voltage-Controlled, Temperature-Compensated Crystal Oscillator provides main reference for PLLs and digital clocks. ±1.5ppm temperature stability between -30ºC and 60ºC. Produces a 1Vpp output signal into a 10k/10pF load. A digital potentiometer allows trim under DSP firmware control.

Receive Local Oscillator

Consists of the Receive PLL Synthesizer (LMX2316 Integrated Circuit), the Receive VCO, the LO Buffer Amplifier, and a discrete lowpass harmonic filter. Comparison frequency is 12.5kHz or 6.25kHz. Reference is 24.000MHz. Provides a 0dBm local oscillator signal to the first mixer.

Mixer

Downconverts the RF signal to the first IF at 45.000MHz using the Receive Local Oscillator. Provides 6dB of conversion loss. Passive FET type.

IF Amplifier

Provides 10dB of IF gain. SiGe HBT technology.

IF Filter

4-pole crystal filter passes/selects a single channel (15 or 7.5kHz 3dB bandwidth depending on model) at 45.000MHz and rejects off-channel interfering signals including those at the image frequency, 44.090MHz by greater than 70 dBc.

Second Local Oscillator

Voltage-Controller Temperature-Compensated Crystal Oscillator at 44.545000 MHz provides local oscillator signal to the second mixer. 0.6Vpp output signal into a 10k/10pF load.

IF System (SA606 Integrated Circuit)

Contains second mixer, second IF amplifiers, limiter, FM demodulator, and RSSI signal. The 45.000 MHz first IF signal is downconverted to 455kHz by the Second Mixer using the Second Local Oscillator.

The IF amplifiers and limiting amplifier provide 102dB of IF gain.

Balanced FM demodulator recovers original baseband data signal. A digital potentiometer under firmware control provides a tuning voltage to a varactor in the quad tank which allows it to be accurately tuned. The tank is temperature compensated.

Second IF Filters

4-element ceramic filters pass/select a single channel (9kHz or 20kHz 6-dB bandwidth depending on model) at 455kHz and reject off-channel interfering signals.

Receive Audio Lowpass filter

Lowpass filters the recovered data signal at 8kHz and buffers the signal before it passes to the Analog-to-Digital Converter in the Codec.

Codec

TLV320AIC24 Integrated Circuit samples the recovered data signal at a frequency of 76.8 kS/s and a resolution of 16 bits. Also converts the RSSI signal. Controlled by and interfaced with the DSP. Also contains a 16-bit Digital-to-Analog converter which generates a RF Power Amplifier control signal to ramp it from off to full power. The Codec is also used to generate analog test signals.

Transmitter

The transmitter in the RA1001 involves a DDS-driven PLL architecture.

DDS (AD9833 Integrated Circuit)

The Direct Digital Synthesizer produces a 1MHz carrier signal. It's reference clock is a 24.000MHz 5V CMOS clock, which is derived from the main reference TCXO. The DDS contains a sine wave lookup table which is used to digitally construct a phase-continuous sine wave. The rate of phase increment (frequency) is determined by the register value programmed into the DDS by the DSP. 2-FSK and 4-FSK modulation is achieved by varying the applied frequency programming word in accordance with the desired data encoding. Similarly, the desired FM Deviation is achieved by scaling the offset from the nominal carrier frequency accordingly. The final output of the DDS is a current-output 10-bit, 25MS/s DAC. The DDS nominal frequency is varied within about ±80kHz (920kHz to 1080kHz) to allow fine channel stepping while using a relatively high comparison frequency of 1MHz with the transmit PLL.

DDS Filter/Buffer

Reconstruction and harmonic lowpass filter and buffer, allowing a 50Ω load to be driven. Signal level at output is about -3dBm.

72MHz Harmonic Selection Filter

Discrete bandpass filter selects strong 3rd harmonic from the 24.000 MHz square signal. This signal is used as a local oscillator to upconvert the 1MHz DDS modulated carrier signal to 71MHz.

Transmit Mixer

Upconverts 1MHz signal from the DDS to 71MHz using the 72MHz local oscillator signal. Passive diode-ring type. 6dB conversion loss.

Transmit Reference Buffer

Provides 8dB of gain. Signal level at output is about 0dBm. SiGe HBT technology.

Transmit 71MHz SAW Filter

71MHz Surface Acoustic Wave bandpass filter passes desired signal at 71MHz and rejects other unwanted mixer products. 5dB insertion loss. ±80kHz minimum passband width.

Transmit Oscillator

Consists of the Transmit PLL Synthesizer (ADF4116 Integrated Circuit) and the Transmit VCO. Comparison frequency is 1MHz. Reference is 71.000MHz. Generates a modulated RF carrier.

Pre-Drive Amplifier

Provides 18dB of RF gain. +8dBm output signal level. SiGe HBT Technology.

Transmit RF Power Amplifier (RF2117 Integrated Circuit)

Provides 27dB of gain and outputs a +31dBm signal. Output level controlled by the DSP using the Codec to ramp it from off to full power. GaAs HBT Technology.

Transmit Filter

7-pole discrete lowpass filter constructed of high-Q air core inductors and thin film capacitors. Suppresses harmonics generated by the RF Power Amplifier.

Transmit Power Detector

Not used. Signal passes through only.

Temperature Sensor (LM20 Integrated Circuit)

Analog temperature sensor with ±2.5ºC accuracy provides voltage signal to an ADC channel in the Codec. The firmware uses hard-coded lookup tables to implement temperature compensation for the Power Amplifier's drive signal, to provide constant transmitter output power over temperature.

Digital Section

DSP

Digital Signal Processor (TMS320VC5410 Integrated Circuit) controls the receiver and transmitter. It enables power voltage regulators as required, programs the CODEC, PLL Synthesizers, DDS and the Digital Potentiometers and performs baseband modem filtering, symbol timing recovery and encoding/decoding. The DSP communicates with the DDS and the CODEC with its Multichannel Buffered Serial Ports (McBSP). The PLL synthesizers, the Digital Potentiometers and the regulators' control pin are connected to the programmable IO pins of the FPGA. These pins are mapped to the FPGA register space. The DSP control these pins by setting the corresponding bits of the FPGA registers.

Flash Memory

Flash memory provides non-volatile storage of DSP and FPGA firmware and factory calibrated tuning parameters. This design can accept either 4 Mbit flash (M29W400BT, M29W400DT or AM29LV400DT Integrated Circuit) or 8 Mbit flash (M29W800DT, or AM29LV800DT Integrated Circuit).

FPGA

Field Programmable Gate Array (XC2S50 Integrated Circuit) implements PC Card host physical interface and expands the I/O capability of the DSP. It has 128x16 CIS (Card Information Structure) memory space, 4Kx16 common memory space. The DSP has both read and write access to the CIS memory and common memory. The PC Card host has read and write access to the common memory but only read access to the CIS memory. In addition, the FPGA has 2Kx16 register space.

Digital Potentiometer

10 kΩ, 256-position digital potentiometers (AD5204BRU10 Integrated Circuit) provide digital tuning of voltage controlled crystal oscillators and the receive demodulator. The digital potentiometer is programmed by the DSP through the FPGA