PSION TEKLOGIX

7530 ARCHITECTURE
DESIGN DESCRIPTION

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1   SCOPE

This document describes the general architecture of the 7530 handheld computer.

2   GENERAL DESIGN SPECIFICATIONS

The architecture and all electronic components are designed to operate over -30ºC to +70ºC, severe humidity and shock.

3   PROCESSORS

3.1   MAIN PROCESSOR

The main processor is an Intel PXA255 X-Scale device.

3.1.1   Operating Systems Compatibility

WindowsCE

3.1.2   Optimizing System Power Efficiency

High performance RISC processors *a la* PXA255 incur excessive system power consumption when running at maximum clock frequency & actively accessing external SDRAM.   The system is designed to put the CPU into an idle state (and stop all external memory accesses) whenever possible – i.e. whenever the operator is not actively using the handheld.

3.1.3   Memory

3.1.3.1   Synchronous DRAM

The 7530 can support 32MB or 64 MB of SDRAM (32-bit wide format).

3.1.3.2   NAND FLASH

The logic board includes 32MB of NAND FLASH (x 32 format). Additional storage memory may be implemented via a SDIO slot (from 8MB through 64MB) using a 20Mbps SPI-like serial interface. Note that SDIO memory modules cannot support execute-in-place (XIP) functionality, and thus the main DRAM memory must be sufficient to load all necessary applications stored on the MMC module.

3.2   PERIPHERAL CONTROLLER

A Renesas M30624 is used as the internal Peripheral Controller (PCON). In this role this device manages:

- Power system management
- Tracks analog sensors (temperature, light levels, voltages)
- Controls slow or infrequently changing GPIO
- Interfaces to the pistol grip trigger via a Hall effect sensor

- Provides a slow speed diagnostic RS232 UART

This device communicates with the main CPU via a high speed I2C. Functionality has been partitioned so that the messaging requirements between the peripheral controller and the main CPU are minimized (and variable latencies are easily tolerated).

4 REAL-TIME CLOCK

A real-time clock, a Ricoh RV5C386, communicates with the system via an I2C interface.

5 CARDBUS & COMPACT FLASH INTERFACES

The 7530 can support one CardBus and one Compact Flash socket. Only a PCMCIA electrical interface will be supported until an ASIC supporting the CardBus electrical interface is designed.

An FPGA will be used, *pro tem*, until the ASIC is available.

5.1 COMPACT FLASH + SOCKET

The Compact Flash socket is a type II and supports up to 5mm thick cards. This socket is fully CF compliant and includes a cavity at the end of the card for either integrated antenna structures or an internal cable connection.

5.2 CARDBUS SLOT

A double-slot CardBus connector will be provided in the 7530. Only the 'top' slot is connected, providing sufficient space for a type III card (narrow band radio).

6 INTERNAL SCANNERS

6.1 NON-IMAGING SCANNERS

An interface is supplied internally to support various third party barcode scan engines and RFID. These devices may be TTL or USB.

6.2 IMAGING SCANNER

A charge-coupled device (CCD) imaging scanner may be installed in the 7530. This option requires additional circuitry to be populated on the MLB.

7 TETHER CONNECTOR

A single connector supporting a multiplicity of electrical interfaces is provided. This connector is attached to appropriate electrical elements via analogue multiplexing.

7.1 TETHER IDENTIFICATION

One pin in the tether connector is reserved for tether device identification. Identification is accomplished by adding a resistor between the ID line and ground. The 7530 measures the

resistance and determines the device from a look-up table. Once the nature of the device is determined, an appropriate electrical interface is connected to the tether device and power is supplied.

7.2   TETHER POWER

Upon detection of a valid tether device, the tether connector is supplied with 5V for powering the external tether device.

7.3   SUPPORTED INTERFACES

7.3.1   RS-232

RS-232 is supplied for connection to decoded scanners, printers, *et al.*

7.3.2   USB

A USB Device port is supplied for connection to USB scanners, mouse, *et al.*

7.3.3   TTL

A TTL interface supporting decoded scanners is provided.

8   DISPLAY SUB-SYSTEM

8.1   LCD CONTROLLER

The LCD module can is driven from a MediaQ MQ1188. This device also provides a touch panel interface and an SDIO controller.

8.2   LCD MODULE

Multiple display types can be accommodated by the 7530. A separate Display Transition Board (DTB) that connects to the MLB via flex cables is customized for each type of display.

8.3   BACKLIGHT

The LCD module contains backlight drive circuitry. Variable brightness (power levels) is provided.

9   AUDIO SUB-SYSTEM

The audio sub-system is based around an AC'97 stereo audio codec, utilizing a high-speed serial AC-LINK interface and controller embedded in the main CPU.

The audio subsystem is resident on the DTB.

9.1   AC'97 CODEC

Detailed operation of this codec is described in the AC'97 specification. A Wolfson WM9708 codec is used in the design, and does not support all AC'97 modes.

9.2 POWERDOWN OPERATION

The entire audio sub-system is placed in complete powerdown by: de-asserting PWRAMP_ON, then driving all AC_LINK signals to logic 0, then de-asserting AVDD_ENABLE. In this state the circuit draws 10s of microamps. All chips are powered off and a full cold reset is required to move to an active state. Note that both AVDD_ENABLE and PWERAMP_ON can be floated and the audio section will remain in complete powerdown.

9.3 ANALOGUE POWER SUPPLIES

An adjustable low-noise LDO regulator is used to provide a 4.5V supply for the audio circuits. Also, a low noise fixed 3.3V LDO is provided to supply the digital section of the audio sub-section. Both LDOs may be disabled by the PCON for power savings.

9.4 MICROPHONE INPUTS

The 7530 audio sub-system is designed primarily for use with close-speaking microphones that provide the best speech recognition performance. An electret condenser microphone is integrated into the 7530 housing for voice communication.

One half of an LMV722 op-amp configured as a precision voltage follower provides a low-noise 2.5V reference (A_VBIAS) for biasing the electret condenser microphones through a 2.21 kΩ resistor. This reference is heavily decoupled to minimize noise injection into the single-ended microphone inputs.

MIC_VREF is a quiet reference voltage from the codec biased at ½ AVDD (2.25V). The other half of the LMV722 is configured as an inverting multiple-feedback low pass filter (LPF) with TBD dB of passband gain, acting as a microphone pre-amp. Filter Q is set to 0.7071 for Butterworth maximally flat passband response, while fc is 12 kHz nominal. The LPF is 2nd order with a 12 dB/octave attenuation. AC coupling at the input and output of the LPF is provided by two 1uF capacitors. The output capacitor provides a high-pass -3dB pole at fc = 16 Hz, while the input coupling cap high-pass response is negligible.

The codec has an additional 0 or +20 dB selectable gain stage on MIC1.

The codec ADC full-scale input corresponds to 1V rms. The microphone gain modes for best dynamic range are listed below.

Mic Input Level	Gain Mode	Gain
2 – 30 mV rms	MIC1, pre-amp & boost	+ 30 dB
80 – 300 mV rms	MIC1, pre-amp & no boost	+ 10 dB

These levels include some headroom to avoid clipping. Do not apply signals hotter than 900 mV rms to the codec ADC inputs. Levels below 2mV rms will result in unsatisfactory performance.

9.5 AUDIO AMPLIFIER

A 350mW combination mono bridged speaker amplifier (TPA????) is used to drive an internal speaker.

10 POWER SYSTEM

The power system is based on the Smart Battery System (SBS) standard, utilizing the clocked serial SMBus interface. SBS allows the easy integration of a built-in battery charger and simplified / rapid development of various external battery chargers.

Level 2 and Level 3 SBS chargers are supported. The built-in charger is a combined Level 2 / Level 3 charger. A Level 2 charger is controlled by the Smart Battery itself, and need not be aware of the battery type or charging algorithm. Any vendor who offers a Level 2 Smart Battery charger should be able to provide a suitable charger with only a mechanical interface change to support the battery enclosure and electrical contact interface. The SBS-defined electrical connector interface is not appropriate as it is too large for the application.

Standardized software utilities compatible with SBS should be available to accelerate system software development.

10.1 POWER CONTROLLER

The 7530 architecture supports multiple batteries, and the power controller allows intelligent selection from two input sources: a DC supply (from a basic wall adapter or powered cradle) and the battery pack. Connection of either of these sources in any combination is transparently supported.

When a DC supply is available, the power controller can provide fast charge of the battery pack, while allowing the 7530 to be operated normally. If the handheld consumption and the charger consumption exceed the DC supply capability, the charger automatically reduces its charge current, which will extend the charge time somewhat. If the DC supply is between 6V and 14V the handheld will operate but the charger will be shutdown.

10.1.1 General Power Characteristics

The 7530 will accept input voltages (from batteries or DC supplies) in the range 6.0V to 24V maximum. The nominal input voltage (most common configuration) is from the battery and ranges from 11.25V to 16.5V. DC supplies may apply up to 20V (15V is typical). Although voltages above 20V are tolerated, the reliability of the power system is marginally degraded and this mode is not recommended for continuous operation.

Input current ranges are from milliamps in low power states to over 3A at 6.0V under maximum load. The practical limit for main battery operation is 2A off the battery. The use of high efficiency step-down converters allows system load currents over 3A without exceeding the main battery limit of 2A (5V @ 3A + 3.3V @ 1A translates into 1.26A total off the 16.5V battery).

WAN radios are responsible for the peak system current loads. The 7530 can support up to 3A peak radio loads on 3.3V or 5V. GSM PC Card radios such as the CardPhone2.0 are supported even in high duty cycle (multiple timeslot transmission) modes.

Radios in PC Card form factors are limited to 1.0A maximum from the CardBus interface.

10.2 SMART BATTERY SYSTEM IMPLEMENTATION

The multi-drop SMBus data and clock lines, including an SMBus accelerator (built into the charger IC) connect to the two batteries, the built-in charger, the power management microcontroller (MCU), and the external TekDock connector.

The ALERT capability of the SBS is used between the built-in charger & the power management MCU.

10.3 BUILT-IN CHARGER

When enabled by the power controller, the built-in charger will charge either the main or auxiliary battery per the charge algorithm supplied by the batteries themselves (Level 2 mode). The charging algorithm may, if necessary, be overridden by the host CPU (Level 3 mode). By definition the charger communicates over the SMBus. The charger is capable of fast charge operation (current availability near the 1C rate), and will automatically reduce charge current if needed to allow simultaneous handheld operation. When current derated the total charge time will be extended.

The charger is not enabled until the DC input supply reaches 13.5V. Low dropout techniques are used to allow the charger to operate with a 14VDC input while charging the typical battery (3 series Li-Ion cells for a charge voltage of 12.6V). Whenever the charge battery voltage reaches 89% of the DC input, a charge fault indication is transmitted over the SMBus.

The charger utilizes a synchronous current mode PWM step-down DC-DC converter synchronized to a 184kHz clock.

10.4 EXTERNAL POWER SOURCES

The 7530 can be operated while charging the battery via power from the docking connector.

External power sources may include ac-dc adapters via a portable docking module, docking stations and powered cradles.

External power specifications are as follows:

Voltage: 12 – 24VDC input, 15VDC nominal
Current: 2.5A nominal @ 15VDC
Ripple: Less than 300mV at full load
Power: 40 Watt nominal

Note that the 7530 will not charge the main or auxiliary batteries unless the DC input is at least 15V, however the rest of the system will continue to operate. Permanent damage to the electronics will occur if the DC input voltage exceeds 24VDC.

A Schottky diode in the 7530 provides reverse polarity protection.

10.5 SYSTEM BACKUP

10.5.1 Backup Supercapacitor

The backup supercapacitor maintains the system state during main battery swap. If the battery becomes exhausted or unexpectedly removed, a boost converter, sourced from the supercapacitor, is activated to maintain the 3.3V rail of the 7530 allowing the processors to save configurations and gracefully transitions into the SYS Backup state.

Based on a current consumption estimate of 20mA @ 3.3V, a fully charged supercapacitor (2.25V on 9.8F) will provide about 11 minutes system backup at room temperature.

10.5.2 RTC Supercapacitor

The real time clock has a supercapacitor backup supply for the periods when a battery is discharged or removed. The backup time is approximately *TBD* hours.

10.5.3 Supercapacitor Charging

The supercapacitors are charged from a 400mA source when battery (or external) power is available. Voltage is maintained at 2.25V.

10.6 BATTERY PACK

The main battery pack is a 3-cell Li-Ion prismatic custom design. It includes a small PCB assembly with the protection circuit & Smart Battery System (SBS) Controller.

The SBS controller includes all battery charge/discharge parameters to allow Level 2 charger operation, a high accuracy capacity monitoring facility, and various other battery monitoring functions (voltage, temperature, current, self-discharge, etc).

The pack provides 11.1VDC nominal at 1550 mAh for a total capacity of 17.2 W-h. The 3-cell architecture accommodates voltage depression at low temperature inherent in Li-Ion cells, allowing

maximum utilization of the stored energy, particularly in low temp applications. The pack safety cutoff voltage (7.5V) is higher than the minimum voltage required for operation of the handheld (6.5V), allowing discharge close to the cut-off limit. Prismatic cells allow more efficient mechanical pack design.

An emphasis is placed on maximized battery energy utilization as well as accurate battery capacity monitoring due to the significant consumption of the 7530, especially when fully loaded with peripherals or when used in extreme environmental conditions.

10.7 DUAL SWITCHING SUPPLY (3.3V/5V)

An LTC3728 dual synchronous high-efficiency switching regulator generates the 3.3V and 5V supplies. Each supply can deliver 2.5A continuous and 3A peak while maintaining efficiencies over 90%. This regulator is bi-phase synchronous, which ensures only one output switch is on at any given time. This synchronization reduces input ripple currents and EMI.

This supply accepts an input voltage range of 5.3V to 24V.

The supply is operated off a 409kHz clock supplied by the PCON.

10.8 CORE POWER SUPPLY

An LTC1878 high efficiency synchronous DC-DC current mode buck step-down regulator provides the main CPU core VDD. This supply operates at 550 kHz. The output voltage can be set to any voltage in the range 1.1V to 1.3V via resistor R_SET. A maximum of 600mA is available with a ripple of 8mV nominal. The frequency of this switcher is above most radio IF's. This power supply is enabled by the PCON.

10.9 EMC ISSUES

The design of all switching power supplies must be aware of interference issues regarding radio IF frequencies (450 kHz, 455 kHz, and 10.7MHz) as well as audio circuit susceptibility. IF circuitry typically has bandwidths of +/-10kHz @ 455 kHz, so the operating frequencies (and harmonics) of the power supplies should avoid this range.

Synchronous switchers are used wherever possible, running at 409kHz. Many of the switchers utilize a high efficiency 'burst' type of operation at low-load currents that can create noise envelopes in the audio range. Care must be taken when enabling this mode on certain switchers.

11 KEYBOARD

An intelligent keyboard, available in multiple formats, is used. The keyboard communicates with the PCON and main processor via the system I2C bus.

11.1 KEYPAD TYPES

The keypad is available in 58+1 (58 keys plus a redundant Enter key) or 36+1 (36 keys plus a redundant Enter key) formats.

11.2 INDICATORS

The keypad is supplied with four bi colour LEDs. These can be set to display in green, red or yellow with a selection of flash rates.

11.3 KEYPAD EL BACKLIGHT

The keypad includes an electroluminescent element to backlight the keys in darkness. Voltage to drive the EL panel is supplied from the MLB that contains a microcontroller driven EL backlight

driver.   The intensity of the keyboard may be varied, accomplished by the PCON sending commands to the EL microcontroller.

12 DOCKING PORT

A docking port is supplied on the 7530. This port is used to connect the 7530 to a charger or a host of other devices. The port contains multiple interfaces for data communications.

12.1 DOCK IDENTIFICATION

A pin is supplied for identification of devices attaching to the docking port. The device attaching to the docking port provides a (unique) resistance to ground on the DOCK_ID pin.

12.2 POWER CONNECTIONS

12.2.1 DC Power

A DC input for charging the battery and operating the terminal is provided.   The input may be between 6 and 20 volts; however, a minimum of 14 volts is required for battery charging to occur.

12.3 DATA CONNECTIONS

12.3.1 RS-232 Port

Communications with either the PXA255 or PCON can be done via RS-232.   Programming of the PCON may also be done via this port.

12.3.2 USB Device

12.3.3 USB Host

13 FIRMWARE LOADING OPTIONS

13.1 PRODUCTION FIRST LOAD

13.1.1 Peripheral Controller Firmware

The Peripheral Controller is an in-circuit re-programmable FLASH-based device that is programmed via an RS-232 serial interface. This interface is accessible through the Docking Port Connector.

13.1.2 System Firmware

13.1.2.1 Initial Firmware Loading

Automatic loading via Compact Flash card.

13.1.2.2 Subsequent Firmware Loading

Via compact flash card, Ymodem over RS-232 (very slow) or, preferably, via USB using file drop and drag.

13.2 FIELD FIRMWARE UPGRADE

This scenario assumes some or all of the firmware on the handheld is to be upgraded. See 13.1 if the FLASH has been corrupted or erased.

13.2.1 Upgrade Via Laptop/PC

Connect laptop or PC to handheld using the USB slave interface cable (P/N TBD) between the USB port and a USB *host* port on the laptop (this is the standard USB port on every laptop).

Use a standard USB file transfer utility (TBD) to copy the new firmware image onto the handheld (note this connection runs at 12 Mbps and should only take a few seconds to complete).

13.2.2 Upgrade Via RF Backbone

For 802.11 backbones only, a Teklogix firmware upgrade facility may have been deployed, in which case it will be ported to this handheld.

14 OPERATING STATES

The fundamental power conservation technique is to execute tasks as quickly as possible (*Run* state) and then return to a low power state (*Suspend* or *Halt*). This method is considered more effective than dynamically adjusting the CPU & bus clock speeds as the consumption of the SDRAM array is the primary contributor to power consumption (excluding the LCD backlight). SDRAM has high current consumption in all but power down modes, so there is a power penalty incurred holding the SDRAM in standby even if not running SDRAM cycles. The CPU clock is set as high as necessary to provide the required peak performance level.

This technique relies on extremely fast entry/exit from low power states.

14.1 STANDARD OPERATING STATES

Standard operating states are entered/exited either under software control or by hardware signal. In all standard operating states the system state is maintained (no data is lost). State transitions are sequential when moving to lower power states (on entry), while all low power states exit directly to the *Run* state. Transitions to lower power states occur on separately programmable inactivity timeouts.

Resets are not used in any standard operating states.

Suspend is a special implementation of the *Halt* state wherein the LCD controller maintains a static display image even though the CPU, SDRAM, etc are asleep. Instantaneous transition from *Suspend* to *Run* makes it appear the unit is running normally to the user even though a power down mode was entered. In almost all applications, the unit will spend upwards of 80% of a shift in the *Suspend* or *Halt* states. There is a user configurable timeout on the display backlight in *Suspend*

mode, whereby the delay to display dimming as well as the display intensity can be configured. Dimming of the backlight contributes dramatically to the system power savings.

It is required that primary power (dc in or battery) be available in all standard operating states.

Operating State	Power Consumption	Description	Exit
Standby	Minimal	Device appears to be off. Display blank, LEDs off. Restart time is noticeable.	Press ON key sequence to exit.
Halt	V.Low	Device appears off. Display blank, LEDs may all be off. Restart time is immediate.	Press any key (or certain specified keys), press trigger switch, tap touchscreen.
Suspend	Low	Device appears on. Display is on but static, backlight may be dimmed, LEDs may be on. Restart time is immediate.	Press any key, press trigger switch, tap touchscreen, receive radio message, or any other user input.
Run	High	Device is fully operational, running at maximum clock speed.	N/A

14.2 ABNORMAL OPERATING STATES

'SYS Backup', 'RTC Backup', and 'All Power Off' are considered abnormal operating states:

Operating State	Description	Issues
SYS Backup	Primary power removed, supercapacitor supporting system backup	System state is maintained. Unit appears off. System will recover via ON key once primary power is restored.
RTC Backup	Primary power removed, backup supercapacitor depleted, RTC supercapacitor operational	All system state except RTC lost. Recovery via warm reset.
All Power Off	Primary power removed, backup and RTC supercapacitors depleted.	Real time clock is invalid. All system state lost. Recovery via cold reset.

Note that in RTC Backup the peripheral controller is active, periodically transitioning from a sleep mode to active state.

14.3 OPERATING STATE TRANSITIONS

State Transition	Trigger Event	Description
Halt -> Run	Any key pressed, screen tap, other user input but not radio message	
Standby -> Run	ON key pressed	
Suspend -> Run	Any key pressed, screen tap, other user input or radio message	
Run -> Suspend	CPU enters IDLE loop?	

Suspend -> Halt	Inactivity timeout configurable, typical 5 minutes	Unit appears to gone to sleep although full system state is maintained.
Halt -> Standby	Inactivity timeout configurable, typical 1 hour	Unit appears off.
Standby -> SYS Backup	Primary power removal	Transition to abnormal operating states due to battery removal.
SYS Backup -> RTC Backup	Primary power removal + backup supercapacitor discharged to 20% nominal OR backup timer expiration	Typical system backup time is 1 hour, but may be configured from several minutes to approx 2 hours maximum.
RTC Backup -> All Power Off	Primary power removal + Backup supercapacitor depleted	Typical RTC backup time is *TBD* days(?)
All Power Off -> Standby RTC Backup -> Standby SYS Backup -> Standby	Primary power source applied	

14.4 SYSTEM CLOCKS

System Clock	All power off	RTC backup	SYS Backup	Standby	Halt	Suspend	Run
Real-time clock	OFF	32.768kHz		32.768kHz			
CPU Clock	OFF			OFF	OFF	OFF	400 MHz
CPU Ext Bus	OFF			OFF	OFF	OFF	100 MHz
LCD Control	OFF			OFF	48 MHz SS	48 MHz SS	48 MHz SS
PCON Clock	OFF	32.768kHz	2 MHz?	7.3728 MHz	7.3728 MHz	7.3728 MHz	7.3728 MHz
DUART Clock	OFF			OFF	OFF?	3.6864MHz	3.6864MHz
AC'97 Codec	OFF			OFF			
Power Supply Sync	OFF			Not synchronized	409 kHz	409kHz	409 kHz