



COMPAL

4G EXC-N1 Module

DataSheet

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Revision History

Version	Date	Name	Major Changes
AA	Aug. 31, 2022	HW V01	First release
AB	Sep. 20, 2022	HW V01	<ul style="list-style-type: none">● Only support B41M , modify B41to B41M and frequency range on P12/49/59/60● Remove power consumption @ GSM/WCDMA/LTE mode on P31-35

Applicability Table

No.	Product model	Description
1	ZXG1	4G EXC-N1: (V1.0 Module) <u>All relevant LCC HW spec , figures and design guidelines in this document are common specification for All 4G LCC model.</u>



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1 Foreword

1.1 Introduction

This document defines the EXC-N1 module and the air interface and hardware interface that the module connects to the client application.

This document helps customers quickly understand EXC-N1 module interface specifications, electrical characteristics, mechanical specifications, and related product information. With the help of this document, combined with our application manual and user instructions, customers can quickly apply the EXC-N1 module to wireless applications.

EXC-N1 wireless module is a vehicle standard wireless broadband terminal product applicable to TDD-LTE/FDD-LTE/WCDMA.

EXC-N1 can support access rates:

- TDD-LTE:130Mbps/35Mbps;
- FDD-LTE:150Mbps/50Mbps;
- WCDMA rate up to DC HSPA+: 42Mbps/5.76Mbps;
- GSM rate up to EDGE: 236.8kbps/236.8kbps. (N/A)

1.2 Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating with 4G LCC module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, we assume no liability for customers' failure to comply with these precautions.



..Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The



operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.



The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.



In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.



Safety of Children

Do not allow children to use the wireless device without guidance. Small and sharp components of the wireless device may cause danger to children or cause suffocation if children swallow the components.

Environment Protection

Observe the local regulations regarding the disposal of your packaging materials, used wireless device and accessories, and promote their recycling.

WEEE Approval

The wireless device is in compliance with the essential requirements and other relevant provisions of the Waste Electrical and Electronic Equipment Directive 2012/19/EU (WEEE Directive).

RoHS Approval

The wireless device is in compliance with the restriction of the use of certain hazardous substances in electrical and electronic equipment Directive 2011/65/EU (RoHS Directive).



1.3 Reference Standard (to be update)

The design of the product complies with the following standards:

Table1-1 3GPP Standards

3GPP TS specification reference	Title	3GPP Release used as the basis for this declaration
23.122	Non-Access-Stratum functions related to Mobile Station (MS) in idle mode	11.4.0
24.008	Mobile radio interface Layer 3 specification; Core network protocols; Stage 3	11.5.0
25.331	Radio Resource Control (RRC); protocol specification	9.0.0
25.133	Requirements for Support of Radio Resource Management (FDD)	13.2.0
25.101	Radio Transmission and Reception (FDD)	14.0.0
24.301	(NAS) protocol for Evolved Packet System (EPS); Stage 3	11.7.0
36.101	(E-UTRA); User Equipment (UE) radio transmission and reception	12.14.1
36.133	(E-UTRA); Requirements for support of radio resource management	14.14.0
36.213	(E-UTRA) Physical layer procedures	12.11.0
36.214	(E-UTRA) Physical layer measurements	12.3.0
36.304	(E-UTRA); User Equipment (UE) procedures in idle mode	12.8.0
36.321	(E-UTRA); Medium Access Control (MAC) protocol specification	12.9.0
36.322	(E-UTRA); Radio Link Control (RLC) protocol specification	12.4.0
36.323	(E-UTRA); Packet Data Convergence Protocol (PDCP) specification	12.6.0
36.331	(E-UTRA); Radio Resource Control (RRC); Protocol specification	15.3.0
24.501	Non-Access-Stratum (NAS) protocol for 5G System (5GS); Stage 3	15.1.0
38.331	NR;Radio Resource Control (RRC) protocol specification	15.3.0
38.133	NR; Requirements for support of radio resource management	15.3.0
38.213	NR; Physical layer procedures for control	15.3.0
38.323	NR; Packet Data Convergence Protocol (PDCP) protocol specification	15.3.0
37.324	Service Data Adaptation Protocol (SDAP) specification	15.1.0
11.11/51.011	Specification of the Subscriber Identity Module - Mobile Equipment (SIM-ME) Interface	4.15.0
31.102	Characteristics of the Universal Subscriber Identity Module (USIM) application	12.11.0
31.103	Characteristics of the IP Multimedia Services Identity Module (ISIM) application	12.2.0
31.101	UICC-terminal interface; Physical and logical characteristics	12.2.0
27.007	AT command set for 3GPP User Equipment (UE)	9.9.0
36.355	(E-UTRA); LTE Positioning Protocol (LPP)	14.2.0
44.031	Location Services (LCS)- MS-SMLC Radio Resource LCS Protocol (RRLP)	14.3.0

Non-3GPP documentation:

Table1-2 ETSI

Document Source	Title	Version
ETSI	TS 102 221: "UICC-Terminal interface; Physical and logical characteristics".	12.1.0
ETSI	TS 102 223: "Smart Cards; Card Application Toolkit".	12.3.0

Table1-3 GSMA

Document Source	Title	Version
GSMA	IR.92 IMS Profile for Voice and SMS	8.0.0
GSMA	IR.94 IMS Profile for Conversational Video Service	7.0.0



Table1-4 OMA

Document Source	Title	Version
OMA	OMA-AD-SUPL-V1	
OMA	OMA-AD-SUPL-V2	

1.4 Related Documents

- 4G LCC Module System Driver Integration and Application Guidance
- 4G LCC Module AT Commands Manual



2 Overview

2.1 Introduction

EXC-N1 is support for TDD-LTE/FDD-LTE /WCDMA wireless communication module. It supports data connection of TDD-LTE and FDD-LTE networks, and is compatible with DC-HSPA+ of WCDMA network data connection. It can provide Voice (PCM), Analog voice, Short message, Address book and other functions for customers' special applications.

Table 2-1 EXC-N1 module support frequency bands

Network	EXC-N1
TDD-LTE	B41M
FDD-LTE	B2/4/5/7/12/13/17/ 25/26/66
WCDMA	B2/4/5
TD-SCDMA	Not supported
EVDO	Not supported
CDMA	Not supported
GSM	Not supported

2.2 Specification

Table 2-2 LCC module features

Specification	
Platform	QCT MDM9207 Cortex-A7 up to 1.2 GHz
Memory	1Gb NAND Flash with 1Gb LPDDR2(400MHz) MCP
Operating Band	5G Refarmed Sub6 : NA
	5G NR_mmWave: N/A
	LTE FDD: B2, B4, B5, B7, B12, B13, B17, B25, B26, B66
	LTE TDD: B41M
	WCDMA/HSPA+: B2, B4, B5



	Simultaneous GPS : L1, GLONASS(GLO), Galileo(GAL) and BeiDou(BDS)	
Network option	SA	N/A
	NSA	N/A
Downlink	LTE	LTE CAT4
	5G sub-6	N/A
	5G mmWave	N/A
Uplink	LTE	LTE CAT3
	5G sub-6	N/A
	5G mmWave	N/A
HPUE (Class 2)	N/A	
UL 2x2 MIMO	N/A	
DL 4x4 MIMO	N/A	
Carrier aggregation	N/A	
Power Supply	DC 3.3V~4.2V(Typical value is 3.8V)	
Temperature	Operating temperature[1]:-30°C ~+75°C	
	Extended temperature[2] : -40°C ~+85°C	
	Storage temperature: -45°C ~+90°C	
Physical characteristics	Dimension:32.0x29.0mm, Thickness=2.5mm(typ.)	
	Weight: <5g	
Interface		
Antenna Port	Main antenna (ANT_MAIN)	
	RX- diversity antenna (ANT_DIV)	
	GNSS antenna(ANT_GNSS)	
	Power interface	
	USB2.0 High-Speed interface	
	UART interface	
	USIM/SIM interface (Support 3V,1.8V)	
	PCM interface(optional)	
	Reset interface	



Function Interface	Indicator interface
	Dormancy control interface
	Flight mode control interface
	ADC interface
	I2C interface
	SGMII interface(optional)
	SD card interface(optional)
	WLAN interface(optional)
	BT_UART interface(optional)
	USB_BOOT interface(optional)
Software	
Driver	TBD
Protocol Stack	TBD
AT commands	Comply with 3GPP TS 27.007, 27.005
Firmware update	FOTA (not support for 1Gb+1Gb)
Others feature	Windows MBIM support
	Windows update



NOTE:

[1] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP.

[2] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. When the LCC module works at this temperature, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, etc.

Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may undergo a reduction in value, exceeding the specified tolerances of 3GPP.



2.3 CA combinations

N/A

2.4 EN-DC combinations with in 5G FR1

N/A

2.5 EN-DC combinations with in 5G FR2

N/A

2.6 Circuit Block Diagram

The following is the block diagram of EXC-N1, illustrating its main functions.

- Power management
- Baseband chip
- DDR + NAND memory
- RF part
- Peripheral interface

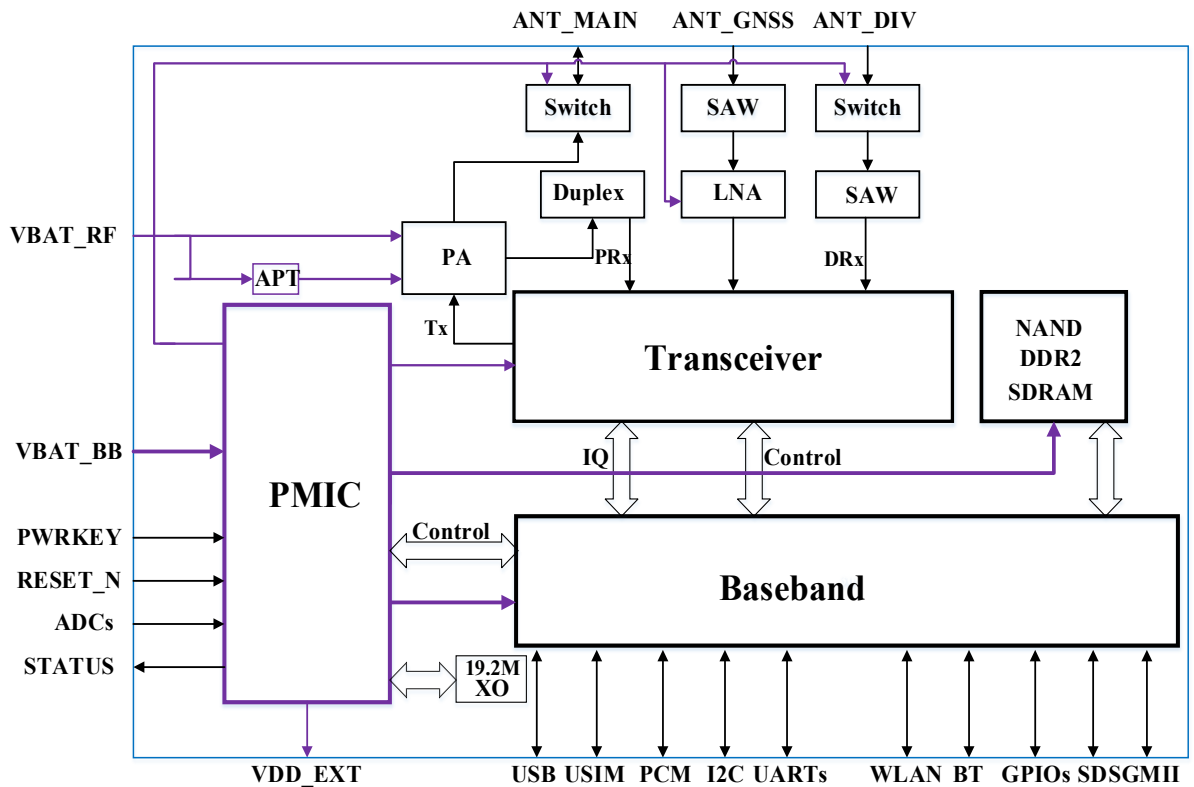


Figure 2-1 Functional Block Diagram



2.7 Application Block Diagram

N/A

Peripherals Interface Description:

USB Interface:

The USB interface supports USB 2.0 high speed standard.

SDIO Interface:

Supports the SDIO 3.0 protocol

USIM Interface:

The USIM interface.

LCM:

N/A

Audio Interface:

The module supports I2S/PCM interface (can be configured as either I2S or PCM interface)

PCIE:

N/A

SPI Interface:

N/A.

I2C Interface:

Reserved for intelligent module in future.

UART Interface:

The module supports 2 UART interfaces. One is 7-wire UARTs. One is 2-wire UART, which is only for debugging.

External Power Supply:

Output Power Supply from LCC module:

- A. VDD_EXT (1.8V) : External 1.8V output , Power supply for external GPIO's pull up circuits; If unused, keep it open



B. USIM_VDD (1.8V/3V) : USIM card supply voltage , Automatic module recognition 1.8V or 3.0V USIM card

C. USIM2_VDD(1.8V/2.85V): SGMII MDIO pull-up power supply ,Output 1.8V/2.85V configurable; Can be used for pull-up, not directly for power supply. If unused, keep it open.

Extra Power Supply Require for LCC module:

A. DC 3.8 V is recommended for module VPH_PWR

B. USB_VBUS for USB detection

RF Pad:

RF antenna interface.(Main, Div, GNSS)

Tunable ANT CTRL:

N/A

SGMII:

The EXC-N1 module includes an integrated Ethernet MAC SGMII interface and two management interfaces (MDIO). Support 10/100/1000Mbps Ethernet connection

3 Application Interface

3.1 LCC Interface

EXC-N1 adopts LCC+LGA interface, A total of 144 Pins, including 80 LCC pins and 64 LGA pins, are provided with the following functional interfaces:

- Power interface
- USB2.0 High-Speed interface
- UART interface
- USIM/SIM interface
- PCM interface
- Reset interface
- Indicator interface
- Dormancy control interface
- Flight mode control interface
- ADC interface
- I2C interface
- SGMII interface
- SD card interface
- WLAN interface
- BT_UART interface
- USB_BOOT interface



3.2 Pin Map

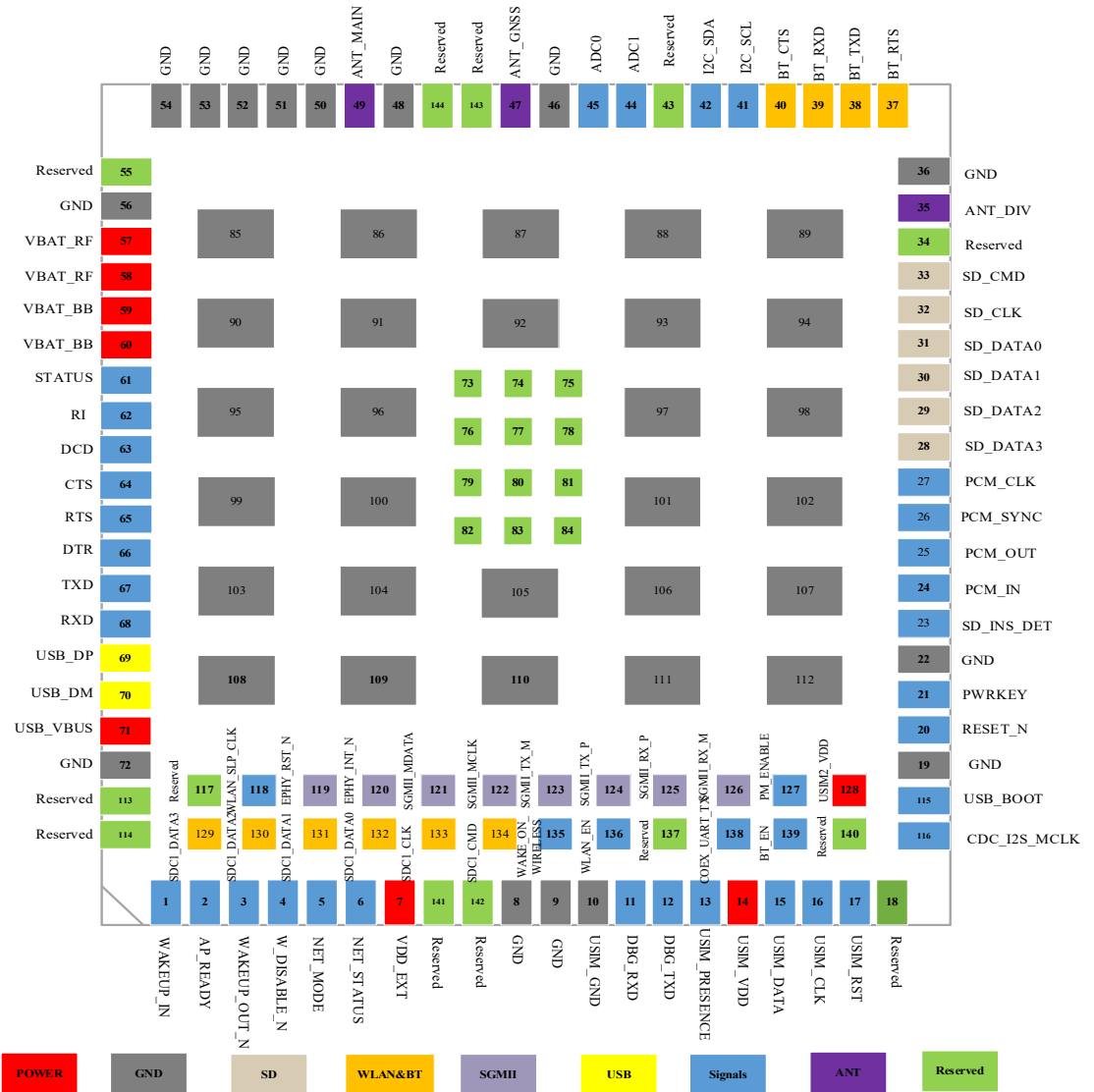


Figure 3-1 Module pin number diagram

3.2.1 Pin Definition

The following table describes the definitions of the individual pins for the EXC-N1 module.

Table 3-1 IO parameter definition

Type	Description
IO	Input and output
DI	Digital input
DO	Digital output
PI	Power input



PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 3-2 Pin description

Pin name	Pin number	I/O	Description	DC features	Note
VBAT_BB	59, 60	PI	Power supply for module baseband	V _{max} =4.2V V _{min} =3.3V V _{norm} =3.8V	It must be able to provide sufficient current up to 1A
VBAT_RF	57, 58	PI	Power supply for module RF	V _{max} =4.2V V _{min} =3.3V V _{norm} =3.8V	It must be able to provide sufficient current up to 2A
VDD_EXT	7	PO	1.8V output	V _{norm} =1.8V I _{o,max} =80mA	Power supply for external GPIO's pull up circuits; If unused, keep it open
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	-	Ground	-	-
RESET_N	20	DI	Reset the module	V _{IH,max} =2.1V V _{IH,min} =1.3V V _{IL,max} =0.5V	1.8V power domain, effective at low level; If unused, keep it open
PWRKEY	21	DI	Turn on/off the module	V _{IH,max} =2.1V V _{IH,min} =1.3V V _{IL,max} =0.5V	There is a voltage drop in the diode inside the High-pass chip, so the Pin outputs 0.8V
STATUS	61	OD	Indicate the module operating status	The drive current should be less than 0.9mA	Require external pull-up. If unused, keep it open.
NET_MODE	5	DO	Indicate the module network registration status	V _{OH,min} =1.35V V _{OL,max} =0.45V	1.8V power domain; If unused, keep it open
NET_STATUS	6	DO	Indicate the module network activity status	V _{OH,min} =1.35V V _{OL,max} =0.45V	1.8V power domain; If unused, keep it open
USB_VBUS	71	PI	USB detection	V _{max} =5.25V V _{min} =3.0V V _{norm} =5.0V	
USB_DP	69	IO	USB differential data positive signal	Compliant with USB2.0 standard specification	Require differential impedance of 90Ω



USB_DM	70	IO	USB differential data negative signal	Compliant with USB2.0 standard specification	Require differential impedance of 90Ω
USIM_DATA	15	IO	USIM card data signal	1.8V USIM: V _{ILmax} =0.6V V _{IHmin} =1.2V V _{OLmax} =0.45V V _{OHmin} =1.35V 3.0V USIM: V _{ILmax} =1.0V V _{IHmin} =1.95V V _{OLmax} =0.45V V _{OHmin} =2.55V	-
USIM_CLK	16	DO	USIM card clock signal	1.8V USIM: V _{OLmax} =0.45V V _{OHmin} =1.35V 3.0V USIM: V _{OLmax} =0.45V V _{OHmin} =2.55V	-
USIM_RST	17	DO	USIM card reset signal	1.8V USIM: V _{OLmax} =0.45V V _{OHmin} =1.35V 3.0V USIM: V _{OLmax} =0.45V V _{OHmin} =2.55V	-
USIM_PRESENCE	13	DI	USIM detection	V _{ILmin} =-0.3V V _{ILmax} =0.6V V _{IHmin} =1.2V V _{IHmax} =2.0V	1.8V power domain, need external pull up to 1.8V
USIM_VDD	14	PO	USIM card supply voltage	1.8V USIM: V _{max} =1.9V V _{min} =1.7V 3.0V USIM: V _{max} =3.05V V _{min} =2.7V I _o max=50mA	Automatic module recognition 1.8V or 3.0V USIM card
USIM_GND	10		USIM ground		Connect to the ground of the module
RI	62	DO	Ring indicator	V _{OLmax} =0.45V V _{OHmin} =1.35V	1.8V power domain.do not pull up to high level before the module starts successfully. If unused, keep it open
DCD	63	DI	Carrier detect	V _{OLmax} =0.45V V _{OHmin} =1.35V	1.8V power domain. If unused, keep it open



DTR	66	DO	DTE ready, sleep mode control	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open
RXD	68	DI	ReCompalve data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open
TXD	67	DO	Transmit data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open
CTS	64	DI	Clear to send	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open
RTS	65	DO	DTE requires to transmit data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open
DBG_TXD	12	DO	The module sends data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open
DBG_RXD	11	DI	The module reCompalves data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open
ADC0	45	AI	Universal analog-to-digital conversion	voltage range: 0.1V~1.7V	If unused, keep it open
ADC1	44	AI	Universal analog-to-digital conversion	voltage rang: 0.1V~1.7V	If unused, keep it open
USB_BOOT	115	DI	Mandatory download mode control, High level effective	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. It is recommended to reserve test points.
PCM_IN	24	DI	PCM data input	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. Module as the main device, the pin is the output signal, module as the slave device, the pin is the input signal. If unused, keep it open.



PCM_SYNC	26	IO	PCM data synchronization signal	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. Module as the main device, the pin is the output signal, module as the slave device, the pin is the input signal. If unused, keep it open.
CDC_I2S_MCLK	116	DO	19.2MHz clock signal	-	The module outputs a 19.2mhz clock signal to provide a clock signal to the external CODEC, If unused, keep it open.
I2C_SCL	41	IO	I2C clock	-	Require external pull-up to 1.8V.If unused, keep it open.
I2C_SDA	42	IO	I2C data	-	Require external pull-up to 1.8V.If unused, keep it open.
ANT_DIV	35	AI	Diversity antenna	50Ω impedance	
ANT_MAIN	49	IO	Main antenna	50Ω impedance	
ANT_GNSS	47	AI	GNSS antenna	50Ω impedance	
WAKEUP_IN	1	DI	Sleep mode control	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. High level wakes up the module; in low level the module enters into sleep mode. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. Do not pull up to high level before the module starts successfully. If unused, keep it open.
WAKEUP_OUT_N	3	DO	Sleep mode output	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open. The module output low level after entering sleep.
W_DISABLE_N	4	DI	Airplane mode control	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. The low level puts the module into flight mode, If unused, keep it open.
BT_RTS	37	DO	DTE requires to transmit data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open
BT_TXD	38	DO	Transmit data	$V_{OLmax}=0.45V$	1.8V power domain. If



				$V_{OHmin} = 1.35V$	unused, keep it open
BT_RXD	39	DI	ReCompalve data	$V_{ILmin} = -0.3V$ $V_{ILmax} = 0.6V$ $V_{IHmin} = 1.2V$ $V_{IHmax} = 2.0V$	1.8V power domain. If unused, keep it open
BT_CTS	40	DI	Clear to send	$V_{OLmax} = 0.45V$ $V_{OHmin} = 1.35V$	1.8V power domain. If unused, keep it open
BT_EN	139	DO	Bluetooth enable	$V_{OLmax} = 0.45V$ $V_{OHmin} = 1.35V$	1.8V power domain. If unused, keep it open
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open
PM_ENABLE	127	DO	WLAN external power enable control, high level effective	$V_{OLmax} = 0.45V$ $V_{OHmin} = 1.35V$	1.8V power domain. If unused, keep it open
SDC1_DATA3	129	IO	WLAN SDIO Bus data line 3	$V_{OLmax} = 0.45$ $V_{OHmin} = 1.35V$ $V_{ILmin} = -0.3V$ $V_{ILmax} = 0.6V$ $V_{IHmin} = 1.2V$ $V_{IHmax} = 2.0V$	1.8V power domain. If unused, keep it open
SDC1_DATA2	130	IO	WLAN SDIO Bus data line 2	$V_{OLmax} = 0.45$ $V_{OHmin} = 1.35V$ $V_{ILmin} = -0.3V$ $V_{ILmax} = 0.6V$ $V_{IHmin} = 1.2V$ $V_{IHmax} = 2.0V$	1.8V power domain. If unused, keep it open
SDC1_DATA1	131	IO	WLAN SDIO Bus data line 1	$V_{OLmax} = 0.45$ $V_{OHmin} = 1.35V$ $V_{ILmin} = -0.3V$ $V_{ILmax} = 0.6V$ $V_{IHmin} = 1.2V$ $V_{IHmax} = 2.0V$	1.8V power domain. If unused, keep it open
SDC1_DATA0	132	IO	WLAN SDIO Bus data line 0	$V_{OLmax} = 0.45$ $V_{OHmin} = 1.35V$ $V_{ILmin} = -0.3V$ $V_{ILmax} = 0.6V$ $V_{IHmin} = 1.2V$ $V_{IHmax} = 2.0V$	1.8V power domain. If unused, keep it open
SDC1_CLK	133	DI	WLAN SDIO clock	$V_{OLmax} = 0.45$ $V_{OHmin} = 1.35V$	1.8V power domain. If unused, keep it open
SDC1_CMD	134	IO	WLAN SDIO command	$V_{OLmax} = 0.45$ $V_{OHmin} = 1.35V$	1.8V power domain. If unused, keep it open
WAKE_ON_WIRELESS	135	DI	WLAN wake up the module	$V_{ILmin} = -0.3V$ $V_{ILmax} = 0.6V$	1.8V power domain. If unused, keep it open. Do



				$V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	not pull up to high level before the module starts successfully
WLAN_EN	136	DO	WLAN enabled, high level effective	$V_{OLmax}=0.45$ $V_{OHmin}=1.35V$	1.8V power domain, high level effective, Do not pull up to high level before the module starts successfully
COEX_UART_TX	138	DO	GPIO	$V_{OLmax}=0.45$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open. Do not pull up to high level before the module starts successfully
EPHY_RST_N	119	DO	Ethernet PHY reset	For 1.8V: $V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ For 2.85V: $V_{OLmax}=0.35V$ $V_{OHmin}=2.14V$	1.8V /2.85V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interruption	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V /2.85V power domain. If unused, keep it open.
SGMII_MDATA	121	IO	SGMII MDIO data	For 1.8V: $V_{OLmax}=0.45V$ $V_{OHmin}=1.4V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ For 2.85V: $V_{OLmax}=0.35V$ $V_{OHmin}=2.14V$ $V_{ILmax}=0.71V$ $V_{IHmin}=1.78V$	1.8V /2.85V power domain. If unused, keep it open. External pull up to USIM2_VDD, pull up resistance is 1.5K;
SGMII_MCLK	122	DO	SGMII MDIO clock	For 1.8V: $V_{OLmax}=0.45V$ $V_{OHmin}=1.4V$ For 2.85V: $V_{OLmax}=0.35V$ $V_{OHmin}=2.14V$	1.8V /2.85V power domain. If unused, keep it open.
USIM2_VDD	128	PO	SGMII MDIO pull-up power supply	-	Output 1.8V/2.85V configurable; Can be used for pull-up, not directly for power supply. If unused, keep it open.
SGMII_TX_M	123	AO	SGMII differential data sends a negative signal	-	If unused, keep it open.



SGMII_TX_P	124	AO	SGMII differential data sends a positive signal	-	If unused, keep it open.
SGMII_RX_P	125	AI	SGMII differential data reCompalve positive signals	-	If unused, keep it open.
SGMII_RX_M	126	AI	SGMII differential data reCompalves negative signals	-	If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detection	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
SD_CMD	33	IO	SD card SDIO instruction signal	1.8V SD card: $V_{OLmax}=0.45$ $V_{OHmin}=1.4V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{IHmax}=2.0V$ 3.0V SD card: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.76V$ $V_{IHmin}=1.72V$ $V_{IHmax}=3.34V$	SDIO signal level can be selected according to the signal level supported by SD card. For details, please refer to SD 3.0 protocol. If unused, keep it open.
SD_CLK	32	DO	SD card SDIO clock signal	1.8V SD card: $V_{OLmax}=0.45V$ $V_{OHmin}=1.4V$ 3.0V SD card: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$	SDIO signal level can be selected according to the signal level supported by SD card. For details, please refer to SD 3.0 protocol. If unused, keep it open.
SD_DATA3	28	IO	SD card SDIO Bus DATA3	1.8V SD card: $V_{OLmax}=0.45$ $V_{OHmin}=1.4V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{IHmax}=2.0V$ 3.0V SD card: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.76V$ $V_{IHmin}=1.72V$	SDIO signal level can be selected according to the signal level supported by SD card. For details, please refer to SD 3.0 protocol. If unused, keep it open.



				$V_{IHmax}=3.34V$	
SD_DATA2	29	IO	SD card SDIO Bus DATA2	<p>1.8V SD card: $V_{OLmax}=0.45$ $V_{OHmin}=1.4V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{IHmax}=2.0V$</p> <p>3.0V SD card: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.76V$ $V_{IHmin}=1.72V$ $V_{IHmax}=3.34V$</p>	SDIO signal level can be selected according to the signal level supported by SD card. For details, please refer to SD 3.0 protocol. If unused, keep it open.
SD_DATA1	30	IO	SD card SDIO Bus DATA1	<p>1.8V SD card: $V_{OLmax}=0.45$ $V_{OHmin}=1.4V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{IHmax}=2.0V$</p> <p>3.0V SD card: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.76V$ $V_{IHmin}=1.72V$ $V_{IHmax}=3.34V$</p>	SDIO signal level can be selected according to the signal level supported by SD card. For details, please refer to SD 3.0 protocol. If unused, keep it open.
SD_DATA0	31	IO	SSD card SDIO Bus DATA0	<p>1.8V SD card: $V_{OLmax}=0.45$ $V_{OHmin}=1.4V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{IHmax}=2.0V$</p> <p>3.0V SD card: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.76V$ $V_{IHmin}=1.72V$ $V_{IHmax}=3.34V$</p>	SDIO signal level can be selected according to the signal level supported by SD card. For details, please refer to SD 3.0 protocol. If unused, keep it open.
RESERVED	18, 34, 43, 55, 73~84,				Keep it open.



	113, 114, 117, 137, 140~144				
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NOTE:

The unused pins can be left floating.

- **P** indicates power pins; **I** indicate pins for digital signal input; **O** indicates pins for digital signal output; **PO** indicates power output pins; **PI** indicates power input pins.
- **VIL** indicates Low-level Input voltage; **VIH** indicates High-level Input voltage; **VOL** indicates Low-level Output voltage; **VOH** indicates High-level Output voltage.
- The **Reserved** pins are internally connected to the module. Therefore, these pins should not be used, otherwise they may cause problems. Please contact with us for more details about this information.

3.3 Power Interface

EXC-N1 has four VBAT pins for connecting an external power supply, which can be divided into two power supply domains:

- Two VBAT_RF pins are used to power the module's RF;
- Two VBAT_BB pins are used to power the baseband of the module.

The following table shows the distribution of power pins and ground pins for the module:

Table 3-3 VBAT pin and ground pin

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
57, 58	VBAT_RF	Power supply for module baseband	3.3	3.8	4.2
59, 60	VBAT_BB	Power supply for module RF	3.3	3.8	4.2
8, 9, 10, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	GND	Ground	-	0	-

4G LCC Module can use any power source which is followed “Table 3-3 power supply input” as an Input power. Then, it has 2 output powers for each function such as, USIM, and SGMII. Due to the limited power trace, all of them should use efficiently when design the layout.



When the 4G LCC module is used for different external applications, pay special attention to the design for the power supply. When the 4G LCC module works at 4G mode and transmits signals at the maximum power, the transient current may reach the transient peak value of about 4A due to the differences in actual network environments. In this case, the VBAT voltage drops. If you want wireless good performance, please make sure that the voltage does not decrease below 3.4 V in any case. Otherwise, exceptions such as restart of the 4G LCC module may occur.

It is recommended that customers add the EMI ferrite bead (FBMJ1608HS280NT manufactured by TAIYO YUDEN or MPZ1608S300ATAH0 manufactured by TDK is recommended) to directly isolate DTE from DCE in the power circuit.

3.3.1 Power Supply

The power supply range of EXC-N1 is from 3.3V to 4.2V. During data transmission or conversation, instantaneous high-power emission will form a peak current up to 2A, which will lead to a large ripple of VBAT. If instantaneous voltage drop leads to too low VBAT power supply voltage, the module will shut down. Make sure there are sufficient power supply capabilities and the input voltage will never drop below 3.3V to make the module work well. The following figure is the module switch threshold state definition

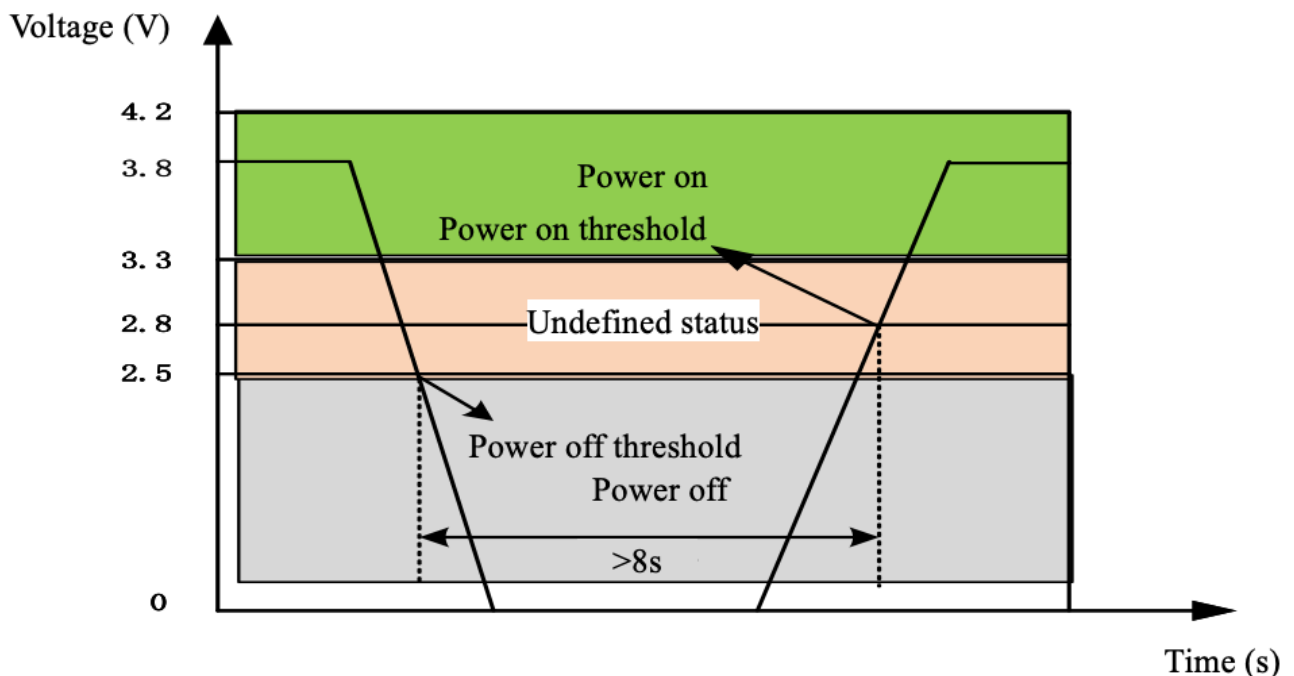


Figure 3-2 Switching machine threshold

The following figure shows the voltage drop during transmitting burst in 2G network. The voltage drop will be less in 3G and 4G networks.

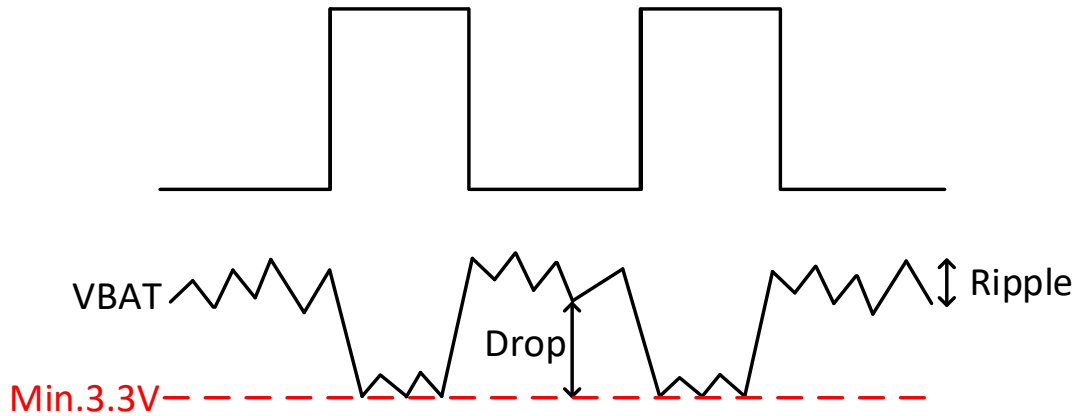


Figure 3-3 Power requirements for burst transmission

To reduce voltage sags, a 100uF filter capacitor with a low ESR is required. MLCC has the best ESR. It is recommended to add 3 ceramic capacitors (100nF, 33pF, 10pF) to VBAT_BB and VBAT_RF pins, and the capacitors should be placed close to the VBAT pins. At the same time, in order to ensure better power supply performance, a TVS tube is added near the input end of the module VBAT to improve the surge voltage bearing capacity of the module. It is recommended to use Changyuan Vian, model WS4.5DPV. When the external power supply is connected to the module, VBAT_BB and VBAT_RF need to adopt star routing. VBAT_BB wire width shall not be less than 1mm, and VBAT_RF wire width shall not be less than 2mm. In principle, the longer the line in VBAT, the wider the line.

The reference circuit is as follows :

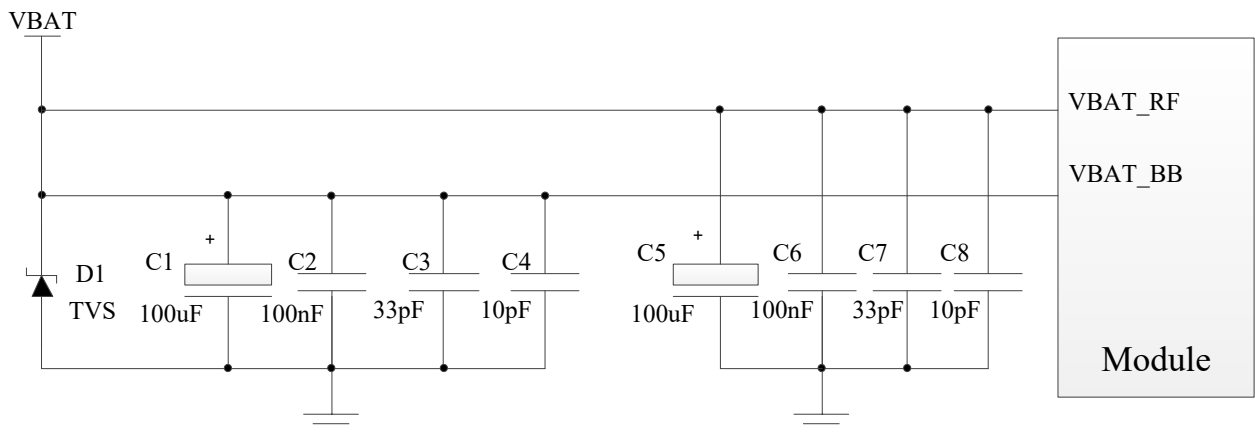


Figure 3-4 Reference Circuit for Power Supply

The design of the module power supply is very important because the performance of the module depends largely on the power supply. The power supply can provide at least 2A current. If the voltage difference between input and output is not very large, it is recommended to use LDO power supply module; If the voltage difference between input and output is large, DCDC is preferred as the power source.



The figure below is the reference design of +5V power supply circuit. The design use Micrel LDO, model MIC29302WU. Its typical output voltage is 3.8V and the peak load current reaches 3A.

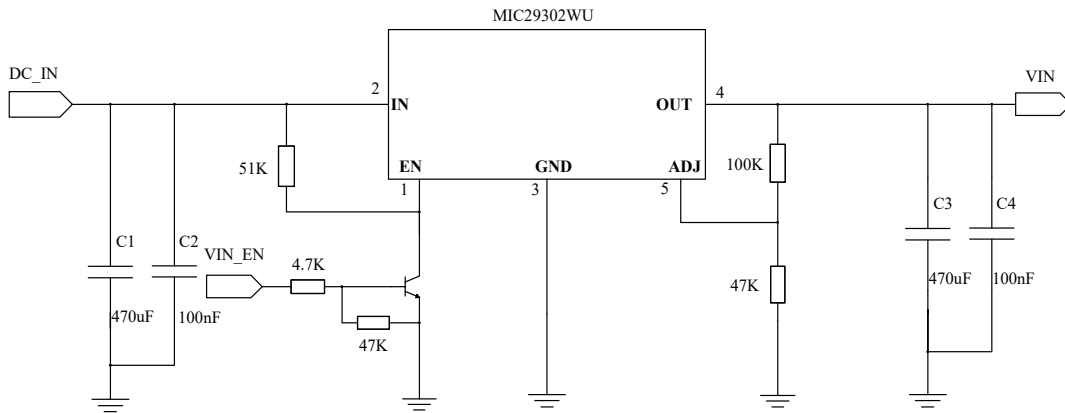


Figure 3-5 Reference design for power supply input

If EXC-N1 module turns on normally, there is a voltage output of 1.8V, current load 80mA in PIN7. You can use the output voltage as an external power supply, for example level reference, and judge if the module is turned on by reading pin level status.

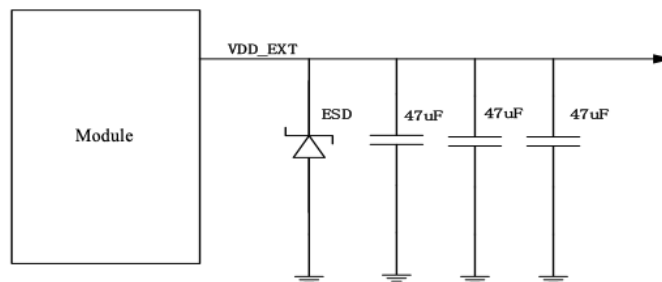


Figure 3-6 VDD_EXT external capacitor and ESD schematic diagram

The following table shows the recommended ESD models for VDD_EXT output:

Table 3-4 VDD_EXT output recommends adding ESD models

Manufacturers	Model	Power consumption	Package
On semi	ESD5Z3.3T1G	200mW	SOD523
Prisemi	PESDNC5D3V3U	150mW	SOD523

 NOTE:



This pin is sensitive to ESD. If this pin is used, please advised to add an ESD component to it for ESD prevention.

To prevent Flash data loss due to frequent module power outages, it is recommended that the customer reserve three 47uF capacitors (0603 or 0805) externally on VDD_EXT, and determine whether to attach capacitors based on actual conditions and scenarios

3.3.2 Logic level

4G LCC Module 1.8V logic level definition as shown in the following table3-5:

Table 3-5

Parameters	Minimum	Typical	Maximum	Unit
1.8V logic level	1.71	1.8	1.89	V
V _{IH}	1.3	1.8	1.89	V
V _{IL}	-0.3	0	0.3	V

The 4G LCC Module 3.3V logic level definition as shown in the following table 3-6:

Table 3-6

Parameters	Minimum	Typical	Maximum	Unit
3.3V logic level	3.135	3.3	3.465	V
V _{IH}	2.3	3.3	3.465	V
V _{IL}	-0.3	0	0.3	V

3.3.3 Power Consumption

The following is the power consumption of EXC-N1 module in each working mode. Please contact us for more product information.

Table 3-6 Power consumption situation

Parameter	Description	Requirement	Typical	Unit
I _{VBAT}	Shutdown mode	Module shutdown leakage	12	uA
	Sleep mode	AT+CFUN=0 (USB disconnect)	2.2	mA
		GSM 900 DRX=2 (USB disconnect)	N/A	mA
		GSM 900 DRX=9 (USB disconnect)		
		DCS1800 DRX=2 (USB disconnect)	N/A	mA
		DCS1800 DRX=9 (USB disconnect)		
GSM 850 DRX=2 (USB disconnect)	N/A	mA		
GSM 850 DRX=9 (USB disconnect)				



		WCDMA Band 1 PF=128 (USB disconnect)	N/A	mA
		WCDMA Band 5 PF=128 (USB disconnect)	2.01	
		WCDMA Band 8 PF=128 (USB disconnect)	N/A	
		WCDMA Band 1 PF=51 (USB disconnect)	N/A	mA
		WCDMA Band 5 PF=512 (USB disconnect)	2.13	
		WCDMA Band 8 PF=512 (USB disconnect)	N/A	
		LTE-TDD Band 38 PF=128 (USB disconnect)	N/A	mA
		LTE-TDD Band 39 PF=128 (USB disconnect)	N/A	
		LTE-TDD Band 40 PF=128 (USB disconnect)	N/A	
		LTE-TDD Band 41 PF=128 (USB disconnect)	2.26	
		LTE-TDD Band 38 PF=256 (USB disconnect)	N/A	mA
		LTE-TDD Band 39 PF=256 (USB disconnect)	N/A	
		LTE-TDD Band 40 PF=256 (USB disconnect)	N/A	
		LTE-TDD Band 41 PF=256 (USB disconnect)	2.34	
		LTE-FDD Band 1 PF=128 (USB disconnect)	N/A	mA
	LTE-FDD Band 3 PF=128 (USB disconnect)	N/A		
	LTE-FDD Band 5 PF=128 (USB disconnect)	2.16		
	LTE-FDD Band 8 PF=128 (USB disconnect)	N/A		
	LTE-FDD Band 20 PF=128 (USB disconnect)	N/A		
	LTE-FDD Band 1 PF=256 (USB disconnect)	N/A	mA	
	LTE-FDD Band 3 PF=256 (USB disconnect)	N/A		
	LTE-FDD Band 5 PF=256 (USB disconnect)	2.13		
	LTE-FDD Band 8 PF=256 (USB disconnect)	N/A		
	LTE-FDD Band 20 PF=256 (USB disconnect)	N/A		
	Idle mode	GSM 900 DRX=5 (USB disconnect)	N/A	mA
		GSM 900 DRX=5 (USB connection)		
		DCS1800 DRX=5 (USB disconnect)	N/A	mA
DCS1800 DRX=5 (USB connection)				
GSM 850 DRX=5 (USB disconnect)		N/A	mA	
GSM 850 DRX=5 (USB connection)				
WCDMA Band 1 PF=64 (USB disconnect)		N/A	mA	
WCDMA Band 1 PF=64 (USB connection)				
WCDMA Band 5 PF= 64 (USB disconnect)		20.2	mA	
WCDMA Band 5 PF= 64 (USB connection)		39.6		
WCDMA Band 8 PF= 64 (USB disconnect)		N/A	mA	
WCDMA Band 8 PF= 64 (USB connection)				
TD-SCDMA Band 34 PF=64 (USB disconnect)	N/A	mA		
TD-SCDMA Band 34 PF=64 (USB connection)				
TD-SCDMA Band 39 PF=64 (USB disconnect)	N/A	mA		
TD-SCDMA Band 39 PF=64 (USB connection)				
LTE-TDD Band 38 PF=64 (USB disconnect)	N/A	mA		
LTE-TDD Band 38 PF=64 (USB connection)				
LTE-TDD Band 39 PF=64 (USB disconnect)	N/A	mA		
LTE-TDD Band 39 PF=64 (USB connection)				



		LTE-TDD Band 40 PF=64 (USB disconnect)	N/A	mA
		LTE-TDD Band 40 PF=64 (USB connection)		
		LTE-TDD Band 41 PF=64 (USB disconnect)	20.5	mA
		LTE-TDD Band 41 PF=64 (USB connection)	43.2	
		LTE-FDD Band 1 PF=64 (USB disconnect)	N/A	mA
		LTE-FDD Band 1 PF=64 (USB connection)		
		LTE-FDD Band 3 PF=64 (USB disconnect)	N/A	mA
		LTE-FDD Band 3 PF=64 (USB connection)		
		LTE-FDD Band 5 PF=64 (USB disconnect)	27.6	mA
		LTE-FDD Band 5 PF=64 (USB connection)	49.2	
		LTE-FDD Band 8 PF=64 (USB disconnect)	N/A	mA
		LTE-FDD Band 8 PF=64 (USB connection)		
		LTE-FDD Band 20 PF=64 (USB disconnect)	N/A	mA
		LTE-FDD Band 20 PF=64 (USB connection)		
	GPRS data transmission (GNSS off)	GSM900 4DL/1UL@30.4dBm	N/A	mA
		GSM900 3DL/2UL@30.4dBm	N/A	mA
		GSM900 2DL/3UL@30.3dBm	N/A	mA
		GSM900 1DL/4UL@30.1dBm	N/A	mA
		DCS1800 4DL/1UL@25.2dBm	N/A	mA
		DCS1800 3DL/2UL@23.7dBm	N/A	mA
		DCS1800 2DL/3UL@23.8dBm	N/A	mA
		DCS1800 1DL/4UL@23.7dBm	N/A	mA
		GSM850 4DL/1UL@30.9dBm	N/A	mA
		GSM850 3DL/2UL@30.8dBm	N/A	mA
		GSM850 2DL/3UL@30.8dBm	N/A	mA
	GSM850 1DL/4UL@30.7dBm	N/A	mA	
	EDGE data transmission (GNSS off)	GSM900 4DL/1UL@27.4dBm	N/A	mA
		GSM900 3DL/2UL@27.2dBm	N/A	mA
		GSM900 2DL/3UL@27.1dBm	N/A	mA
		GSM900 1DL/4UL@26.9dBm	N/A	mA
		DCS1800 4DL/1UL@24.8dBm	N/A	mA
		DCS1800 3DL/2UL@28.8dBm	N/A	mA
		DCS1800 2DL/3UL@24.63dBm	N/A	mA
		DCS 1800 1DL/4UL@23.6dBm	N/A	mA
		GSM 850 4DL/1UL@25.7dBm	N/A	mA
		GSM 850 3DL/2UL@25.3dBm	N/A	mA
		GSM 850 2DL/3UL@25.3dBm	N/A	mA
		GSM 850 1DL/4UL@25.3dBm	N/A	mA
	WCDMA data transmission	WCDMA Band 1 HSDPA@23.274dBm	N/A	mA
		WCDMA Band 1 HSUPA@23.273dBm	N/A	mA
		WCDMA Band 5 HSDPA@23.197dBm	529.6	mA
		WCDMA Band 5 HSUPA@23.197dBm	512.9	mA
WCDMA Band 8 HSDPA@23.374dBm		N/A	mA	
WCDMA Band 8 HSUPA@23.374dBm		N/A	mA	



	LTE data transmission	FDD- LTE Band 1 20M@22.20dBm	N/A	mA
		FDD- LTE Band 3 20M@22.30dBm	N/A	mA
		FDD- LTE Band 5 10M@23.00dBm	556	mA
		FDD- LTE Band 8 10M@23.10dBm	N/A	mA
		FDD- LTE Band 20 10M@22.90dBm	N/A	mA
		TDD- LTE Band 38 20M@23.10dBm	N/A	mA
		TDD- LTE Band 39 20M@23.10dBm	N/A	mA
		TDD- LTE Band 40 20M@23.30dBm	N/A	mA
		TDD- LTE Band 41 20M@23.10dBm	366	mA
	GSM voice call	GSM900 PCL=5 @32.21dBm	N/A	mA
		DCS1800 PCL=0 @28.14dBm	N/A	mA
		GSM850 PCL=5 @32.12dBm	N/A	mA
	CDMA voice call	BC0 @20.31dBm	N/A	mA
	WCDMA voice call	WCDMA Band 1@23.1dBm	N/A	mA
		WCDMA Band 5@22.0dBm	574.3	mA
WCDMA Band 8@22.8dBm		N/A	mA	

3.4 Signal Control Interface

3.4.1 Overview

The signal control part of the interface in the LCC module consists of the following:

- Power-on/off (PWRKEY) pin
- System PMIC reset (RESET_N) pin

Table 3-7 Signal Control Interface

Pin name	Pin NO.	Function	DC features	Description
PWRKEY	21	Turn on/off the module	VIHmax=2.1V VIHmin=1.3V VILmax=0.5V	Due to the diode drop in the chip set, the output voltage of the pin after being charged is 0.8V.
RESET_N	20	Restart the module	VIHmax=2.1V VIHmin=1.3V VILmax=0.5V	

3.4.2 PWRKEY Pin

When EXC-N1 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 100ms. It is suggested that you use an open set driver circuit to control PWRKEY pin. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. Reference circuit is illustrated in the following figure :

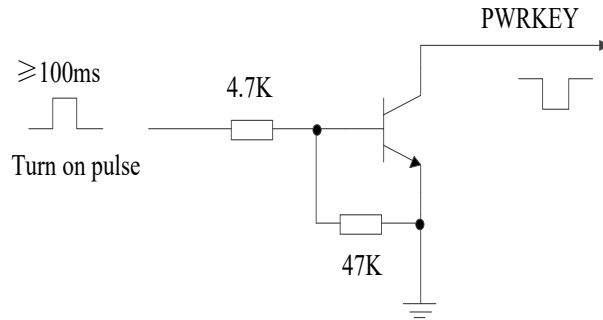


Figure 3-7 Turn on the module using driving circuit

The other way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure:

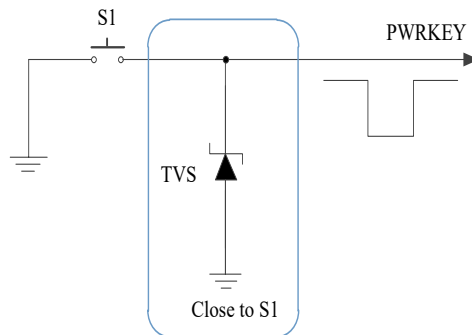


Figure 3-8 Turn on the module using keystroke

Power-On Time Sequence

Turning on time is illustrated as follows:

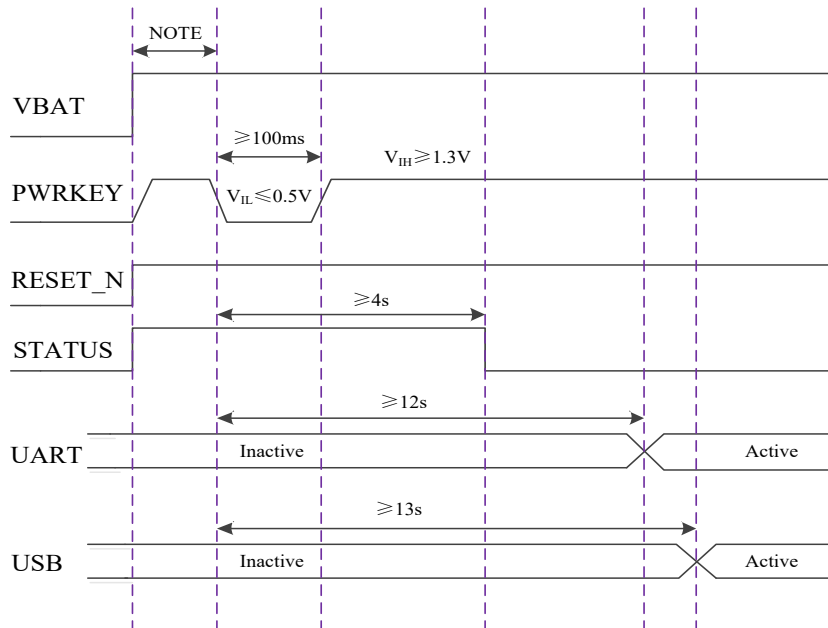


Figure 3-9 Timing of turning on module



NOTE:

Before pulling down PWRKEY pin, VBAT voltage should be guaranteed to be stable. It is recommended that the time interval between powering up VBAT and pulling down PWRKEY pins should be no less than 30ms.

Power-Off Time Sequence

When the module is in boot state, pull down the PWRKEY pin for at least 6.5s and release it. The module will execute shutdown process. The shutdown sequence is shown in the figure below :

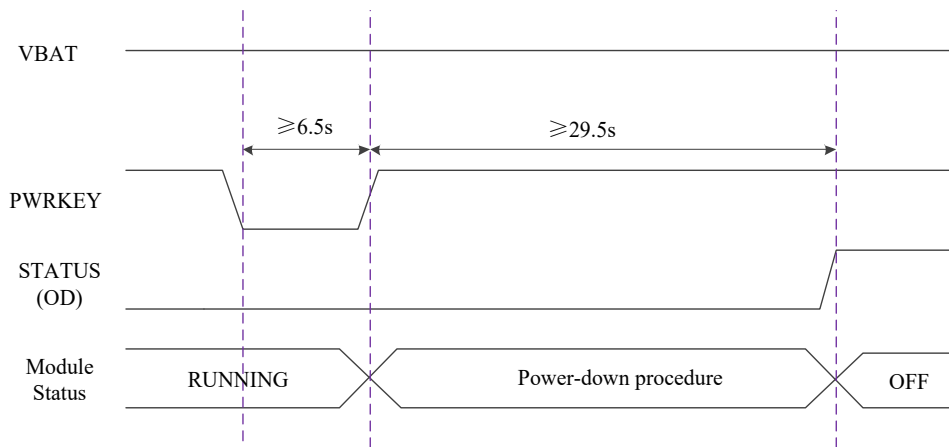


Figure 3-10 Timing of turning off module



NOTE:

1. When the module is working normally, do not immediately cut off the power supply of the module to avoid damaging the Flash data inside the module. It is strongly recommended to close the module through the AT command before disconnecting the power.
2. When using AT command to shut down, make sure that PWRKEY is always in high level state after the shutdown command is executed; otherwise, the module will start up again automatically after the shutdown is completed.

3.4.3 RESET_N Pin

When the module is working, restart the module by pulling down the RESET_N pin for at least 150ms. RESET_N signal is sensitive to interference, so it is suggested that the routing on the module interface board should be as short as possible and should be processed in package.

Reference circuit is as follows: you can use open set driver circuit or button to control RESET_N pin.

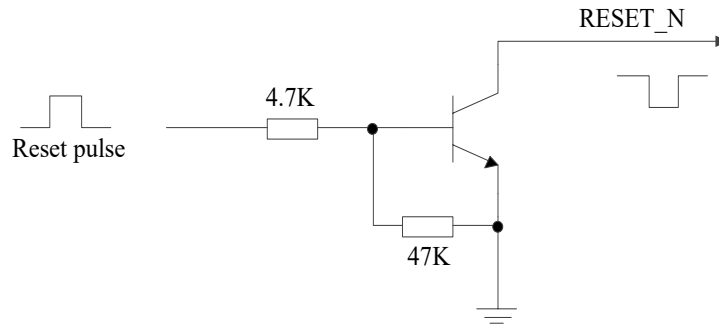


Figure 3-11 Reference circuit of RESET_N by using driving circuit

3.4.4 LED_MODE Signal

N/A

3.4.5 Forced Boot

EXC-N1 supports USB_BOOT functionality. The client can pull USB_BOOT to VDD_EXT(1.8V) before starting the module, and then the module will enter the forced download mode. In this mode, the module can be upgraded via USB interface.

Table 3-8 USB_BOOT pin definition

Pin name	Pin NO.	I/O	Description	Note
USB_BOOT	115	DI	Emergency download mode control, high level in effect	1.8V power domain. It is recommended to reserve test points.

The USB_BOOT interface reference circuit is as follows:

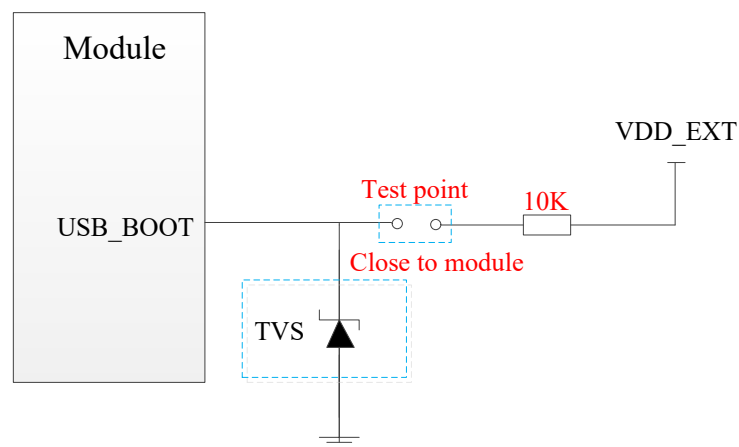


Figure 3-12 USB_BOOT interface reference circuit



3.5 UART Interface

3.5.1 Overview

The EXC-N1 module has two serial ports: main serial port and debugging serial port. The main features of these two serial ports are described below.

- Main serial port to support 9600192, 00384, 00576, 00115, 200230, 400460, 800 baud rate, the default baud rate to 115200bps, support the RTS and CTS flow control. Used for data transfer and AT command transfer;
- Debug serial port supports 115200bps baud rate, control and log print for Linux.

Table 3-9 Main serial port pin description

Pin name	Pin NO.	I/O	Description	Note
RXD	68	DI	ReCompalve data	1.8V power domain.
TXD	67	DO	Transmit data	1.8V power domain.
DTR	66	DO	DTE ready, sleep mode control	1.8V power domain.
RTS	65	DO	DTE requires to transmit data	1.8V power domain.
CTS	64	DI	Clear to send	1.8V power domain.
DCD	63	DI	Output carrier detect	1.8V power domain.
RI	62	DO	Ring indicator	1.8V power domain.

Table 3-10 Debug serial port pin description

Pin name	Pin NO.	I/O	Description	Note
DBG_RXD	11	DI	ReCompalve data	1.8V power supply domain
DBG_TXD	12	DO	Transmit data	1.8V power supply domain

Table 3-11 Serial logic level

Parameter	Min	Max	Unit
VIL	-0.3	0.6	V
VIH	1.2	2.0	V
VOL	0	0.45	V
VOH	1.35	1.8	V

3.5.2 Circuit Recommended for the UART Interface

The serial port level of EXC-N1 module is 1.8V. If the client host is 3.3V, the level converter needs to be added in the serial port application. TI's TXB0104PWR is recommended. The following picture is a reference design:

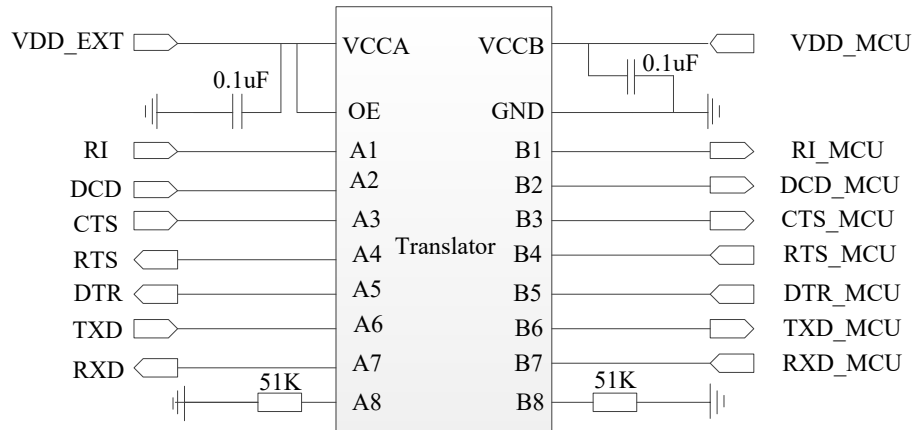


Figure 3-13 Level conversion chip reference circuit



NOTE:

1. It is recommended that customer set the pins related to UART interface as test points on the DTE board for debugging.
2. Keep UART Buses away from sensitive function and trace.

3.6 PCM and I2C Interface

EXC-N1 provides one PCM interface which supports the following two modes:

- Short frame mode: the module works as both master and slave
- Long frame mode: the module works as master only;

In short frame mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge; the PCM_SYNC falling edge represents the more significant bit.

PCM_CLK supports 128, 256, 512, 1024 and 2048kHz speech codes.

In long frame mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge; the PCM_SYNC rising edge represents the more significant bit. The mode only supports 128 kHz PCM_CLK and 8kHz, 50% duty cycle PCM_SYNC.

The EXC-N1 module supports 8-bit A-Law, U-Law and 16-bit linear coding formats. The following two graphs are short frame mode timing diagram (PCM_SYNC= 8KHz, PCM_CLK=2048kHz) and long frame mode timing diagram (PCM_SYNC= 8kHz, PCM_CLK=128kHz).

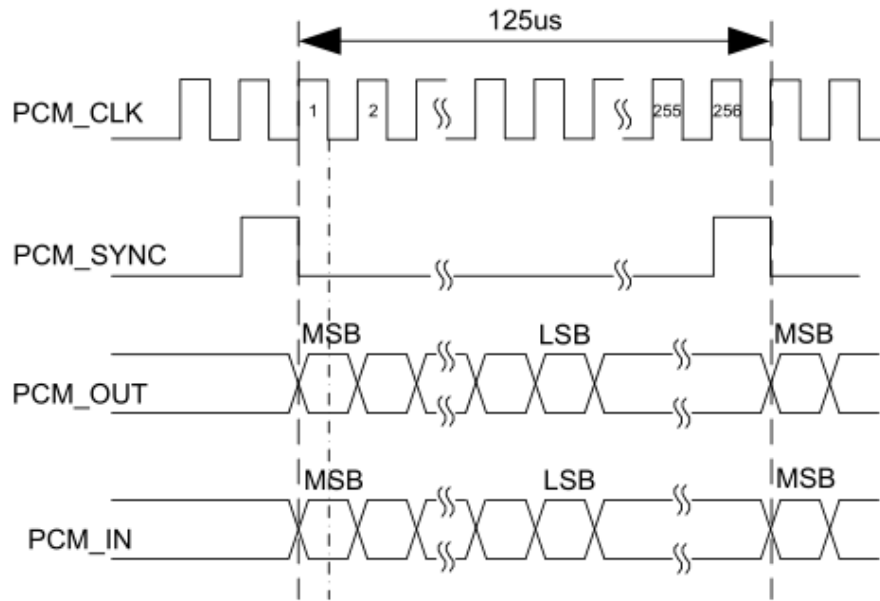


Figure 3-14 Timing in short frame mode

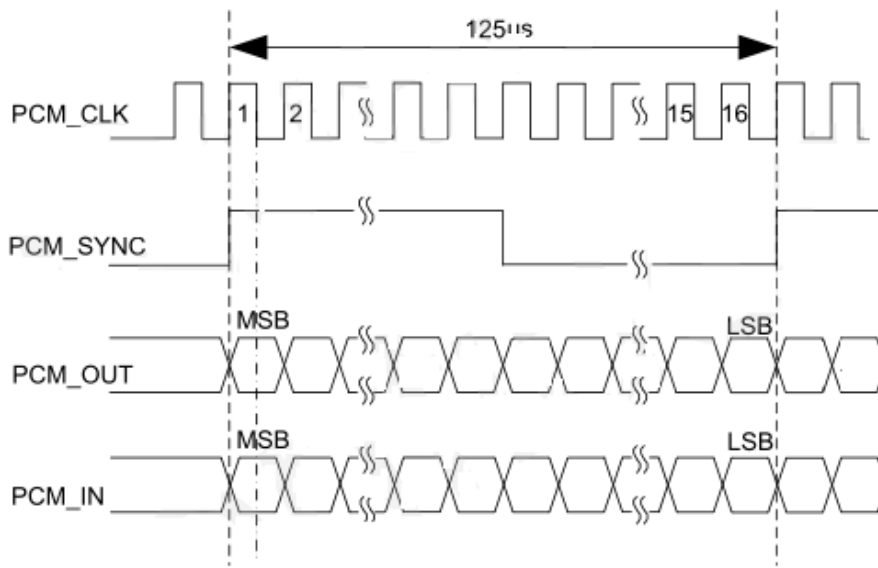


Figure 3-15 Timing in short frame mode

Table 3-12 Pin description for PCM interface

Pin name	Pin number	I/O	Description	Note
PCM_CLK	27	IO	PCM clock	1.8V power supply domain
PCM_OUT	25	DO	PCM data output	1.8V power supply domain
PCM_IN	24	DI	PCM data input	1.8V power supply domain
PCM_SYNC	26	IO	PCM data synchronous signal	1.8V power supply domain
I2C_SCL	41	OD	I2C clock	Require 1.8V external pulling-up
I2C_SDA	42	OD	I2C data	Require 1.8V external pulling-up



CDC_I2S_MCLK	116	DO	19.2MHz clock signal	The 19.2MHz clock signal output by the module is used to provide the clock signal to the external CODEC, otherwise it is suspended
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Below is a reference design for a PCM interface with an external Codec chip :

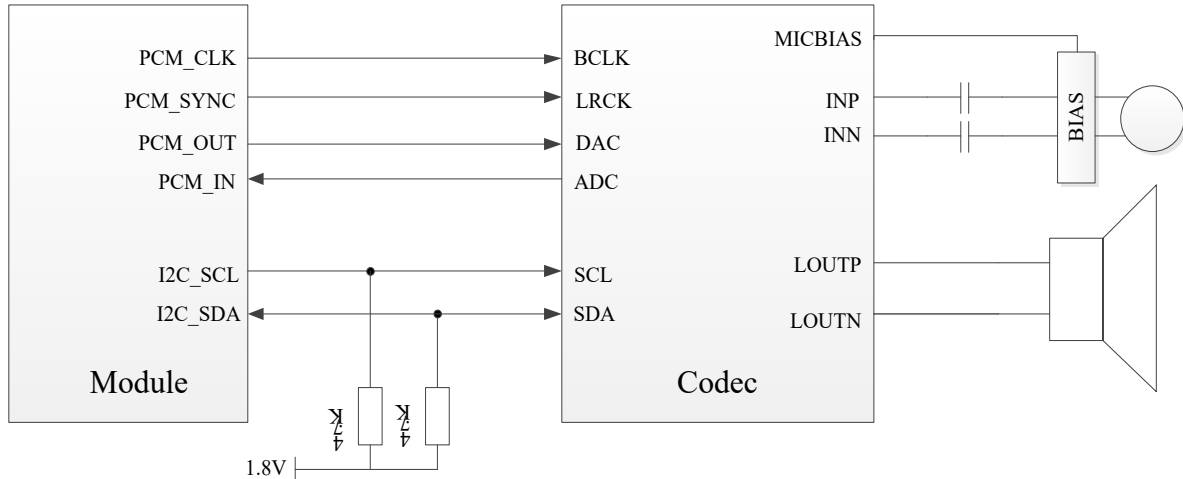


Figure 3-16 PCM circuit reference design

3.7 SPI Interface

N/A

3.8 USB Interface

3.8.1 Overview

The EXC-N1 provides a USB 2.0 compliant interface that supports both high speed (480Mbps) and full speed (12Mbps) modes. This interface is used for AT command interaction, data transfer, software debugging and version upgrading, etc.

3.8.2 USB Interface Definition

The EXC-N1 module provides a USB2.0 high-speed interface.

Table 3-13 USB pin description

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
70	USB_DM	USB differential data signal -			
69	USB_DP	USB differential data signal +			
72	GND	Ground		0	
71	USB_VBUS	USB power supply, used for USB detection	3.0	5.0	5.25



3.8.3 USB Interface Application

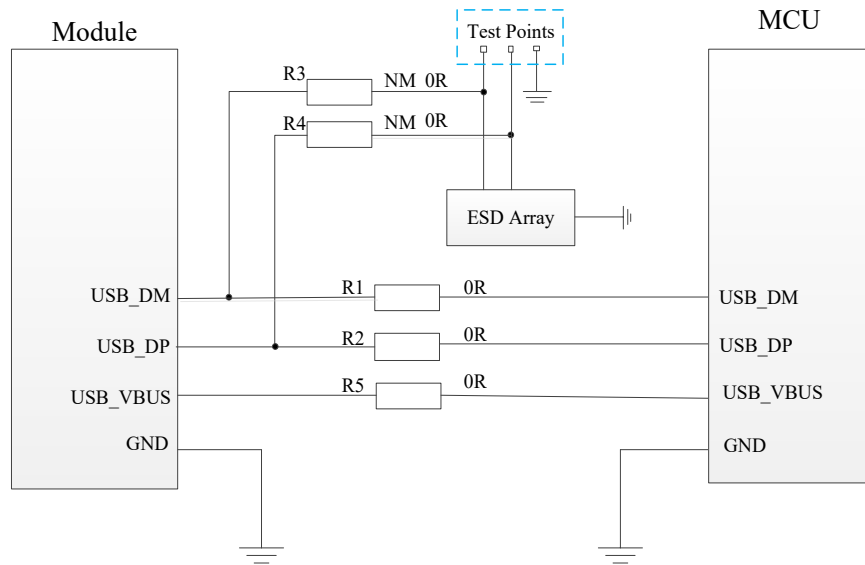


Figure 3-17 USB reference circuit

In order to meet the signal integrity requirement of USB data line, R1/R2/R3/R4 resistors must be placed close to the module and between resistors close to each other. The branch connecting the test point must be as short as possible.

3.8.4 USB Interface Layout Guide

In USB interface circuit design, to ensure USB performance, the following principles are recommended in circuit design :

- The module USB_VBUS is not used to power the module, but to detect USB insertion and unplugging;
- In order to reduce the USB high speed data transmission of signal interference, in USB_DM USB_DP interface circuit and concatenated R1 and R2 can improve the accuracy of data transmission, 0Ω R1 and R2 are recommended;
- In order to improve the antistatic performance of USB interface, ESD protective devices are recommended to be added to USB_DP and USB_DM interface circuits, and ESD devices with junction capacitance less than 2pF are recommended. USB ESD protection device should be placed as close as possible to USB interface;
- In order to ensure the USB work reliable, the design still needs more consideration to the protection of USB, such as the Layout of the protection of the USB, need to do to USB_DP and USB_DM 90 Ω impedance control, strictly in accordance with the requirements of the differential line, as far as possible away from the interference signal;
- Do not use USB cable under crystal oscillator, oscillator, magnetic device and RF signal. It is recommended to use inner differential wiring and wrap the ground left, right, up and down.



EXC-N1 module supports various operating systems, such as PC operating system: Windows 7/8, Windows 10, embedded operating system: Linux version 2.6 or higher, Android2.3/4.0/4.2/4.4/5.0/7.0/5.1/6.0, need special support USB driver.

USB driver for different operating systems, different VID and PID, there are different driver files can be provided, please contact the support staff for specific requirements.

HS-USB guidelines

- External components must be located near the USB connector.
- There are relatively fast edge rates, so they must be routed away from sensitive circuits and signals (RF, audio, and 78.6 MHz XO).
- If a USB connector is used as a charger input: The USB_VBUS node must be routed to the PMIC device using extremely wide traces or sub-planes.

Table 3-14 lists the USB 2.0 Routing Constraints

Metrics			Guidance
Data rate			480 Mbps
Impedance	Differential	Field route	75–105 Ω
Length match	Intralane match		2 mm
Maximum PCB trace length			250 mm
Spacing	To other signals	Field route	3 \times line width

3.9 PCIe Interface

N/A

3.9.1 Overview

3.9.2 PCIe Interface Definition

3.9.3 PCIe Interface Application

3.10 USIM Card Interface



3.10.1 Overview

USIM card interface meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V USIM cards are supported by EXC-N1.

Table 3-15 USIM/SIM interface

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
13	USIM_PRESENCE	SIM card plug detection		1.8	
14	USIM_VDD	USIM card power supply		1.8/3.0	
15	USIM_DATA	USIM card data signal		1.8/3.0	
16	USIM_CLK	USIM card clock signal		1.8/3.0	
17	USIM_RST	USIM card reset signal		1.8/3.0	
10	USIM_GND			0	

3.10.2 Circuit Recommended for the USIM Card Interface

The EXC-N1 module supports USIM card hot-swap through USIM_PRESENCE pin, supports high level detection, and the default hot-swap function is turned off. In the figure, the USIM_PRESENCE pin level is high after the SIM card holder is inserted. When no card is detected, the USIM_PRESENCE pin level is low.

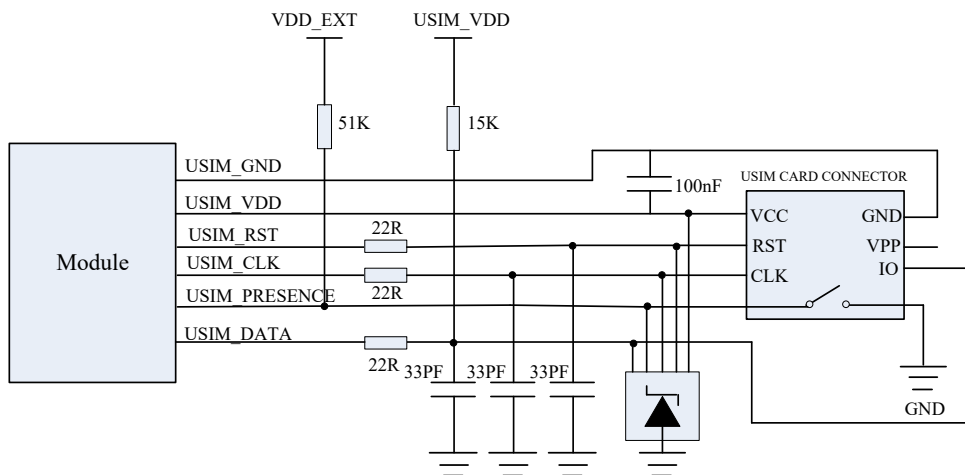


Figure 3-18 Reference circuit for 8-pin USIM/SIM connector

If USIM card detection is not required, keep the USIM_PRESENCE pin suspended. The figure below is the 6-PIN USIM socket interface reference circuit :

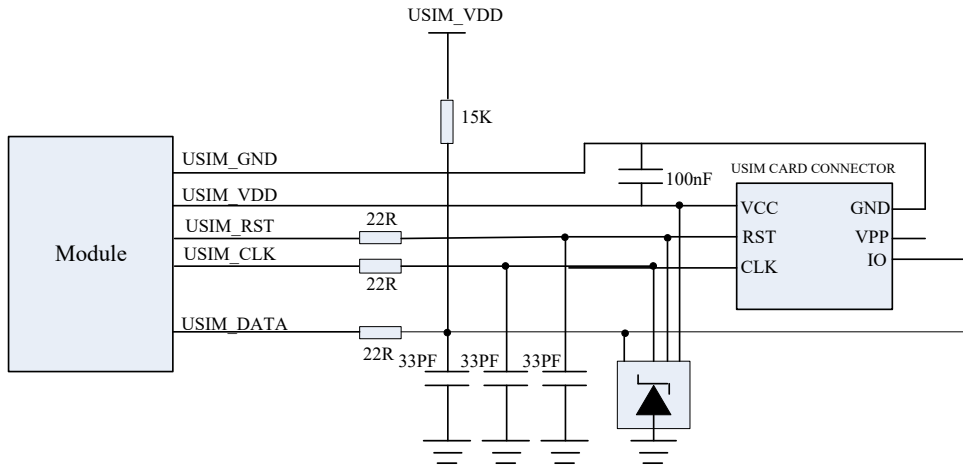


Figure 3-19 Reference circuit for 6-pin USIM/SIM connector

In order to enhance the reliability and availability of the USIM card in your application, please follow the criteria below in the USIM circuit design :

- USIM_DATA requires a pull-up resistor of 15kΩ to USIM_VCC; the pull-up resistor helps to increase SIM card's anti-interference ability. When USIM card trace is too long or it is close to the interference source, it is recommended that you add a pull-up resistor near the card.
- In order to suppress stray EMI and enhance ESD protection, it is recommended to connect a resistance of 22Ω on USIM_DATA, USIM_CLK and USIM_RESET line;
- In order to improve the antistatic ability and offer good ESD protection, it is recommended to add TVS whose parasitic capacitance should be less than 15pF on USIM_VCC, USIM_DATA, USIM_CLK and USIM_RESET line;
- In order to filter GSM900 interference, add a parallel 33pF resistance on USIM_VCC, USIM_DATA, USIM_CLK and USIM_RESET line;
- Keep layout of USIM card as close as possible to the module. Assure the length of signal wiring is less than 200mm;
- Keep USIM card signal away from RF and VBAT power line;
- To avoid cross-talk between USIM_CLK and USIM_DATA, keep them away from each other and shield them with surrounded ground;

For the USIM/SIM card hot-plugging function, the hot plugging pin is used to DETECT the pin and the Pin13 pin of the module. The default hot plug function is off. Please contact us for more details. Note: Hot plug-unsupported SIM Connectors May cause damage to USIM /SIM card or EXC-N1 USIM /SIM interface if the SIM Connectors do not support hot plug-back.



NOTE:



- The requirements for detection mechanisms of SIM detect pin, it is consider Low to High as triggered. So, please make sure that the selected SIM socket can meet these design specifications. (Active Low)
- Keep USIM Buses away from sensitive function and trace; and although USIM is slow, but recommend make DATA to clock to 2x space if possible and 50 ohm impedance control.
- The length of the SIM bus needs to be based on the condition that can meet the ISO/IEC 7816-3 SI quality, it is recommended not to exceed 3300mil. (for reference data)



CAUTION

- To meet the requirements of 3GPP TS 51.010-1 protocols and electromagnetic compatibility (EMC) authentication, the USIM socket should be placed near the LCC interface (it is recommended that the PCB circuit connects the LCC interface and the USIM socket does not exceed 100 mm), because a long circuit may lead to wave distortion, thus affecting signal quality.
- It is recommended that you wrap the area adjacent to the USIM_CLK and USIM_DATA signal wires with ground. The Ground pin of the USIM socket and the Ground pin of the USIM card must be well connected to the power Ground pin supplying power to the module.
- A 100nF capacitor (0402 package is recommended so that greater capacitance such as 1 μ F can be employed if necessary) and a 33 pF capacitor are placed between the USIM_VCC and Ground pins in parallel. Three 33 pF capacitors are placed between the USIM_DATA and Ground pins, the USIM_RESET and Ground pins, and the USIM_CLK and Ground pins in parallel to filter interference from RF signals.
- USIM_DATA is already pulled up internally.
- It is recommended to take electrostatic discharge (ESD) protection measures near the USIM card socket. The TVS diode with Vrwm of 5 V and junction capacitance less than 10 pF must be placed as close as possible to the USIM socket, and the Ground pin of the ESD protection component is well connected to the power Ground pin that supplies power to the module.
- The ESD protection component should choose low capacitance. The capacitance of the component should be lower than **10pF**.

3.11 Audio Interface

N/A

3.12 General Purpose I/O Interface (Reserved GPIO)

The LCC module provides GPIO pins for customers to use for controlling signals which are worked at 1.8 V CMOS logic levels, it can be release as a GPIO pin when charging function is no use. Customers can use AT command to control the state of logic levels of GPIO output signal. About the details of GPIO command see the Compal LCC LTE Module AT Command



Interface Specification.

It is recommended that a TVS be used on the related interface such as interrupt/reset pin, to prevent electrostatic discharge and protect integrated circuit (IC) components.

3.13 JTAG Interface

N/A

3.14 RF Antenna Interface

The LCC module provides three antenna pads (Main / DIV / GNSS) for connecting the external antennas.

The RF pad difference is the most important difference between LCC modules; please refer to 29 mm x 32 mm LCC Module Hardware Migration Guide.

Route the antenna pad as close as possible to antenna connector. In addition, the impedance of RF signal traces must be 50 Ω .

EXC-N1 module is designed with a main antenna interface, a diversity reCompalving antenna interface (used to suppress signal drops due to high-speed movement and multipath) and a GNSS antenna interface. The impedance of antenna interface is 50 Ω .

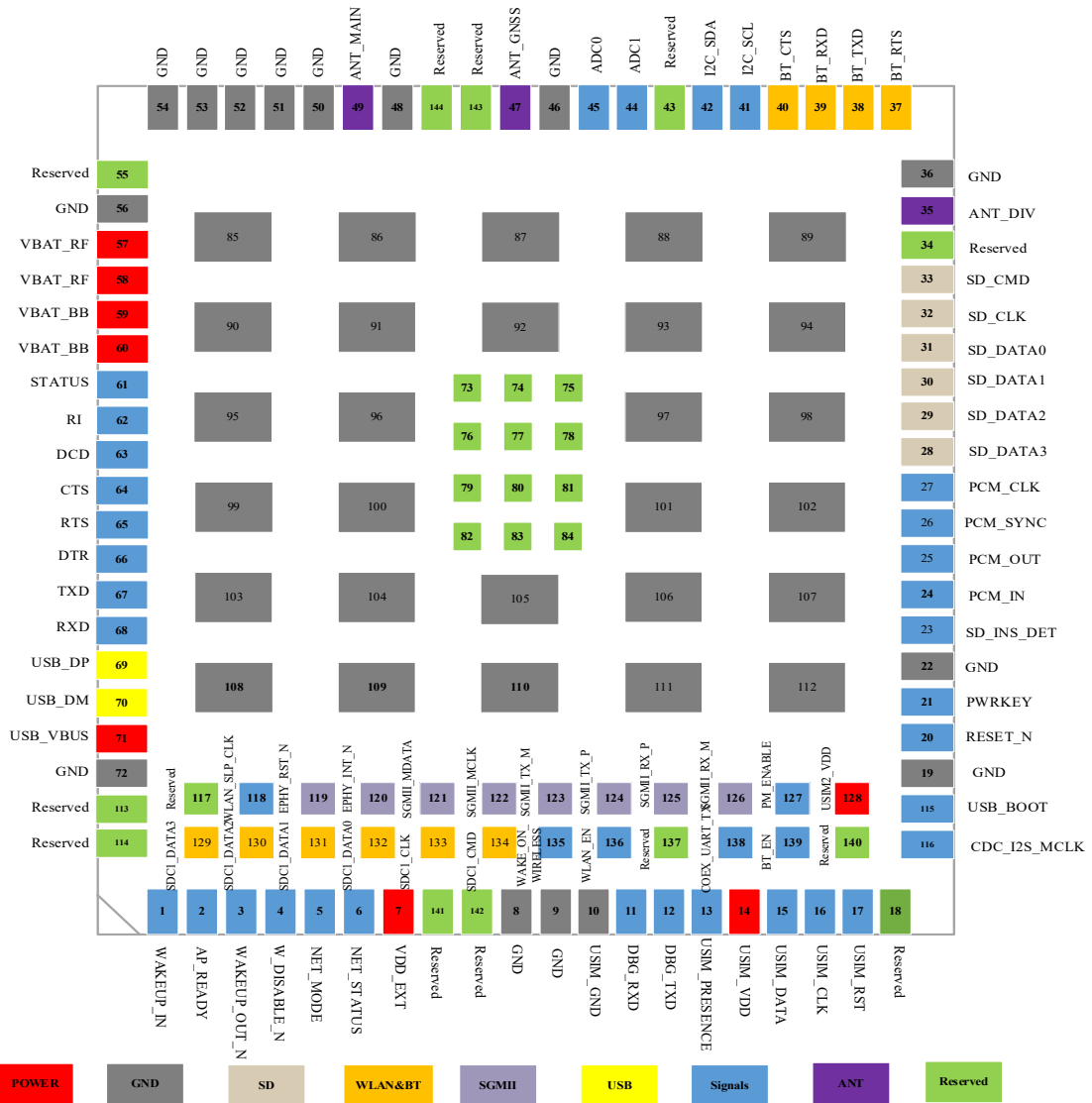


Figure 3-20 Definition of the antenna pinout location (Perspective View from TOP Side)

Table 3-16 Definition of the antenna port mapping

Pin Name	Pin Number	Description	I/O	Note
ANT_MAIN	49	Main antenna	IO	50Ω impedance
ANT_DIV	35	Diversity reCompalving antenna interface	AI	50Ω impedance
ANT_GNSS	47	GNSS antenna interface	AI	50Ω impedance

Supported air Interfaces for each of band groups are listed in the following table 3-17.

Table 3-17



Band Group	Fmin (MHz)	Fmax (MHz)	Air Interface
LB	600	960	WCDMA: N/A LTE FDD: B5/12/13/14/26/ LTE TDD: N/A
MB	1427.9	2170	WCDMA: N/A LTE FDD: B2/4/25/66 LTE TDD: N/A
HB	2300	2690	WCDMA: N/A LTE FDD: B7 LTE TDD: B41M
UHB	3000	6000	WCDMA: N/A LTE FDD: N/A LTE TDD: N/A

3.14.1 RF Connector Characteristic

Table 3-18

Rated Condition		Environment Condition
Frequency Range	DC to 6GHz	Temperature Range
Characteristic Impedance	50Ω	-40°C to +85°C

3.14.2 RF Connector Dimension

N/A

3.15 Reserved Interface

The LCC module provides some reserved pins in the section 3.13. All reserved pins cannot be used by the customer. All of them must be leave unconnected.

Table 3-19 reserved lists pins signal

Pin	Pin Name	I/O	Pin Description	DC Parameter(V)
-----	----------	-----	-----------------	-----------------



				Minimum Value	Typical Value	Maximum Value
18, 34, 43, 55, 73~84, 113, 114, 117, 137, 140~144	NC	NA	Please keep these pins open.			

3.16 NC Interface

N/A

3.17 Tunable Antenna Control

N/A

3.18 Network status indication

The network status indicator pin is mainly used to drive the network status indicator light (it is necessary to switch the LED light on and off by controlling the audion and off, instead of directly driving the LED light). The EXC-N1 module has NET_MODE and NET_STATUS. The following two tables describe the pin definition and logic level changes in different network states.

Table 3-20 Network indicator pin description

Pin name	Pin number	I/O	Description	Note
NET_MODE	5	DO	Indicate the module network registration mode.	
NET_STATUS	6	DO	Indicate the module network activity status.	

Table 3-21 The network indicates the working status of pins

Mode	Status	Description
NET_MODE	High level	Register LTE network status
	Low level	Others
NET_STATUS	Scintillation (200ms high /1400ms low)	Digital state
	High level	Register network success
	Low level	Other

The reference circuit is shown in the figure below :

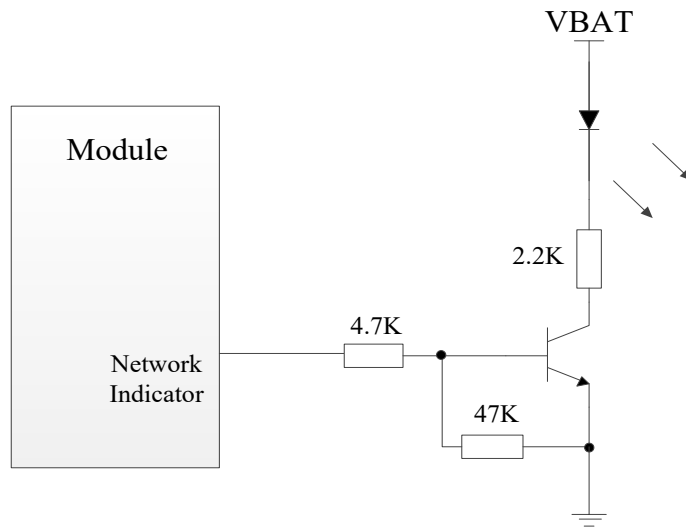


Figure 3-21 Network indication reference design drawing

3.19 Status

STATUS is used to indicate the working STATUS of the module. It is the open-leak output pin. The customer can refer to the LED indicating circuit as shown in the following figure. When the module is normally started, the STATUS will output the low level. Otherwise, the STATUS becomes high impedance.

Table 3-22 STATUS pin description

Pin name	Pin number	I/O	Description	Note
STATUS	61	Indicates the working status of the module	OD	Need an external pull-up

The following figure shows the STATUS reference circuit design :

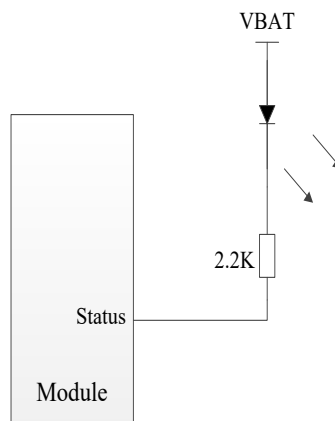




Figure 3-22 STATUS reference circuit

3.20 ADC Interface

EXC-N1 provides a 2-way analog-digital conversion interface. The voltage value of ADC0 can be read by using AT+ADCREAD=1, and the voltage value of ADC1 can be read by using AT+ADCREAD= 6.

In order for ADC voltage measurement accuracy to be higher, the ADC needs to be processed in packet during wiring.

Table 3-23 ADC pin description

Pin name	Pin no.	Description	Voltage range	Resolution
ADC0	45	Analogy to digital converter interface 0	0.1 –1.7V	15bits
ADC1	44	Analogy to digital converter interface 1	0.1 – 1.7V	15bits

3.21 SGMII interface

The EXC-N1 module includes an integrated Ethernet MAC SGMII interface and two management interfaces (MDIO). The main features of the SGMII interface are as follows :

- IEEE802.3 compliance;
- Full duplex at 1000Mbps;
- Half/full duplex for 10/100Mbps;
- Support VLAN tagging;
- Support IEEE1588 and Precision Time Protocol (PTP);
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch;
- MDIO supports dual voltage 1.8V/2.85V;

Table 3-24 SGMII interface pin description

Pin name	Pin no.	I/O	Description	Comment
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8V/2.85V power domain.
EPHY_INT_N	120	DI	Ethernet PHY interruption	1.8V/2.85V power domain.
SGMII_MDATA	121	IO	SGMII MDIO data	1.8V/2.85V power domain.
SGMII_MCLK	122	DO	SGMII MDIO clock	
USIM2_VDD	128	PO	SGMII MDIO power supply	1.8V/2.85V power domain, require external pull-up level for SGMII SDIO Pin



SGMII_TX_M	123	AO	SGMII data transmit negative signals	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	124	AO	SGMII data transmit positive signals	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	125	AI	SGMII data reCompalve positive signals	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_M	126	AI	SGMII data reCompalve negative signals	Connect with a 0.1uF capacitor, close to the PHY side.

The following diagram shows the application block diagram of Ethernet:

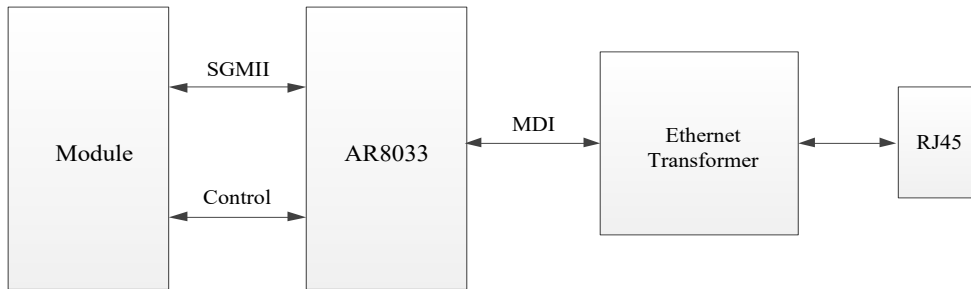


Figure 3-23 Ethernet Application diagram

The following figure shows the application reference circuits of module SGMII and PHY AR8033 :

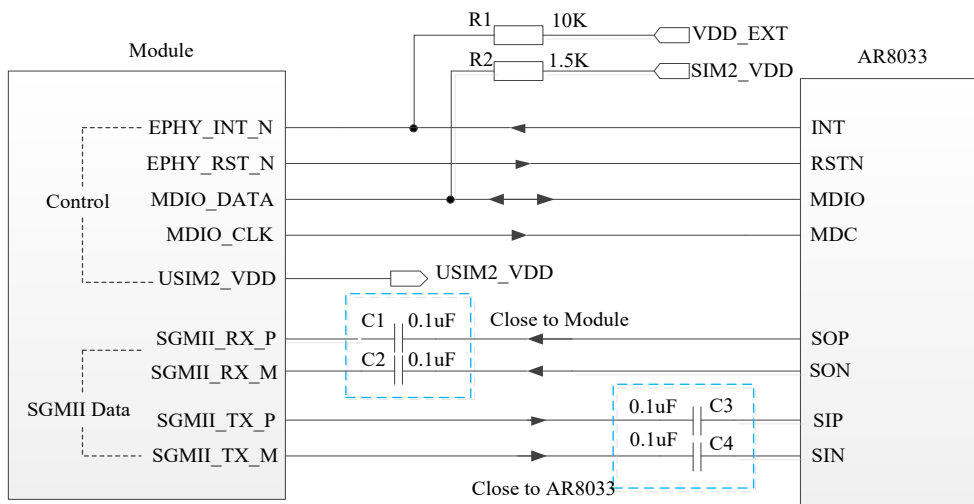


Figure 3-24 SGMII interface and PHY AR8033 application circuit diagram

In order to improve the reliability of customers in the application, please follow the standard Ethernet PHY circuit design. The main points to note are as follows :

- Keep SGMII data and control signal lines away from RF and VBAT when wiring;



- The maximum line length shall not exceed 25.4cm, and the difference line shall be less than 0.7mm;
- SGMII cable differential impedance control in $100\ \Omega \pm 10\%$, and guarantees the complete reference to the ground plane;
- SGMII RX/TX spacing should be at least 3 times line width, and SGMII signals should be at least 3 times line width from other signal lines;
- The SGMII RX module has 0.1UF capacitor, which does not need to be added externally.

3.22 Wireless Connectivity Interfaces

The EXC-N1 module provides a low-power SDIO 3.0 interface for WLAN design and a serial port and PCM interface for Bluetooth design.

The pins of the wireless connection interface are defined in the following table :

The following figure is the connection reference figure of the wireless connection interface and EVB module:

Table 3-25 The pin description of the wireless connection interface

WLAN part				
Pin name	Pin NO.	I/O	Description	Note
SDC1_DATA3	129	IO	WLAN SDIO signal data line 3	1.8V power domain.
SDC1_DATA2	130	IO	WLAN SDIO signal data line 2	1.8V power domain.
SDC1_DATA1	131	IO	WLAN SDIO signal data line 1	1.8V power domain.
SDC1_DATA0	132	IO	WLAN SDIO signal data line 0	1.8V power domain.
SDC1_CLK	133	DO	WLAN SDIO signal clock	1.8V power domain.
SDC1_CMD	134	DO	WLAN SDIO instruction signal	1.8V power domain.
WLAN_EN	136	DO	WLAN enables	1.8V power domain. Active high level.
Coexistence and control part				
Pin name	Pin NO.	I/O	Description	Note
PM_ENABLE	127	DO	External power control	1.8V power domain.
WLAN_SLP_CLK	118	DO	WLAN sleep clock	32kHz clock output by module
WAKE_ON_WIRELESS	135	DI	WLAN wakes up the module	1.8V power domain.



BT part				
Pin name	Pin NO.	I/O	Description	Note
BT_EN	139	DO	Bluetooth enables.	1.8V power domain. Active high level.
BT_RTS	37	DO	DTE requires to transmit data	1.8V power domain.
BT_TXD	38	DO	Transmit data	1.8V power domain.
BT_RXD	39	DI	ReCompalve data	1.8V power domain.
BT_CTS	40	DI	Clear to send	1.8V power domain.
PCM_IN	24	DI	Bluetooth PCM data input.	1.8V power domain.
PCM_OUT	25	DO	Bluetooth PCM data output.	1.8V power domain.
PCM_SYNC	26	IO	Bluetooth PCM data synchronous signal.	1.8V power domain.
PCM_CLK	27	IO	Bluetooth PCM clock.	1.8V power domain.

The following figure is the connection reference figure of the wireless connection interface and EVB module:

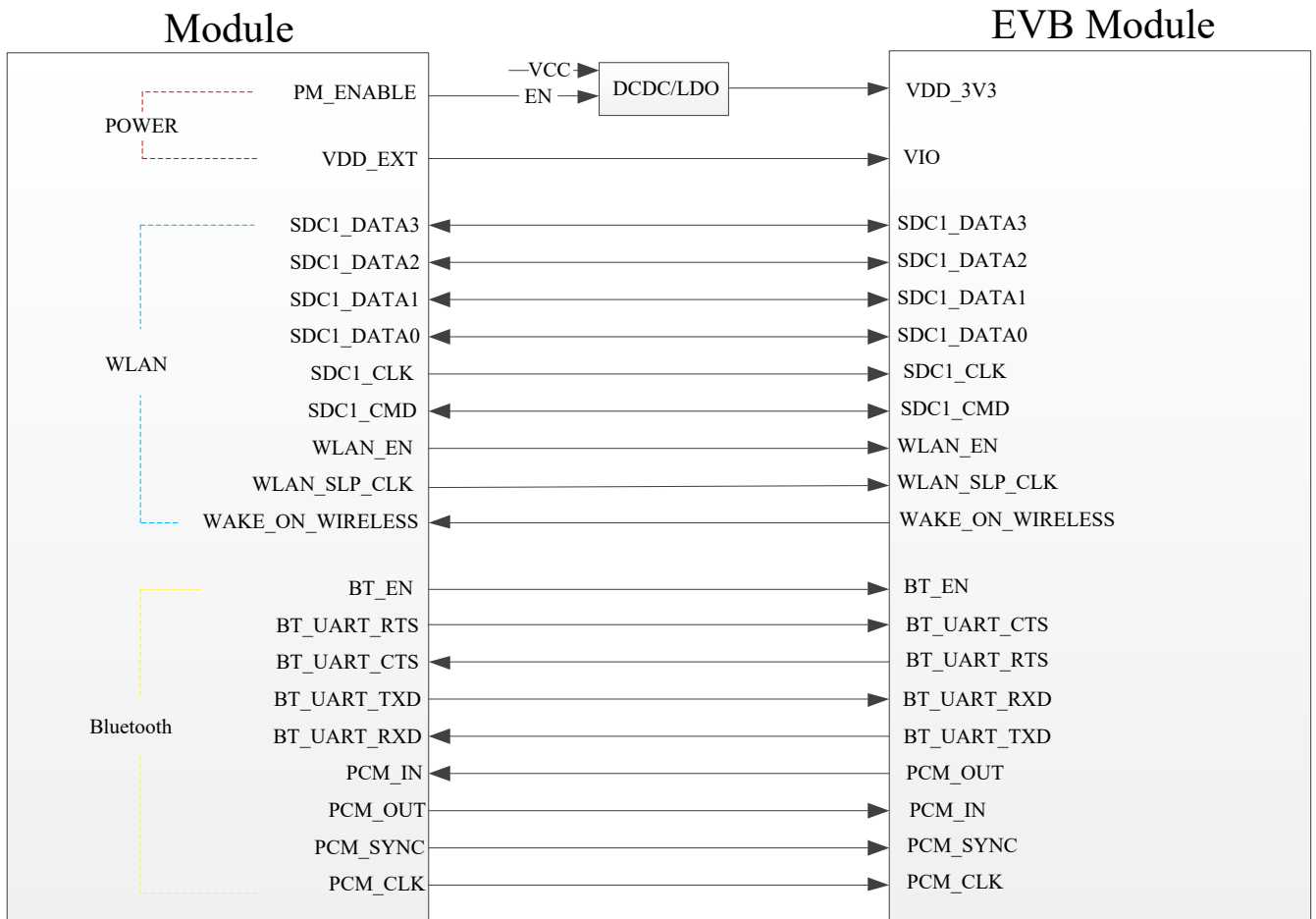


Figure 3-25 Wireless interface and EVB connected to the reference circuit



NOTE:

1. EVB module can only be used as slave equipment;
2. PCM_SYNC and PCM_CLK are only used for signal output when the EXC-N1 module enables Bluetooth functionality;
3. 24~27 pins are multiplexed pins that can be used for Codec voice or to connect THE EXC-N1 PCM for Bluetooth voice communication.

3.22.1 WLAN Interface

The EXC-N1 module provides a low-power SDIO 3.0 WLAN and a control interface.

The SDIO interface supports a single rate mode with a maximum frequency of 50MHz.

SDIO interface rate is very high. In order to ensure that the interface design conforms to THE SDIO 3.0 specification, the following principles are recommended in circuit design :

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is $50\Omega (\pm 10\%)$;
- SDIO signal lines should be away from sensitive signals, such as RF circuits, analog signals, and noise signals, such as clock signals and DCDC signals;
- It is recommended to keep the wire length difference between CLK and DATA/CMD less than 1mm and the total length less than 50mm;
- Close to the module of the clock signal on the series resistance matching between 15 -24 Ω , and resistance from the module's walk line not more than 5 mm.

3.22.2 BT Interface

The EXC-N1 module provides a proprietary UART interface and a PCM interface for bluetooth interfaces.

Table 3-26 Bluetooth interface pin description

Pin name	Pin NO.	I/O	Description	Note
BT_EN	139	DO	Bluetooth enables.	1.8V power domain. Active high level.
BT_RTS	37	DO	DTE requires to transmit data	1.8V power domain.
BT_TXD	38	DO	Transmit data	1.8V power domain.
BT_RXD	39	DI	ReCompalve data	1.8V power domain.
BT_CTS	40	DI	Clear to send	1.8V power domain.
PCM_IN	24	DI	Bluetooth PCM data input.	1.8V power domain.
PCM_OUT	25	DO	Bluetooth PCM data output.	1.8V power domain.
PCM_SYNC	26	IO	Bluetooth PCM data synchronous signal.	1.8V power domain.
PCM_CLK	27	IO	Bluetooth PCM clock.	1.8V power domain.



3.23 SD card interface

The SD card interface of EXC-N1 module supports the SDIO 3.0 protocol. Interface pins are defined in the following table:

Table 3-27 SD card interface pin description

Pin name	Pin NO.	I/O	Description	Note
SD_CMD	33	IO	SD card SDIO instruction signal	SDIO signal level can be selected according to the signal level supported by SD card. Please refer to SD3.0 protocol for details.
SD_CLK	32	DO	SD card SDIO clock signal	
SD_DATA0	31	IO	SD card SDIO signal data line 3	
SD_DATA1	30	IO	SD card SDIO signal data line 2	
SD_DATA2	29	IO	SD card SDIO signal data line 1	
SD_DATA3	28	IO	SD card SDIO signal data line 0	
SD_INS_DET	23	DI	SD card insertion detection	

The following is the SD card reference design:

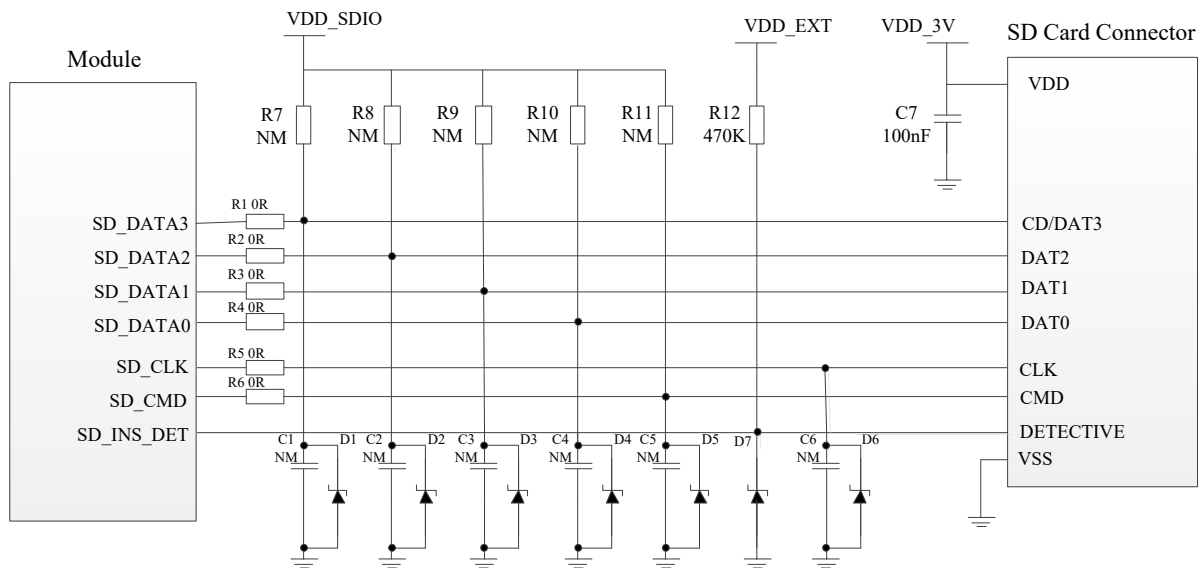


Figure 3-26 SD card reference design

In the circuit design of SD card interface, in order to ensure the good performance and reliability of SD card, the following principles are recommended in the circuit design :

- The voltage range of SD card power supply VDD_3V is 2.7~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card;



- To maximally limit the surge current caused by SD card insertion, the bypass capacitor (C7) of SD card power source should not exceed 5uF;
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. The value of these resistors is among 10~100kohm and the recommended value is 100kohm.
- In order to improve signal quality, it is recommended to add 0 ohm resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved with no mounting by default. All resistors and bypass capacitors should be placed close to the module;
- In order to better prevent static electricity, TVS tube is suggested to be added on the Pin of SD card. It should be placed as close as possible to The SD card seat and ensure that the inter-pole capacitance of TVS is less than 15pF;
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 ohm ($\pm 10\%$);
- SDIO signal lines need to stay away from other sensitive signals, such as RF, analog signals, and the clock signal and noise signal such as DCDC.
- It is recommended to keep the wire length difference between CLK and DATA/CMD less than 1mm and the total length less than 50mm. The wiring length in the module is 27mm, so the outer wiring length should be less than 23mm;
- Make sure that adjacent lines are spaced twice the width of the line and that the bus load is less than 15pF.



4 Radio Frequency

4.1 Overview

This chapter describes the RF specifications of the LCC module, including:

- Operating Frequencies
- Conducted Rx Sensitivity and Tx Power
- Antenna Design Requirements

4.2 Operating Band

Table 4-1 EXC-N1-SK1 Working Frequency

3GPP Frequency band	Transmit	ReCompalve	Unit
WCDMA B2	1850-1910	1930-1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE-FDD B2	1855~1905	1935~1985	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5	829~844	874~889	MHz
LTE-FDD B7	2505-2565	2626-2685	MHz
LTE-FDD B12	704-711	734~741	MHz
LTE-FDD B13	782	751	MHz
LTE-FDD B17	709~711	739~741	MHz
LTE-FDD B25	1855~1910	1935~1990	MHz
LTE-FDD B26	819~844	864~889	MHz
LTE-TDD B41M	2560~2650	2560~2650	MHz
LTE-TDD B66	1710-1780	2110-2200	MHz

4.3 ReCompalver Sensitivity

Table 4-2 EXC-N1-SK1 Module RF ReCompalving Sensitivity

Frequency	ReCompalving sensitivity (typical value) -10M			
	Main	Diversity	Main + Diversity	3GPP (Main + Diversity)
WCDMA B2	-109dBm	-110dBm	-112dBm	-104.7dBm
WCDMA B4	-109dBm	-110dBm	-112dBm	-106.7dBm
WCDMA B5	-109.5dBm	-110dBm	-113dBm	-104.7dBm
LTE-FDD B2	-98dBm	-99dBm	-101.5dBm	-94.3dBm
LTE-FDD B4	-98dBm	-99dBm	-101.5dBm	-96.3dBm
LTE-FDD B5	-99dBm	-99dBm	-102dBm	-94.3dBm



LTE-FDD B7	-96.5dBm	-97dBm	-99.5dBm	-94.3dBm
LTE-FDD B12	-99dBm	-99dBm	-102dBm	-93.3dBm
LTE-FDD B13	-99dBm	-99dBm	-102dBm	-93.3dBm
LTE-FDD B17	-99dBm	-99dBm	-102dBm	-93.3dBm
LTE-FDD B25	-98dBm	-99dBm	-101.5dBm	-94.8dBm
LTE-FDD B26	-99dBm	-99dBm	-102dBm	-94.8dBm
LTE-TDD B41M	-97.5dBm	-96.5dBm	-100.5dBm	-94.3dBm
LTE-TDD B66	-98dBm	-99dBm	-101.5dBm	-96.3dBm

4.4 GNSS

The EXC-N1 series includes a complete built-in GNSS solution that supports Qualcomm Gen8C-Lite (GPS, Glonass, Galileo, BeiDou).

EXC-N1 series modules support the standard NMEA-0183 protocol and output 1Hz NMEA statements via USB interface by default.

The following table lists the GNSS performance of EXC-N1 series modules.

Table 4-3 GNSS performance list

Parameter	Description	Performance index
Positioning accuracy (open)	CEP-50	<5m
First positioning time TTFF (open)	Cold start	32s
	Warm start	29s
	Hot start	2s
Sensitivity	Cold star	-146dBm
	Capturing	-157dBm
	Tracking	-157dBm

You need to follow the layout guidelines in the below when designing:

- Maximize the distance between the GNSS antenna, the main antenna and the diversity antenna.
- Noisy digital circuits such as the USIM card, USB interface, Camera module, Display connector and SD card should be kept away from the antenna.
- Use ground via around the GNSS trace and sensitive analog signal traces to provide isolation and protection.
- Keep 50ohm characteristics impedance of the ANT_GNSS trace.
- In case of any static electricity or lightning strikes, reserve a place for TVS on the backplane.



4.5 Antenna Design

4.5.1 Interference

Besides the antenna performance, the interference on the user board also affects the radio performance (especially the TIS) of the module. To guarantee high performance of the module, the interference sources on the user board must be properly controlled.

On the user board, there are various interference sources, such as the LCD, CPU, audio circuits, and power supply. All the interference sources emit interference signals that affect the normal operation of the module. For example, the module sensitivity can be decreased due to interference signals.

Therefore, during the design, you need to consider how to reduce the effects of interference sources on the module.

You can take the following measures: Use an LCD with optimized performance; shield the LCD interference signals; shield the signal cable of the board; or design filter circuits.

Recommend to add TVS component in Antenna pin to avoid ESD.

Compal is able to make technical suggestions on radio performance improvement of the module.

4.5.2 Antenna Requirements

The antenna for LCC module must fulfill the following requirements:

Table 4-4 Antenna Requirements

Antenna Requirements	
Frequency range	Depending on frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
Bandwidth of primary antenna	70 MHz in GSM 850 80 MHz in GSM 900 170 MHz in GSM 1800 140 MHz in GSM 1900 250 MHz in WCDMA /LTE Band 1 140 MHz in WCDMA/LTE Band 2 70 MHz in WCDMA/LTE Band 5 80 MHz in WCDMA/LTE Band 8 170 MHz in LTE Band 3 190 MHz in LTE Band 7 71 MHz in LTE Band 20



Antenna Requirements	
Bandwidth of secondary antenna	60 MHz in WCDMA/LTE Band 1 60 MHz in WCDMA/LTE Band 2 25 MHz in WCDMA/LTE Band 5 35 MHz in WCDMA/LTE Band 8 75 MHz in LTE Band 3 70 MHz in LTE Band 7 30 MHz in LTE Band 20
Bandwidth of GPS antenna	35 MHz in GNSS
Gain	≤ 2.5 dBi (≥ 3 dBi for GPS antenna)
Impedance	50 Ω
VSWR absolute max	$\leq 3:1$ ($\leq 2:1$ for GPS antenna)
VSWR recommended	$\leq 2:1$ ($\leq 1.5:1$ for GPS antenna)

4.6 RF a with sub-6G Design Guide

4.6.1 Purpose

N/A

4.6.2 Co-existence Design Main Point

N/A



5 Mechanical Specifications

5.1 Overview

This chapter describes the process design and mechanical specifications:

- Storage Requirement
- Moisture Sensitivity
- Dimensions and Interfaces
- Packaging
- Label
- Customer PCB Design
- Thermal Design Solution
- Assembly Processes
- Specification of Rework

5.2 Storage Requirement

EXC-N1 series modules are shipped in vacuum sealed bags. The storage of modules is subject to the following conditions:

1. When the ambient temperature is below 40°C and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months.
2. After the vacuum sealing bag is opened, the module can directly carry out reflow welding or other high-temperature processes if the following conditions are met:
 - The air humidity for module storage is lower than 10%;
 - The ambient temperature of the module is lower than 30°C, the air humidity is lower than 60%, and the factory completes the placement within 72 hours.
3. If the module is in the following conditions, it needs to be baked before placement:
 - When the ambient temperature is 23°C (± 5 °C fluctuations are allowed), the humidity displayed by the humidity indicator card is greater than 10%;
 - After the vacuum-sealed bag is opened, the ambient temperature of the module is lower than 30°C and the air humidity is lower than 60%, but the factory fails to complete the placement within 168 hours;
 - After the vacuum-sealed bag is opened, the air humidity for module storage is greater than 10%.
4. If the module needs to be baked, bake it for 8 hours at 125°C (± 5 °C fluctuations are allowed).



NOTE:

The package of the module cannot withstand such high temperature, please remove the package of the module before the module is baked.



5.3 Moisture Sensitivity

Refer to 5-2.

5.4 Dimensions and Interfaces

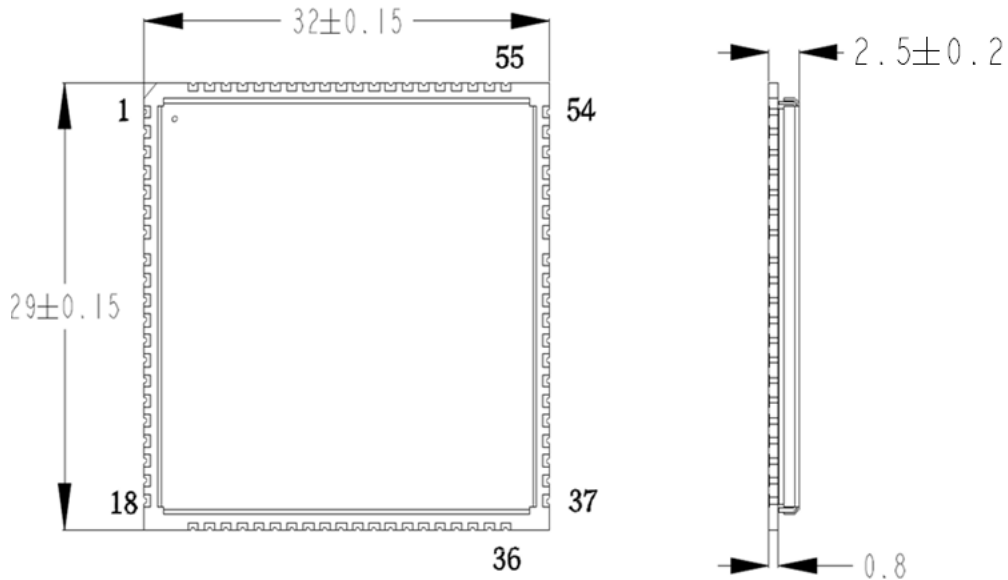
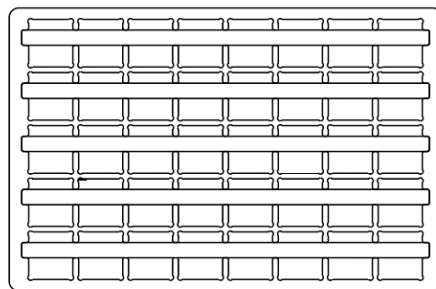


Figure 5-1 shows the LCC dimensions in details.

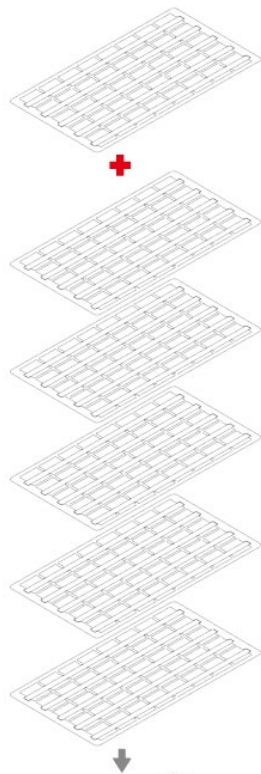
5.5 Packaging (To be update)

Compal RXL-N2 module uses ESD tray and vacuum bag into boxes. The example process shows in below picture: (Pictures of materials are only for reference.)

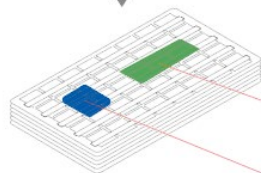


40pcs/tray

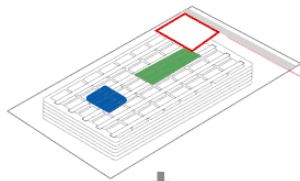
Tray outer dimension: (L) 312 * (W)* 204 (H) 9.5 mm



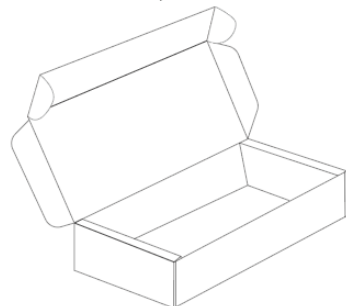
- *An empty tray as a cover.
- *5 trays for loading product.
- *All tray should totally match together while stacking.



*Put the humidity card & desiccant on the tray.

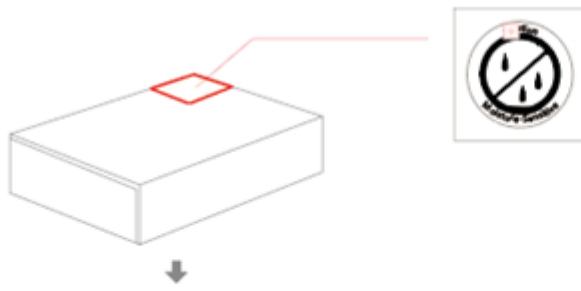


- *Put trays into a vacuum bag.
- * Paste the moisture sensitive caution label on the vacuum bag.

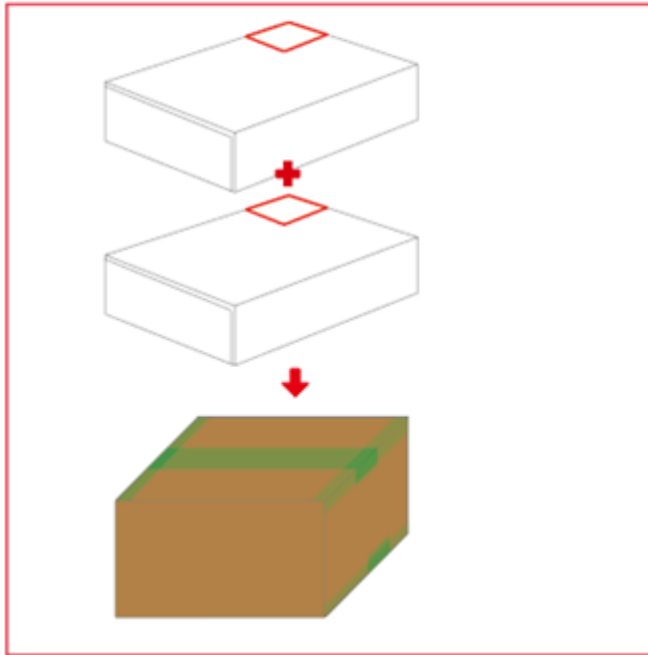


*Put above materials in box.

Pizza box Outer dimension: (L) 335 * (W)* 212 (H) 86 mm



*Paste the moisture sensitive caution label on the vacuum bag.



*Put 2 boxes in one carton.

Carton Outer dimension: (L) 362 * (W)* 233 (H) 469mm



NOTE:

For not fully loaded carton, please use empty pizza box to full fill the space (Empty pizza box need to be placed on top), and mark these empty boxes with "EMPTY" print or label.



5.6 Laser Marking

The Laser Making format is shown as Figure 5-2. It is included P/N and S/N and IMEI information. This Making format is only for reference. Please follow shipment information for final Making format.

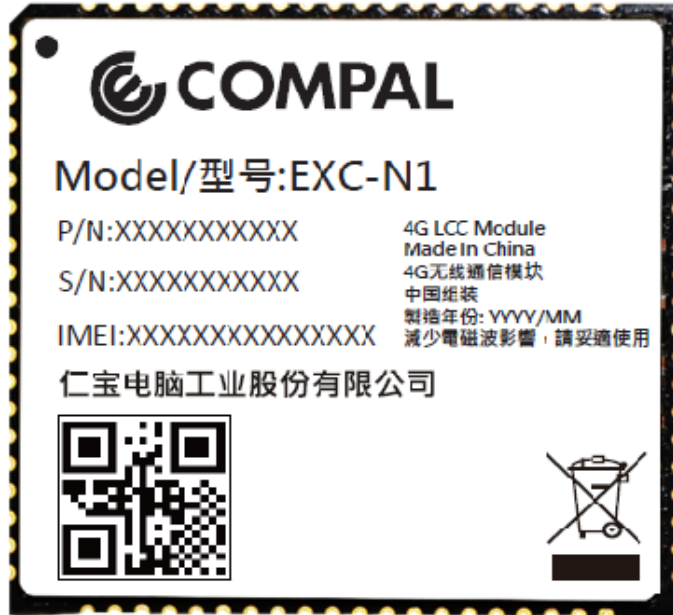


Figure 5-2 LCC Module Laser Marking

5.7 Customer PCB Design

5.7.1 PCB Surface Finish

The PCB surface finish recommended is Electroless Nickel, immersion Gold (ENIG). Organic Solder ability Preservative (OSP) may also be used, ENIG preferred.



5.7.2 PCB Pad Design

To achieve assembly yields and solder joints of high reliability, it is recommended that the PCB pad size be designed as follows:

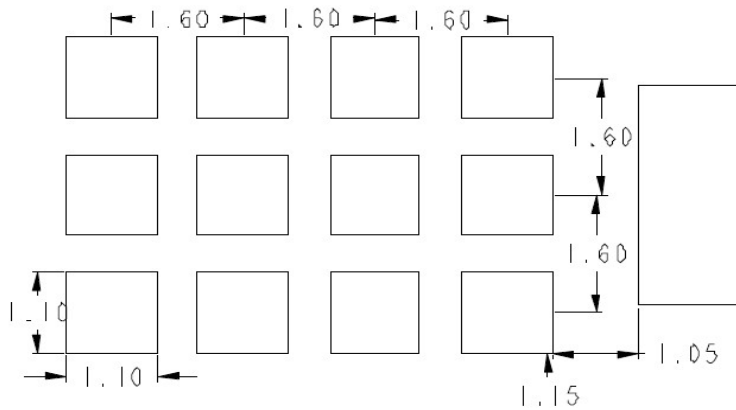
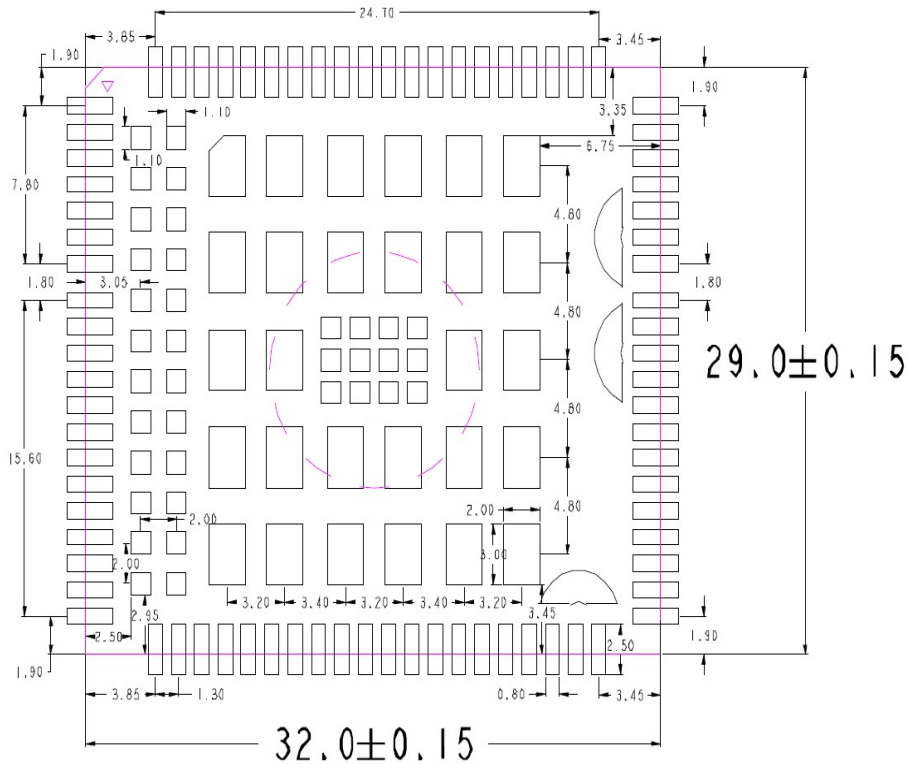


Figure 5-3 PAD Footprint design of customer's PCB (Unit: mm) (Intuitive view from BOT side)

5.7.3 Solder Mask

SMD is recommended. In addition, the solder mask of the SMD (Solder Mask Defined) pad design is larger than the pad so the reliability of the solder joint can be improved.

The solder mask must be 50~100 μm larger than the pad, that is, the single side of the solder mask must be 25~50 μm larger than the pad. The specific size depends on the processing capability of the PCB manufacturer.



Regarding the footprint mask size must be $80\ \mu\text{m}\sim 110\ \mu\text{m}$ larger than the pad, that is, the single side must be $40\ \mu\text{m}\sim 55\ \mu\text{m}$ larger than the pad. Please refer to Figure 5-3 & 5-5 for Module PAD detailed size information.

5.7.4 Requirements on PCB Layout

- Other devices must be located more than 3 mm (5 mm recommended) away from the two parallel sides of the LCC module (rework requirement), and other sides with 0.6 mm. The minimum distance between the LCC module and the PCB edge is 0.3 mm.
- When the PCB layout is double sided, the module must be placed on the second side for assembly; so as to avoid module dropped from PCB or component (located in module) re-melting defects caused by uneven weight.

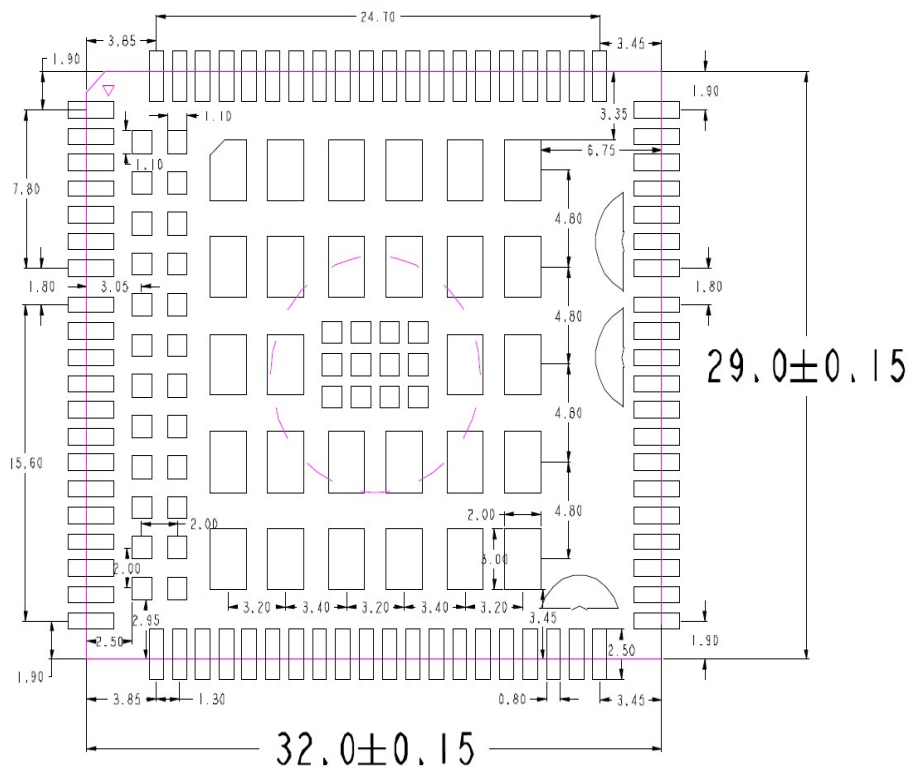


Figure 5-4 PCB Layout (Unit: mm)

5.8 Thermal Design Solution

When the module works in the maximum power condition, the module has high power consumption (for details, see Power Consumption). To improve the module reliability and stability, focus on the thermal design of the device to speed up heat dissipation.



For thermal characteristics of the LCC module, you can refer to Operating and Storage Temperatures.

The LCC module has built in thermal interface material, thermal grease, which thermal conductivity is around 2W/mK.

Below are some thermal recommendation,

The PCB design for thermal heat spreading

- Follow the IC thermal pad placement to put thermal via
- All copper ground layers of the PCB must be connected to each other through via-holes
- Increase the coverage of the PCB ground planes as possible
- The ground planes should be as continuous as possible

Example for thermal heat spreader on LCC module,

- add heat sink on module shielding cover,
- add heat-pipe and copper plate on module shielding cover,
- for extreme condition, use fan(s) and heat sink on module,
- place thermal pad/grease between module cover and heat spreader.

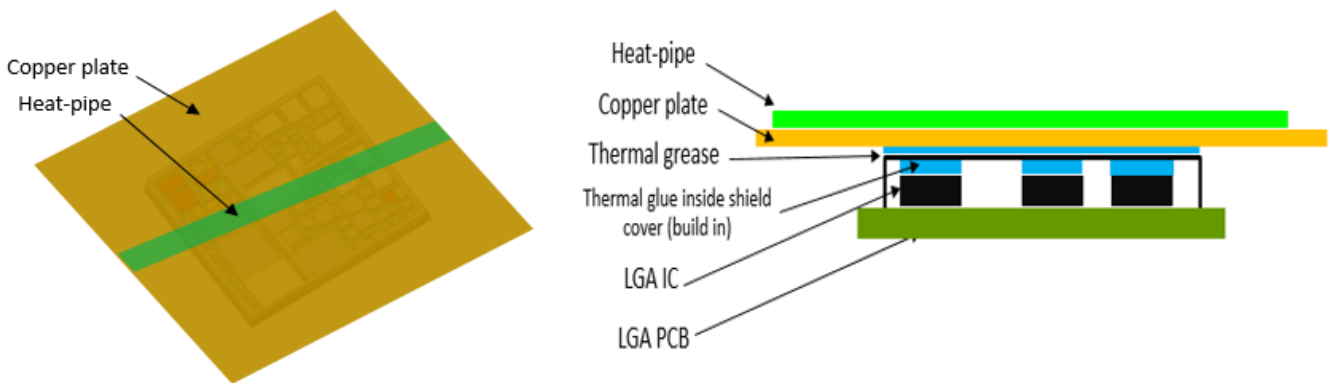


Figure 5-5 Diagrammatic Sketch of Thermal Solutions

5.9 Assembly Processes

5.9.1 General Description of Assembly Processes

- Tray modules are required at SMT lines, because LCC modules are placed on ESD pallets.
- Reflow ovens with at least seven temperature zones are recommended.



- Use reflow ovens or rework stations for soldering, because LCC modules have large solder pads and cannot be soldered manually.

5.9.2 Stencil Design

Module flatness standard: $\leq 0.13\text{mm}$ (Steel mesh: it is suggested that customers open the steel mesh reasonably by combining the main board, and it is suggested that customers open the stepped steel mesh to 0.18mm by combining the experience of COMPAL module SMT)

5.9.3 Reflow Profile

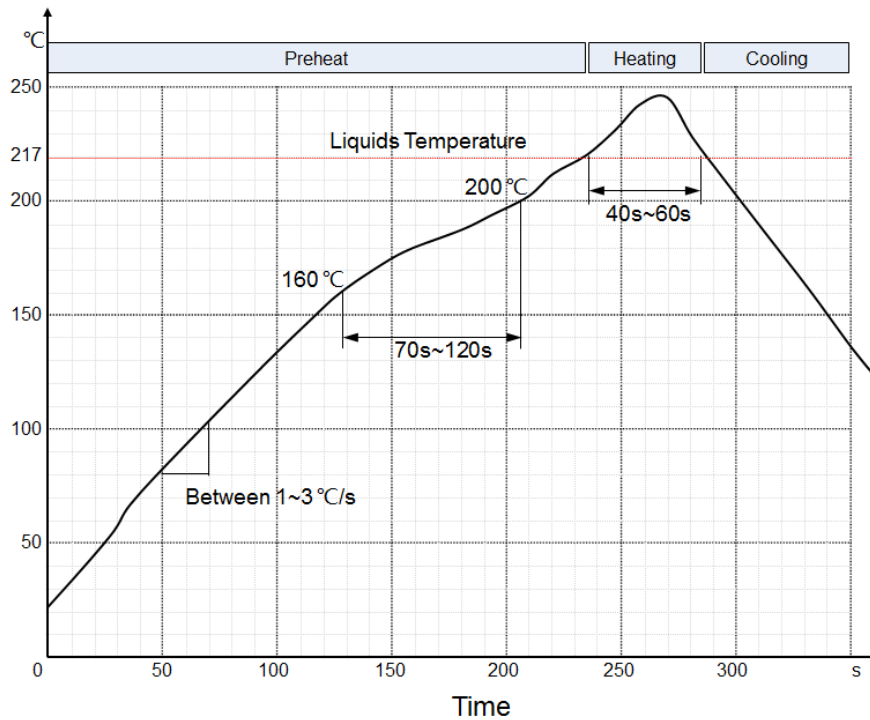


Figure 5-6 Temperature Curve of Solder Reflow

Table 5-1 IPC/JEDEC Reflow Profiles table

Profile Feature	Pb-Free Assembly
Preheating temperature rise requirements ($< 160^{\circ}\text{C}$)	$\leq 2^{\circ}\text{C} / \text{s}$
Average temperature zone requirements ($165^{\circ}\text{C} \sim 217^{\circ}\text{C}$)	60~100 (recommend 70~85s)
Peak temperature rise rate	1~3 $^{\circ}\text{C} / \text{s}$
Minimum reflow peak temperature	230 $^{\circ}\text{C}$
Maximum reflow peak temperature	250 $^{\circ}\text{C}$
Time of over the liquid line (217°C)	35~90s
Time of over 230 $^{\circ}\text{C}$	25~50s



Cooling slope in cooling stage (T=217~120°C)	-2~-5°C/s
Maximum slope of cooling phase	-6°C/s
Time from 50°C to 217°C	150~240s
Number of reflow oven temperature zones	≥10



NOTE:

All temperatures refer to topside of the package measured in the package body surface"

It is recommended to use reflow soldering equipment with 8-temperature zones and above; the maximum number of reflow soldering times allowed for the module is ≤3 times (including the first reflow during the finished module process).

The lead-free process reflow soldering furnace temperature requirements, the actual peak temperature of the furnace temperature of the LCC module device surface should be greater than 240 °C and less than 242 °C, too high furnace temperature will bring the risk of module shield warping; with reflow tooling The peak temperature of the fixture is recommended to be between 243°C and 246°C to prevent cold welding of LCC modules; the furnace temperature span of adjacent temperature zones should be less than 35°C;

For the reflow soldering of the bottom of the module, it is necessary to consider the defective part drop caused by the gravity of the shield cover when the module is soldered upside down. Please refer to the following specifications: allowable weight (g) = pin surface area (mm²) × number of pins × 0.665; for modules that exceed the allowable weight, you can lower the temperature of the back of the module by 5°C to 8°C or use a clamp to support it.

Precautions for secondary reflow

When the client product is reflowed for the second time, it is necessary to pay attention to opening the stencil according to the production requirements of COMPAL stencil. To evaluate the opening of the furnace fixture, so that the flatness of the module can reach the expected standard after the second reflow.

When making the jig for passing through the furnace, it is necessary to pay attention to the uniformity of the temperature of the whole PCB when passing through the furnace. Since there are two layers of PCB in the module position, the heating rate will be slower than the surrounding position of the motherboard. It needs to be improved with a jig, and the module is located at the bottom of the motherboard position and hollowed out. , the outer four corners are used as columnar supports, and other parts of the main board are used as corresponding positions to avoid the position, which has achieved the overall temperature uniformity effect during reflow, and avoids module warping and local deformation.



5.10 Specification of Rework

5.10.1 Process of Rework

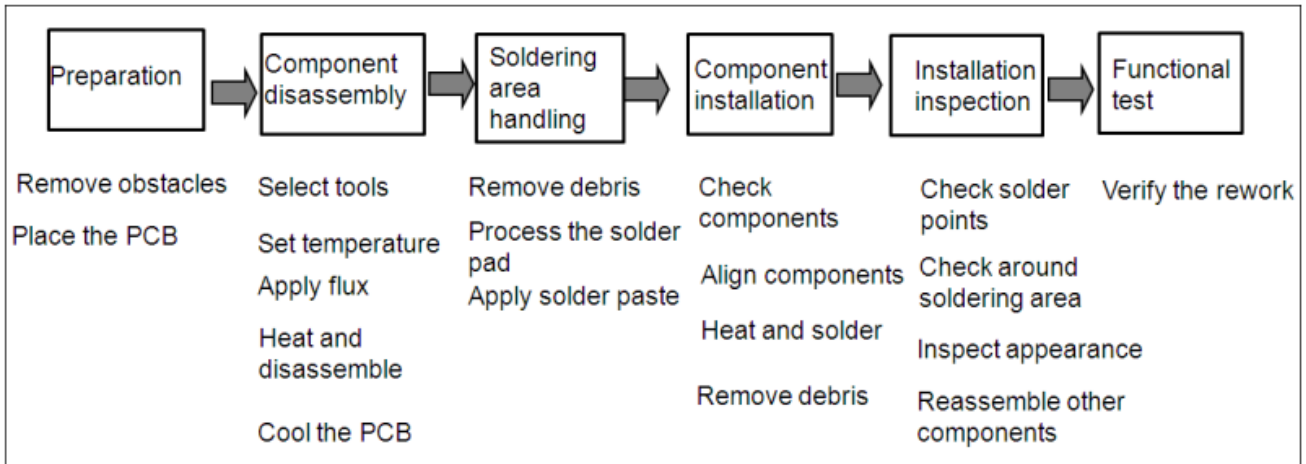


Figure 5-10 Process of Rework

5.10.2 Preparations of Rework

- Remove barrier or devices that can't stand high temperature before rework.
- If the device to be reworked is beyond the storage period, bake the device according to Table 5-1 .

5.10.3 Removing of the Module

The solder is molten and reflowed through heating during the module removing process. The heating rate must be quick but controllable in order to melt all the solder joints simultaneously. Pay attention to protect the module, PCB, neighboring devices, and their solder joints against heating or mechanical damages.



NOTE:

- The LCC module has many solder pads and the pads are large. Therefore, common soldering irons and heat guns cannot be used in the rework. Rework must be done using either infrared heating rework stations or hot air rework stations. Infrared heating rework stations are preferred, because they can heat components without touching them. In addition, infrared heating rework stations produce less solder debris and less impact on modules, while hot air rework stations may cause shift of other components not to be reworked.
- You must not reuse the module after disassembly from PCB during rework.
- It is proposed that a special clamp is used to remove the module.

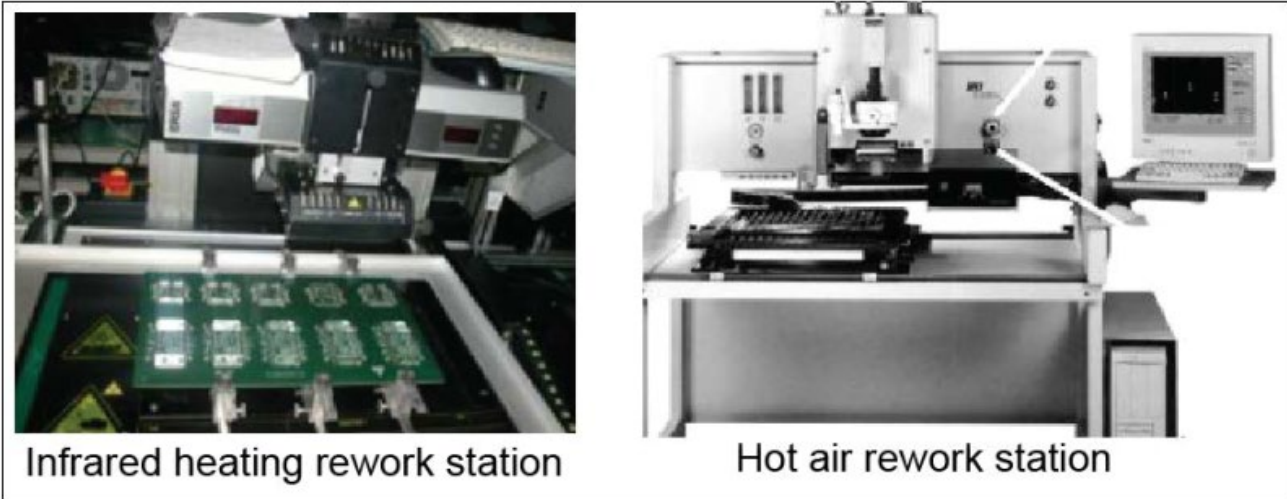


Figure 5-7 Equipment used for rework

5.10.4 Welding Area Treatment

Step 1 Remove the old solder by using a soldering iron and solder braid that can wet the solder.

Step 2 Clean the pad and remove the flux residuals.

Step 3 Solder pre-filling: Before the module is installed on a board, apply some solder paste to the pad of the module by using the rework fixture and stencil or apply some solder paste to the pad on the PCB by using a rework stencil.



NOTE:

It is recommended that a fixture and a mini-stencil be made to apply the solder paste in the rework.

5.10.5 Module Installation

Install the module precisely on the module and ensure the right installation direction of the module and the reliability of the electrical connection with the PCB. It is recommended that the module be preheated in order to ensure that the temperature of all parts to be soldered is uniform during the reflow process. The solder quickly reflows upon heating so the parts are soldered reliably. The solder joints undergo proper reflow duration at a preset temperature to form a favorable Intermetallic Compound (IMC).



NOTE

It is recommended that a special clamp be used to pick the module when the module is installed on the pad after applied with some solder.

A special rework device must be used for the rework.



5.10.6 Specifications of Rework

Temperature parameter of rework: for either the removing or welding of the module, the heating rate during the rework must be equal to or smaller than 3°C/s, and the peak temperature between 240°C–250°C. The following parameters are recommended during the rework.

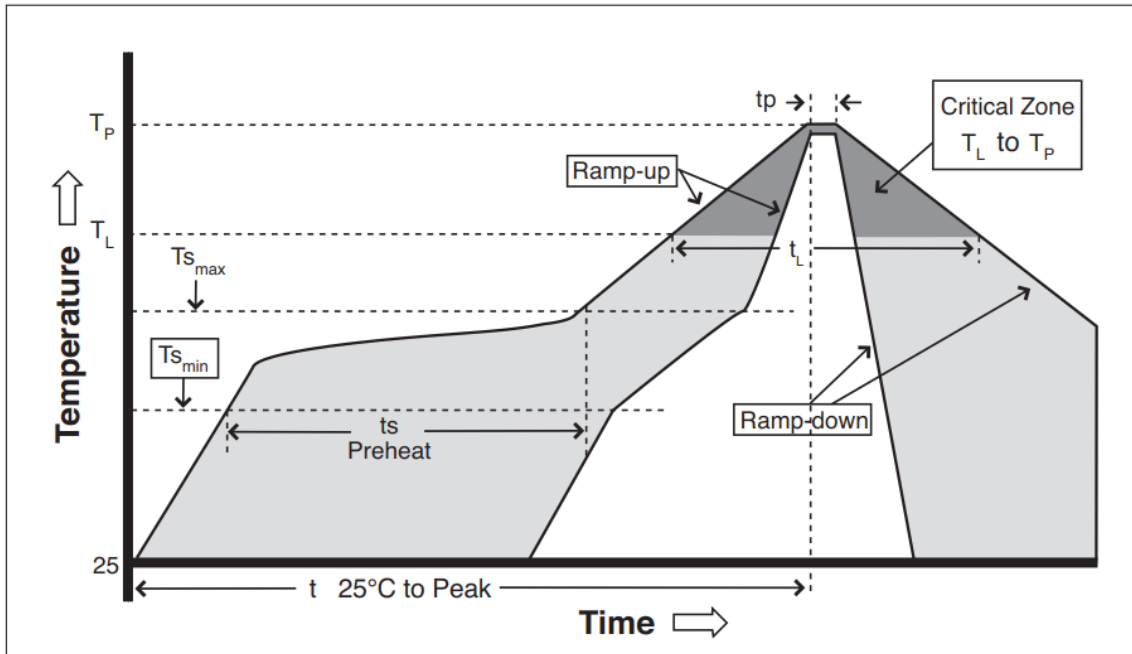


Figure 5-8 Temperature parameter of rework

Table 5-2 IPC/JEDEC Reflow Profiles table

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (TSMAX to TP)	3 °C / second max.
Preheat – Temperature Min (TsMIN) – Temperature Max (TsMAX) – Time (tsMIN to tsMAX)	150 °C 200 °C 60-180 seconds
Time maintained above – Temperature (TL) – Time (tL)	217 °C 60-150 seconds
Peak/Classification Temperature (TP)	260 °C +0/-5 °C
Time within 5 °C of actual Peak Temperature (tp)	20 – 40 seconds
Ramp-Down Rate	6 °C / second max.
Time 25 °C to Peak Temperature	8 minutes max.



NOTE:

All temperatures refer to topside of the package measured in the package body surface"

LCC Rework Guidelines

The 29 x 32 mm LCC module package is capable of being re-worked in a non-destructive manner using standard hot-air reworking stations. Care must be taken that the temperature the package is exposed to does not exceed the maximum reflow temperature of 260°C. Pre-heating of the board can be done to minimize the time the peak re-work temperature is applied. Also, solder flux should be applied to the area to insure proper solder reflow.

When the temperature of the local area of the module board exceeds the glass transition temperature of the PCB board (usually 140-150°C), it is regarded as a maintenance heating, and the maximum number of maintenance heating times for each PCB board is 6 times. Repair welding or spot welding with an electric soldering iron is not considered a repair, and welding repair with a hot air gun will be regarded as a repair. Under normal circumstances, the PCBA board will be heated 2 times for each welding repair (1 time for removal and 1 time for welding), so the maximum number of rework and repair of the PCBA board is 3 times;

5.11 Ordering information

All relevant LCC HW spec 、figures and design guidelines in this document are common specification for All 4G LCC mode

5.11.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table5-4.

Table 5-3 Device ordering information

Character	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th
Module		Module Solution	Module Type	SKU Region	Version				Sample Type	SW Application	SW Version	CPU Version
Code	E	X (MDM9207)	C (LCC Module)	E = EU N = US	(1-9)				* 0=Basic	E =EP MODE R= RC Mode C= CPE PCIe mode		



NOTE:

Example 1: EXC-N1



Sample Type note:

*⁰ Basic version is define support 1Gb NAND Flash with 1Gb LPDDR4X .



6 Reliability test

Table 6-1 Environmental reliability requirements

Test item	Test condition						
Low temperature storage test	Temperature -45°C, 24 hours in shutdown status						
High temperature storage test	Temperature +90°C, 24 hours in shutdown status						
Thermal shock test	In shutdown status, 1h at the temperature -45°C and +90°C respectively. Temperature changeover time <3min, 24 cycles in total						
High temperature and high humidity test	Temperature +85°C, humidity 95%RH, 48 hours in shutdown status						
Low temperature operation test	Temperature -40°C, 24 hours in working status						
High temperature operation test	Temperature +85°C, 24 hours in working status						
Vibration test	Perform vibration test according to the requirements shown in the following table: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Frequency</th> <th>Random vibration ASD (Acceleration Spectral Density)</th> </tr> </thead> <tbody> <tr> <td>5~20Hz</td> <td>0.96m²/s³</td> </tr> <tr> <td>20~500Hz</td> <td>0.96 m2/s3 (at 20Hz), other -3dB / octave</td> </tr> </tbody> </table>	Frequency	Random vibration ASD (Acceleration Spectral Density)	5~20Hz	0.96m ² /s ³	20~500Hz	0.96 m2/s3 (at 20Hz), other -3dB / octave
Frequency	Random vibration ASD (Acceleration Spectral Density)						
5~20Hz	0.96m ² /s ³						
20~500Hz	0.96 m2/s3 (at 20Hz), other -3dB / octave						
Life test of connectors	Board-to-board connector interface can be inserted and removed for 50 times; RF antenna interface cable can be inserted and removed for 30 times.						
ESD test	<ol style="list-style-type: none"> 1. Test the power supply PAD and large-area ground in the call status of the module, and the ESD shall meet the following requirements: <ol style="list-style-type: none"> 1) The contact discharge should pass the test levels of ±4KV and ±5KV 2) Air discharge should pass the test levels of ±8KV and ±10KV 2. When the module is in shutdown status, test the SIM card connector of EVB, and the ESD shall meet the following requirements: <ol style="list-style-type: none"> 1) The contact discharge should pass the test level of ±4KV 2) Air discharge should pass the test level of ±8KV 3. For other interfaces of the module, ESD shall meet the following requirements: <ol style="list-style-type: none"> 1) The contact discharge should pass the test level of ±0.5KV 2) Air discharge should pass the test level of ±1KV 						

6.1 ESD Features

ZXG1 series is a consumer terminal product. Although module design has been considered the ESD problem, and do the ESD protection, but consider ZXG1 series modules in the transport and secondary development may also have ESD problem occurred, so developers to view of



the protection of the final product ESD problem, including the anti-electrostatic packaging processing. Please refer to the document interface design when the customer application recommended circuit.

Refer to the following table for the ESD allowed discharge range for ZXG1 series module.

Table 6-2 ESD Performance Parameters (Temperature: 25°C, Humidity: 45%)

Test point	Contact discharge	Air discharge	Unit
VBAT, GND	±5	±10	KV
Antenna interface	±4	±8	KV
Other interfaces	±0.5	±1	KV



NOTE:

The testing condition is module with external TVS in EVB, not only module.



FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time- averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: GKREXCN1.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- GSM850 : ≤ 9.438 dBi
- GSM1900 : ≤ 10.010 dBi
- WCDMAII: ≤ 8.500 dBi
- WCDMAIV: ≤ 5.500 dBi
- WCDMAV: ≤ 9.908 dBi
- LTE Band2/7/25/41: ≤ 8.500 dBi
- LTE Band4/66: ≤ 5.500 dBi
- LTE Band5: ≤ 9.908 dBi
- LTE Band7: ≤ 8.000 dBi
- LTE Band12: ≤ 9.197 dBi
- LTE Band13: ≤ 9.656 dBi
- LTE Band17: ≤ 9.224 dBi
- LTE Band26: ≤ 9.861 dBi



5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above).

The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: GKREXCN1" or "Contains FCC ID: GKREXCN1" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.



The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.