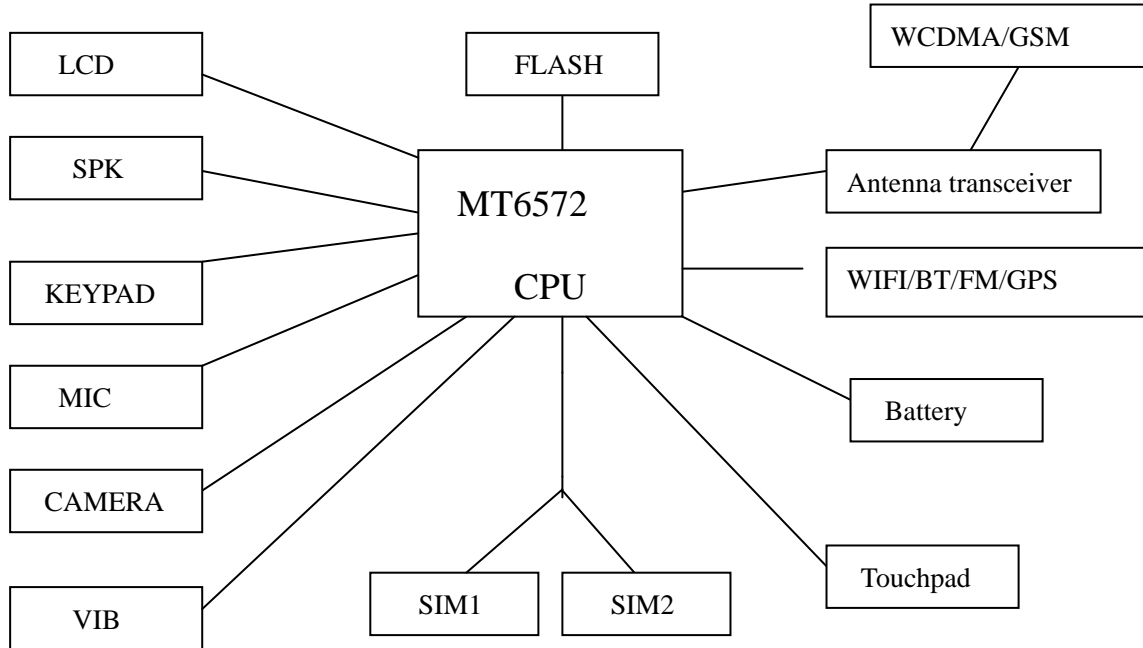


## General Technical Description

### 1. Scope

This document shows and provides the more detail information about the platform we used. The basic description for the Baseband and RF section are also included.

### 2. System Block Diagram



**Figure 1** System Overview

### 3. RF Module

#### 3.1 Transceiver (MT6166)

The MT6166 is a RF transceiver targeted at high speed 2G/3G-FDD/TDD multi-mode smart phone and tablet computers implanted in 40nm CMOS. The RF transceiver function is fully integrated. This document briefly introduces the RF macros in MT6166.

#### 4. Baseband (MT6572)

MT6572 integrates a mixed-signal baseband front-end in order to provide a radio interface with flexibility for efficient customization. It build in gain/offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT6572 achieves great MODEM performance by utilizing a high resolution A/D converter in the RF downlink path.

## 1.1 Platform Features

- **General**
  - Smartphone, 3 MCU subsystems architecture
  - SLC NAND flash and eMMC bootloader
  - Supports LPDDR-1/LPDDR-2/LPDDR-3/PD-DDR3
- **AP MCU subsystem**
  - Dual-core ARM® Cortex-A7 MPCore™ operating at 1.2GHz
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 256KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 1.05V to 1.26V
- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with maximum 480MHz operation frequency
  - 32KB I-cache, 16KB D-cache
  - 256KB TCM (tightly-coupled memory)
  - DSP for running modem/voice tasks, with maximum 245.76MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control
- **MD external interfaces**
  - Supports dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, ...)
  - UART for modem logging/debugging purpose
- **External memory interface**
  - Supports LPDDR1/2/3, PC-DDR3 up to 2GB
  - 32-bit data bus width
  - Memory clock up to 333MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
- **Peripherals**
  - USB2.0 high-speed OTG supporting 8 Tx and 8 Rx endpoints
  - USB2.0 full-speed host
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - 2 UART for debugging and applications
  - SPI for external device
  - 2 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Maximum 5 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional

- external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols
  - GPU voltage: 1.15V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V/1.8V/1.35V/1.5V
  - NAND: 1.8V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz
- **Operating conditions**
    - Core voltage: 1.15V
    - Processor DVFS voltage: 1.15V ~ 1.26V (Typ. 1.15V; sleep mode 1.05V)
    - Processor SRAM voltage: 1.15V ~ 1.26V (Typ. 1.15V; sleep mode 1.05V)
  - **Package**
    - Type: TFBGA
    - 10.6mm x 10.6mm
    - Height: 1.1mm maximum
    - Ball count: 428 balls
    - Ball pitch: 0.4mm

## 5. BT+WIFI+GPS (MT6627)

MT6627 is a four-in-one chip, providing the WIFI/BT/GPS features.