

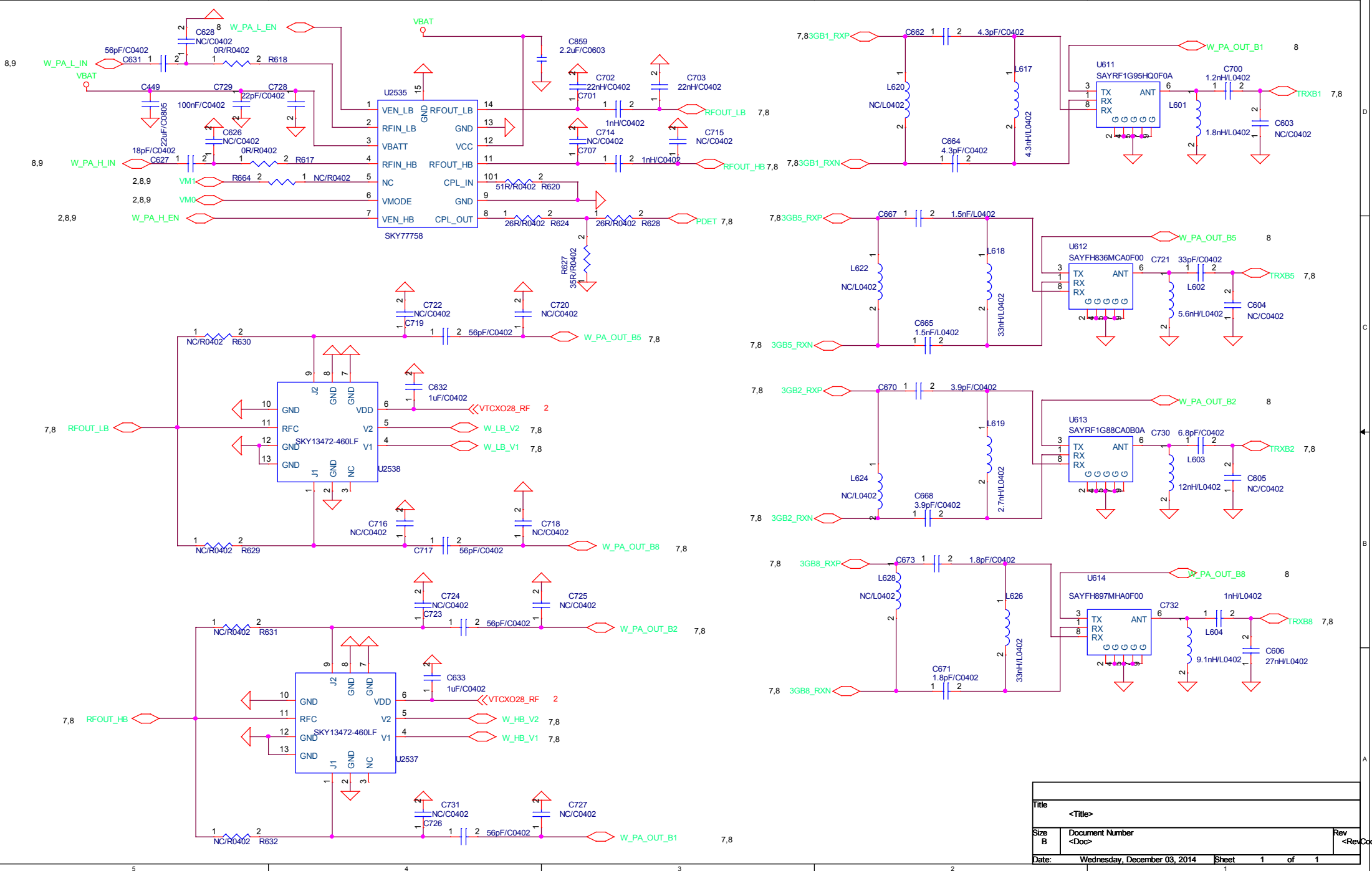
check MSDCl/2 IO power

C115 close to pin E1 (150mil)  
C125 close to pin G26 (150mil)

R327 OR  
R328 OR  
R329 OR

GND\_VPROC\_FB 3 To MT6323 GND\_VPROC\_FB pin  
VPROC\_FB 3 To MT6323 VPROC\_FB pin

(1)VPROC\_BB, GND pin of 1st cap group should be laid differential pair with ground shielding remote sense to PMIC  
(2)R107 & R108 must be close to 1st cap group.  
If you want to remove them, please make sure the VPROC\_FB/GND\_VPROC\_FB must connect from 1st cap. group of VPROC

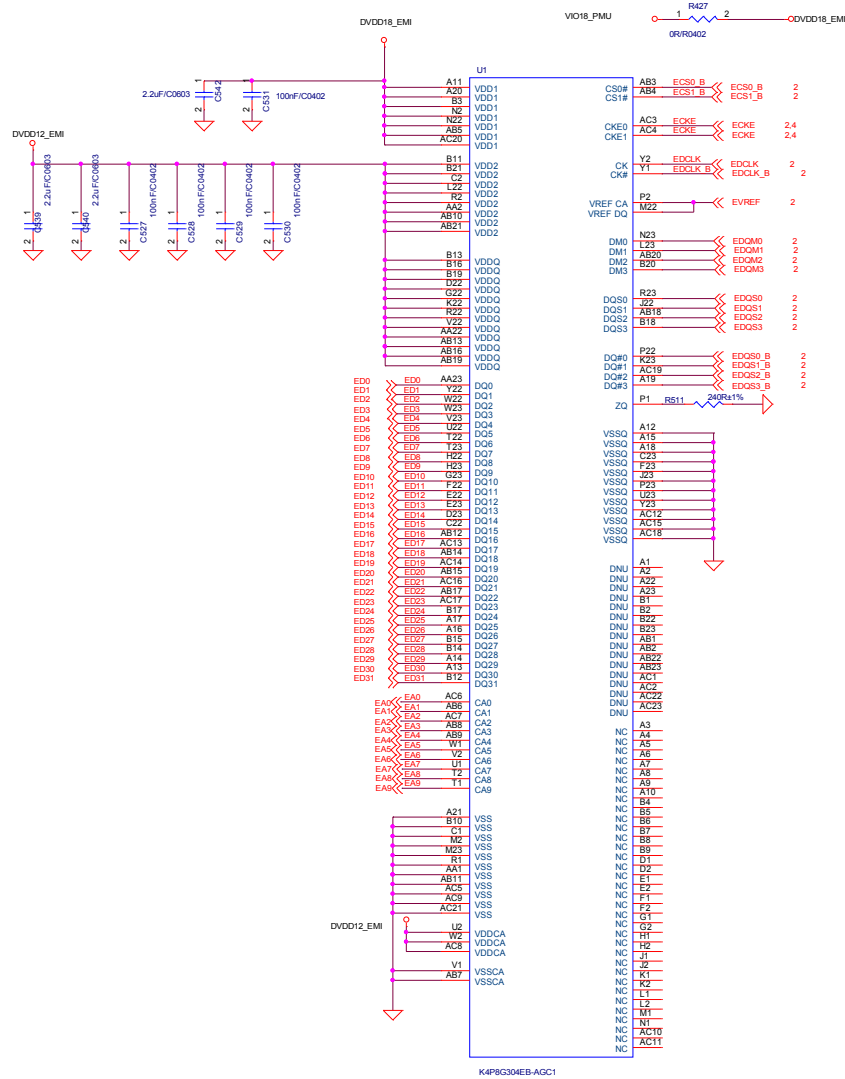


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# Discrete LPDDR2

168 Ball

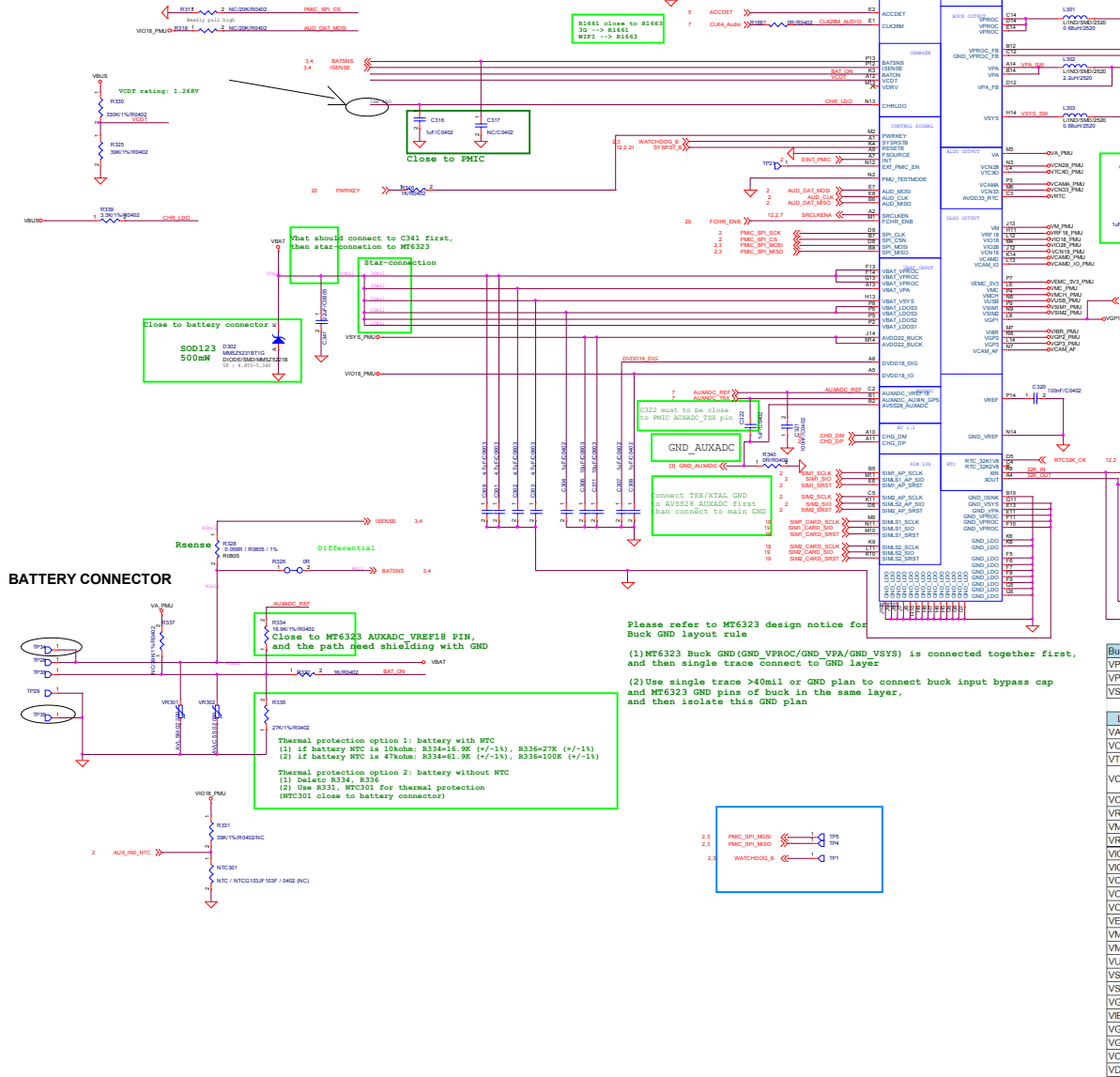
VDD1=1.8V  
VDD2=1.20V  
VDDCA=1.2V  
VDDQ= 1.20V



K4P8G30HEB-AGC1



Symbol	L10D0R2/1.2V	PCDD0R3L/1.35V	PCDD0R3/1.5V	L10D0R1/1.8V	Default
SP1_CSM	H	L (20K)	H	L (20K)	PO
AUX_MOS1	L	H (20K)	H (20K)	L	PD



Buck	Output Voltage(V)	Output Current(mA)	Input Decoupling	Output Decoupling	Notes
VPROG	0.7-1.4	2800	>10uF	L=0.68uH, C=10uF*4	Total output cap >40uF
VPA	0.5-3.4	600	>4.7uF	L=2.2uH, C=2.2uF+2.2uF	Output cap range 4.4uF +/-20%
VSYS	2.2	1200	>10uF	L=0.68uH, C=10uF*2	Total output cap >20uF

LDO	Output Voltage(V)	Output Current(mA)	Bypass cap	cap range	Notes
VA	2.8	150	1uF	-20%~+20%	Far-end bypass cap
VFN28	2.8	30	1uF	-20%~+20%	Far-end bypass cap
VTCXO	2.8	40	1uF	-20%~+20%	Far-end bypass cap
VCAMA	2.8	150	3.2uF	-20%~+20%	1uF near-end 2.2uF Far-end bypass cap
VFN33	3.3/4.3/5/3.6	240	4.7uF	-20%~+20%	Far-end bypass cap
VRTC	2.8	2	0.1uF to 1000uF	-20%~+20%	Far-end bypass cap
VM	1.24/1.39/1.54/1.84	700	10uF	-20%~+20%	Far-end bypass cap
VRF18	1.825	200	1uF	-20%~+200%	Far-end bypass cap
VI018	1.8	300	4.7uF	-20%~+200%	Far-end bypass cap
VI028	2.8	200	2.2uF	-20%~+200%	Far-end bypass cap
VFN18	1.8	120	1uF	-20%~+20%	Far-end bypass cap
VFN40	1.2/1.3/1.5/1.8	150	1uF	-20%~+20%	Far-end bypass cap
VFN40	1.8	100	1uF	-20%~+20%	Far-end bypass cap
VMC	3.0/3.3	400	4.7uF	-20%~+20%	Far-end bypass cap
VMC	1.8/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VMCH	3.0/3.3	400	2.2uF	-20%~+20%	Far-end bypass cap
VSUB	3.3	20	1uF	-20%~+20%	Far-end bypass cap
VSIM1	1.8/3.0	50	1uF	-20%~+20%	Far-end bypass cap
VSIM2	1.8/3.0	50	1uF	-20%~+20%	Far-end bypass cap
VGP1	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VBR	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VGP2	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VSP3	1.2/1.3/1.5/1.8	200	1uF	-20%~+20%	Far-end bypass cap
VFN40	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VDIG1.8	1.8	20	1uF	-20%~+20%	Far-end bypass cap

SKY77590 control logic table  
 Enable Vctc VctB VctA  
 LB GMSK\_TX H L L H  
 HB GMSK\_TX H L L H  
 TRX1 L H L L  
 TRX2 L H H L  
 TRX3 L H L H  
 TRX4 L H H H  
 TRX5 L L L L  
 TRX6 L L L H  
 TDSCDMA H H H H

BPIO\*4 and 10\*11 are 2G+3G mode  
 both  
 BPI5\*9 and 12\*14 are 3G mode only  
 (suggest BPI5\*9 = 1.8V)

D

D

C

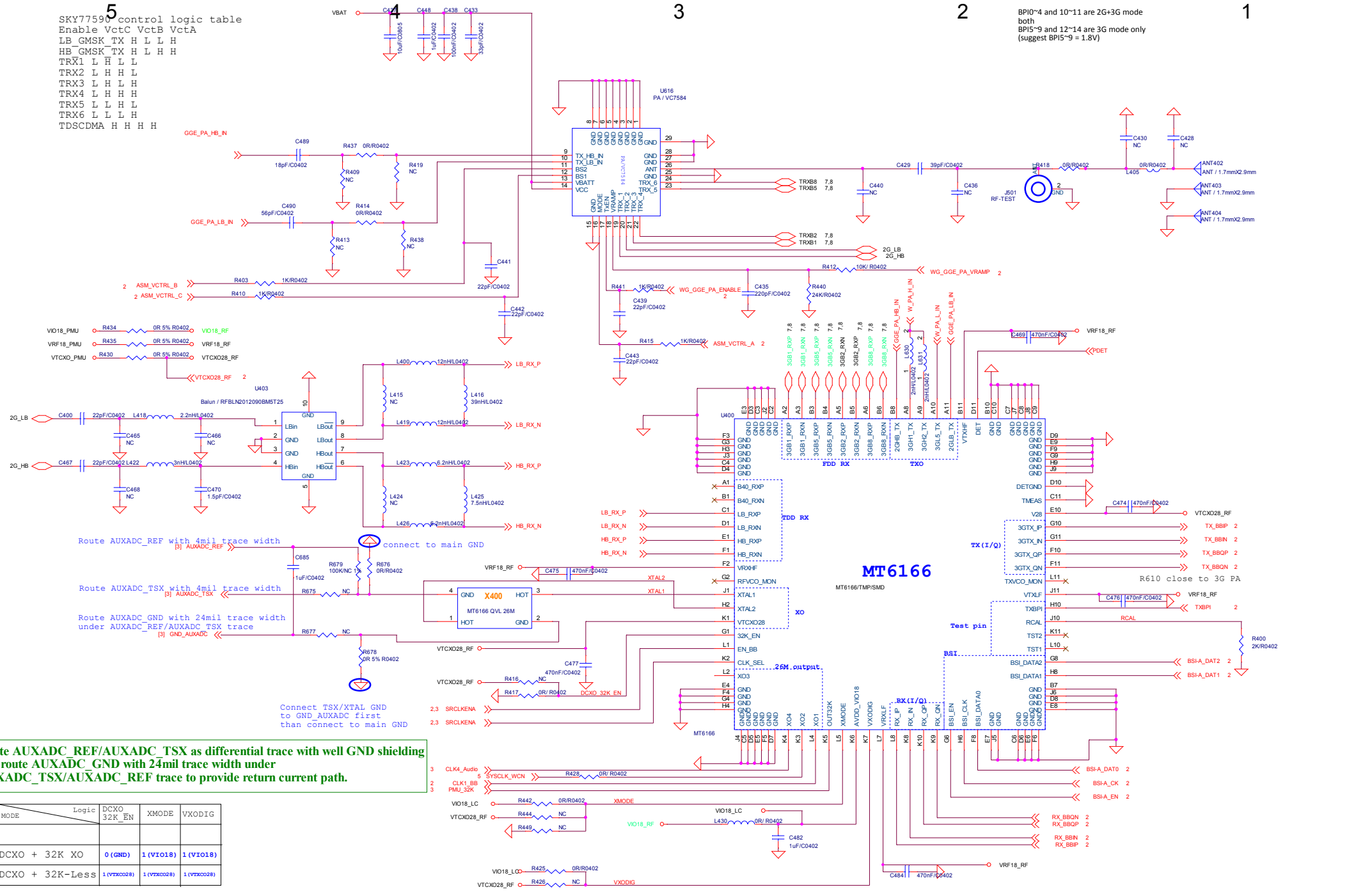
C

B

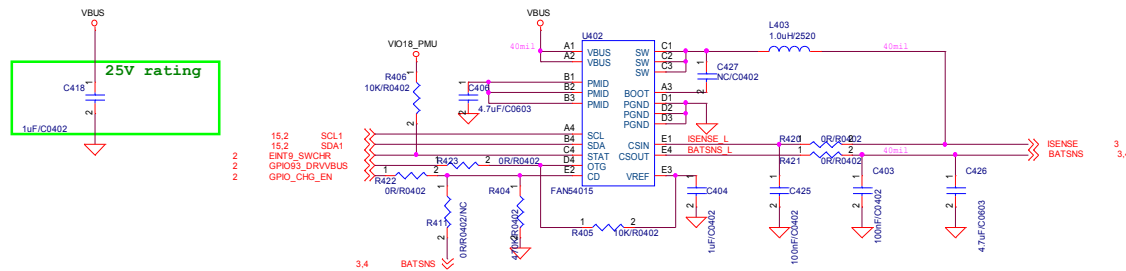
B

A

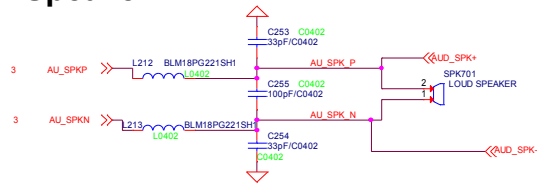
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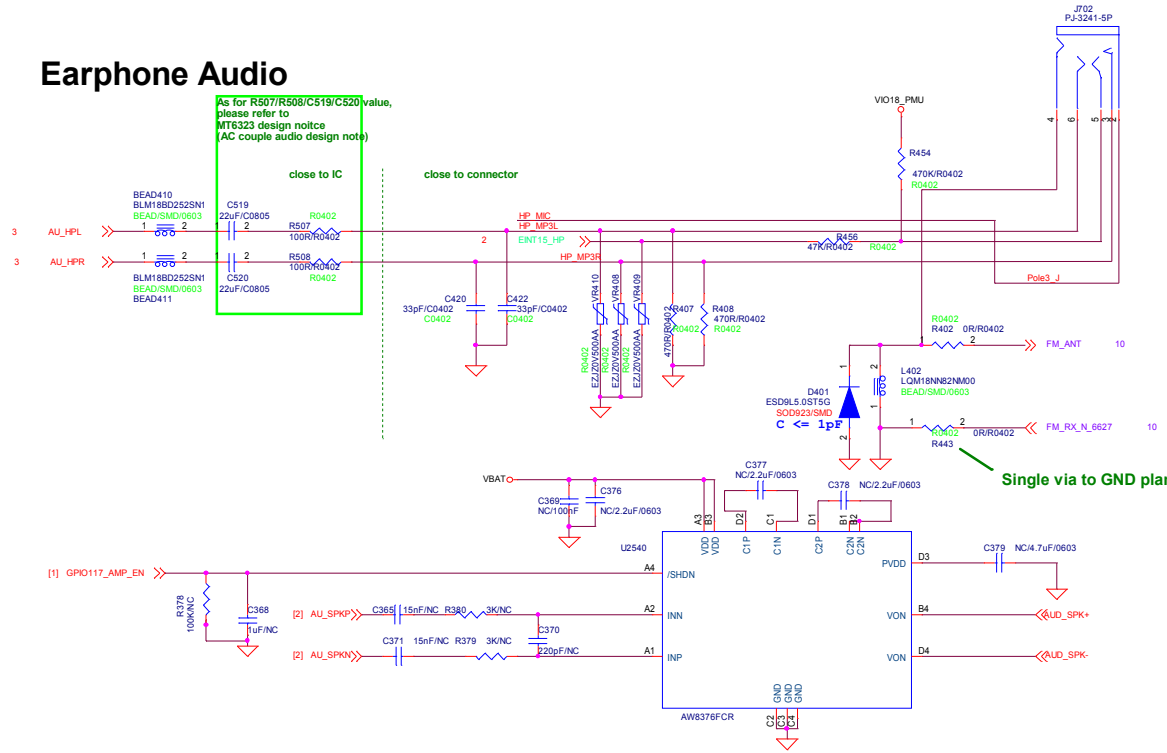
# Switching Charger



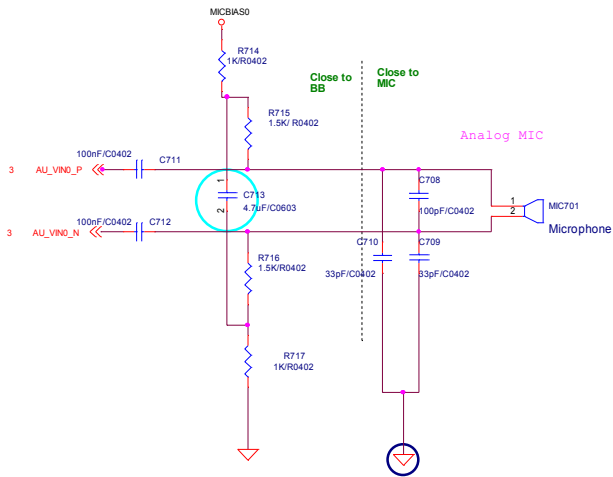
# Speaker



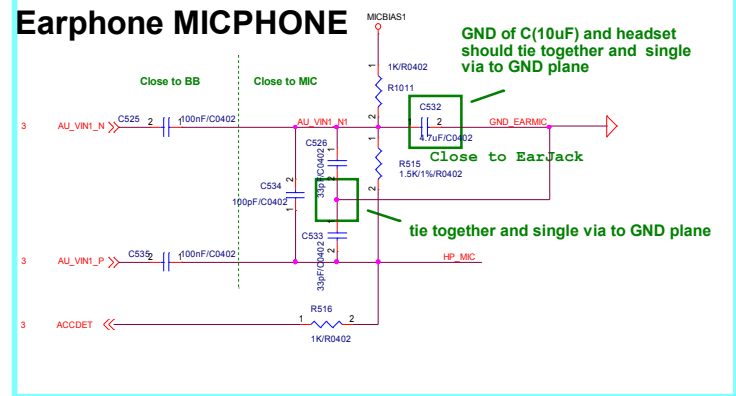
# Earphone Audio



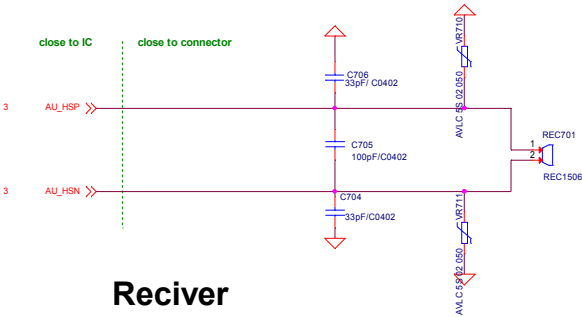
# Microphone



# Earphone MICPHONE

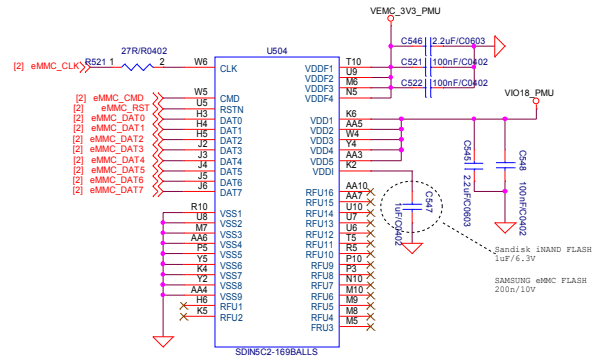


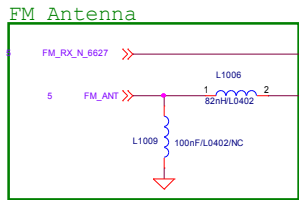
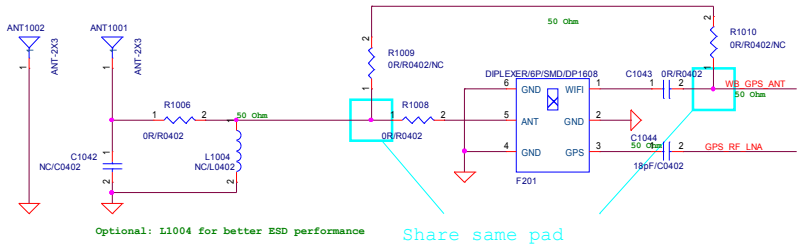
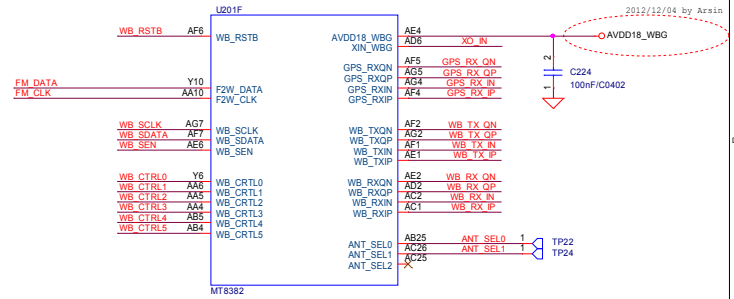
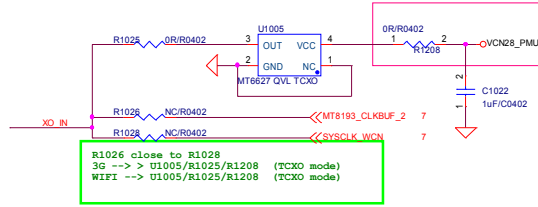
# Reciver





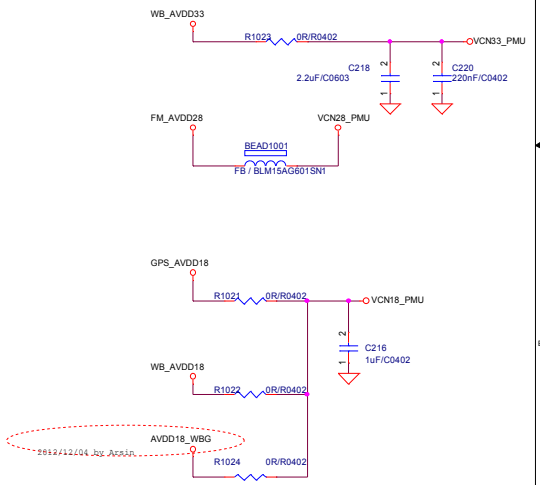
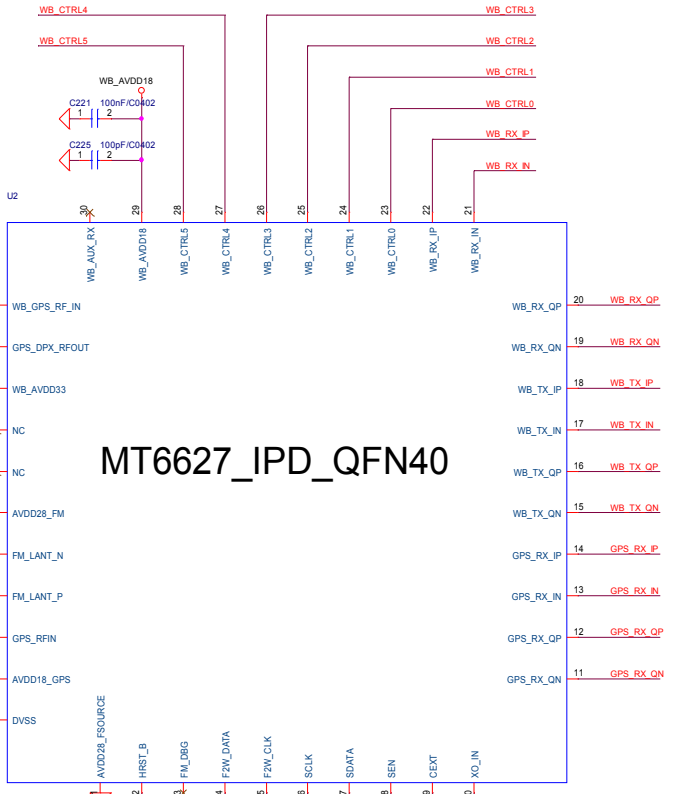
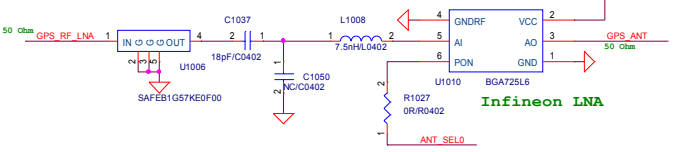
# eMMC

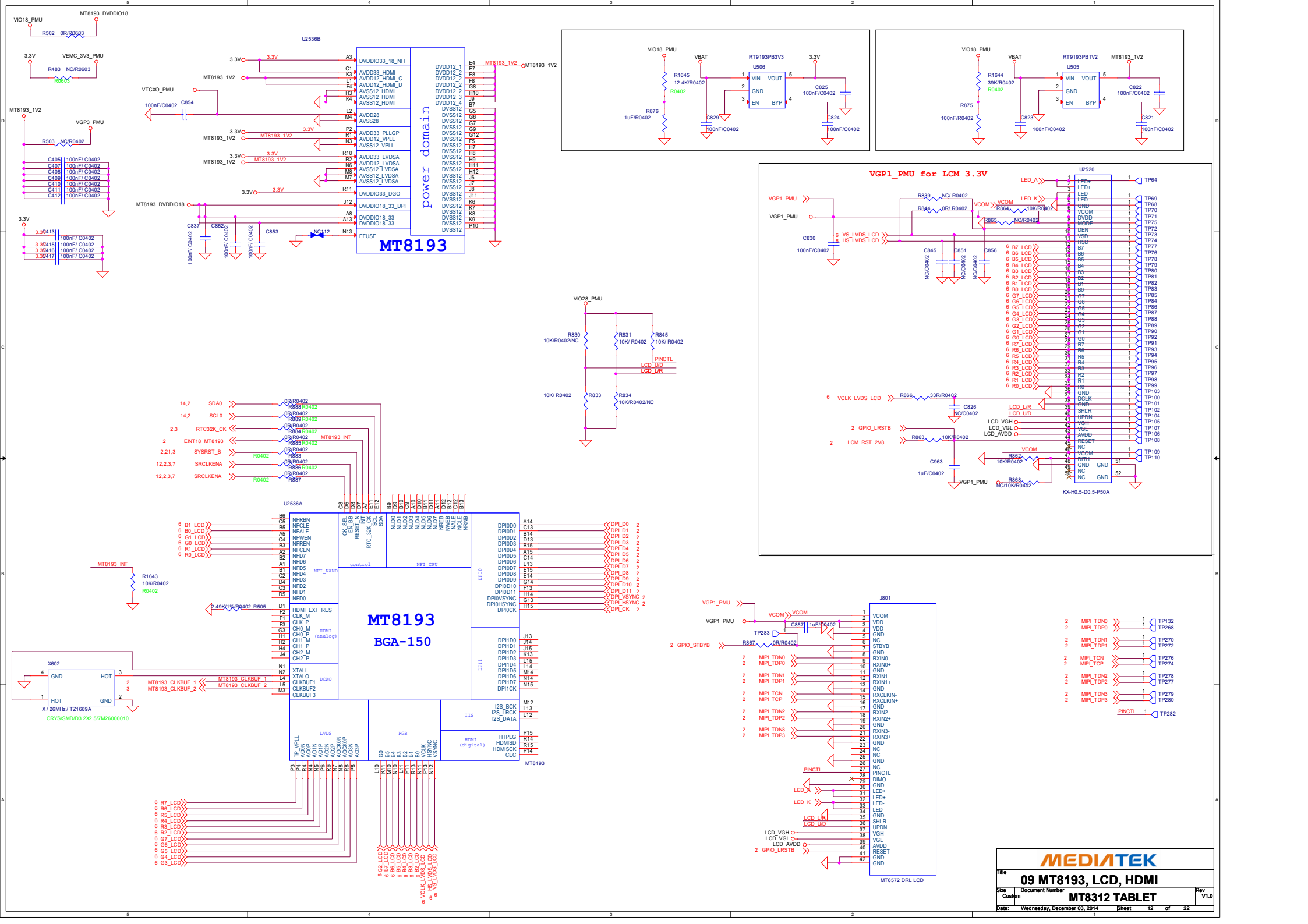


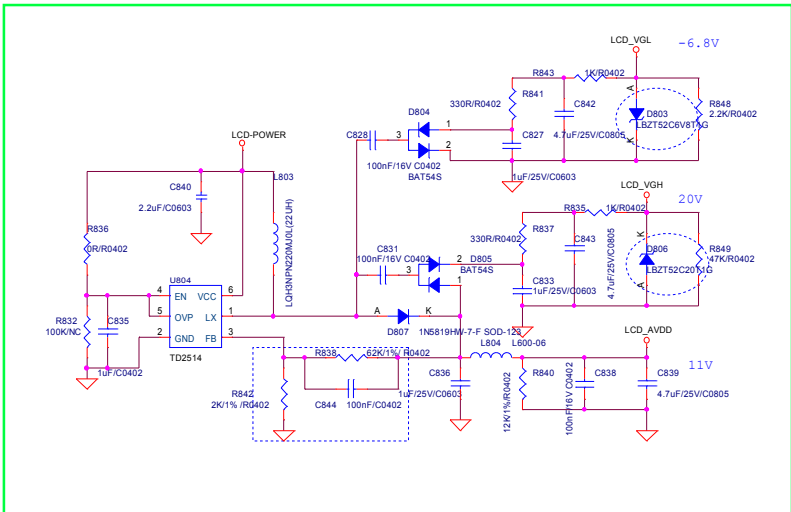
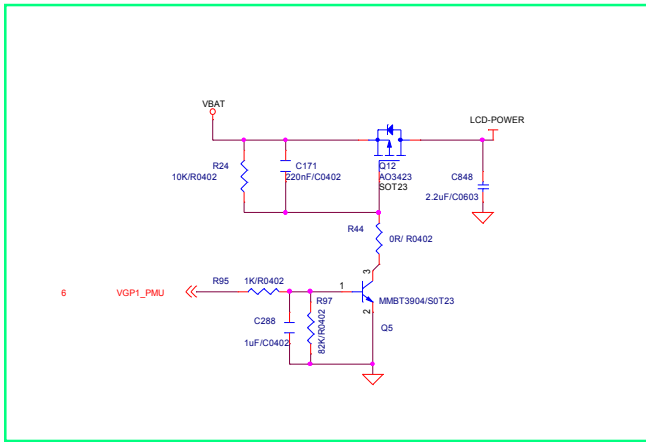


GPS

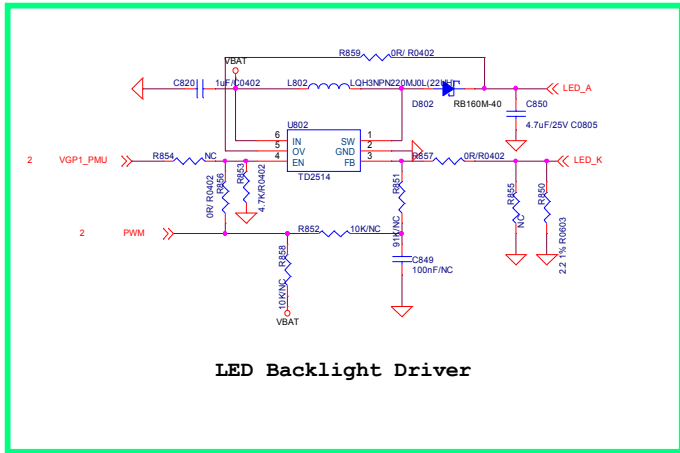
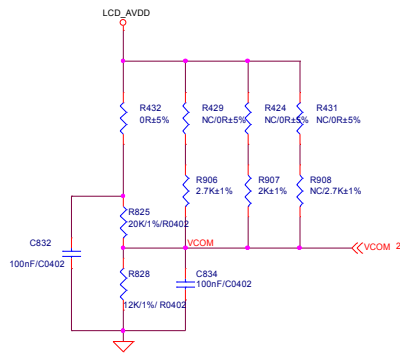
Close to ANT



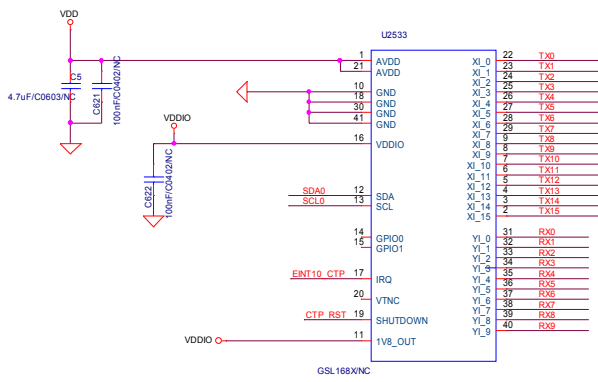




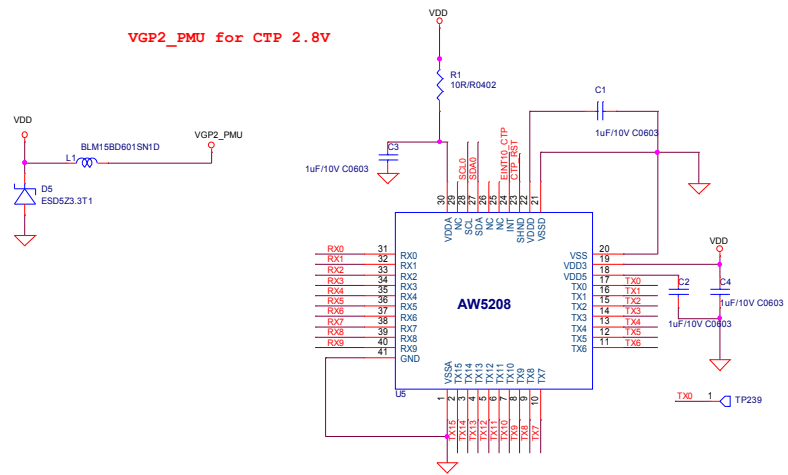
DVDD	3.0 ~ 3.6v (typ. 3.3v)
AVDD	10.8 ~ 11.2v (typ. 11.0v)
VGH	19.7 ~ 20.3v (typ. 20.0v)
VGL	-7.1 ~ -6.5v (typ. -6.8v)
VCOM	3.46 ~ 3.86v (typ. 3.66v)



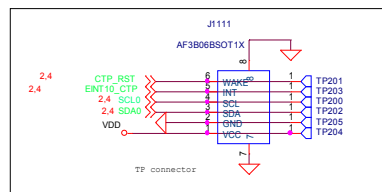
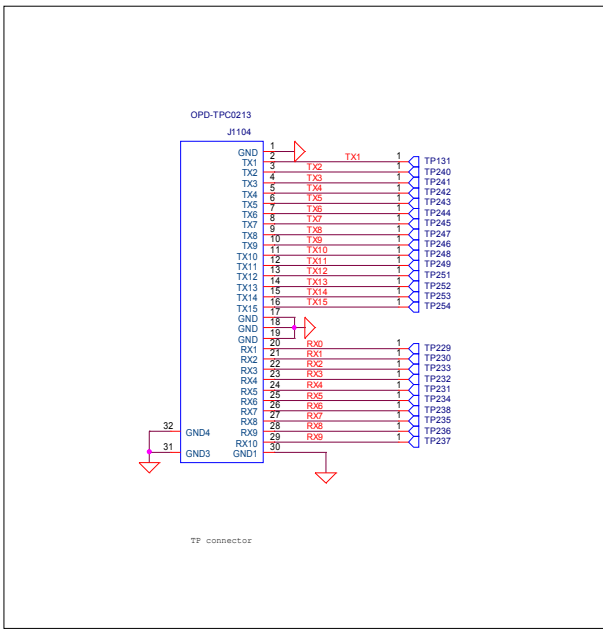
LED Backlight Driver



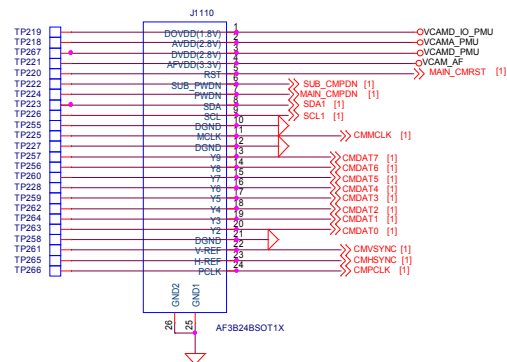
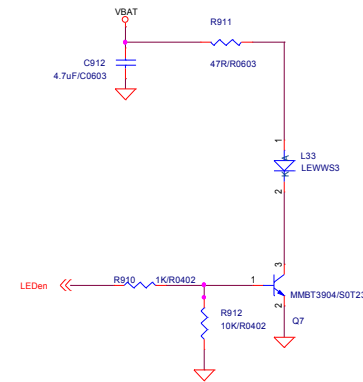
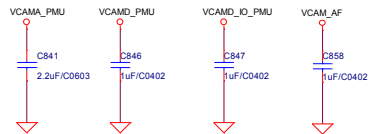
VGP2\_PMU for CTP 2.8V



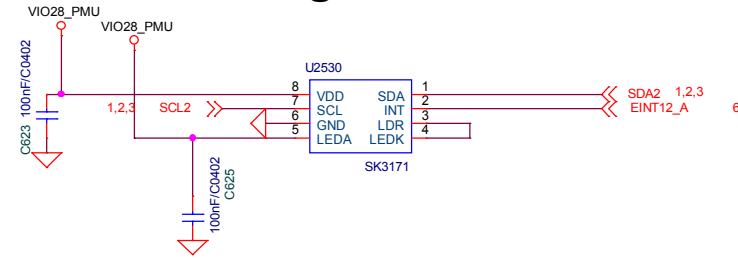
Touch Panel IC circuit



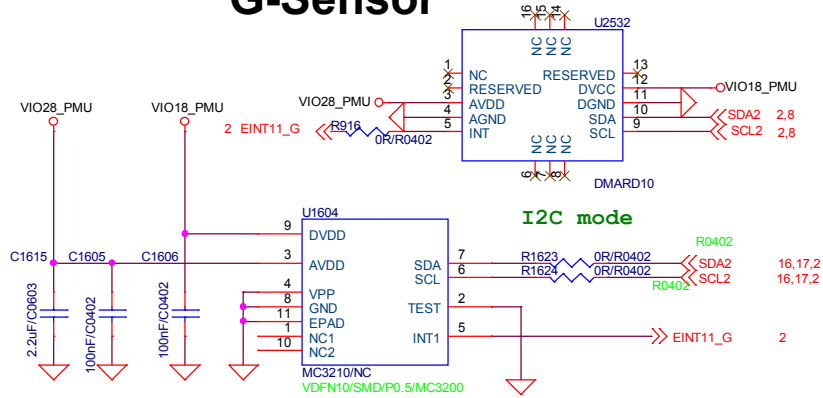
# Main/Sub Camera



# Light-Sensor



# G-Sensor

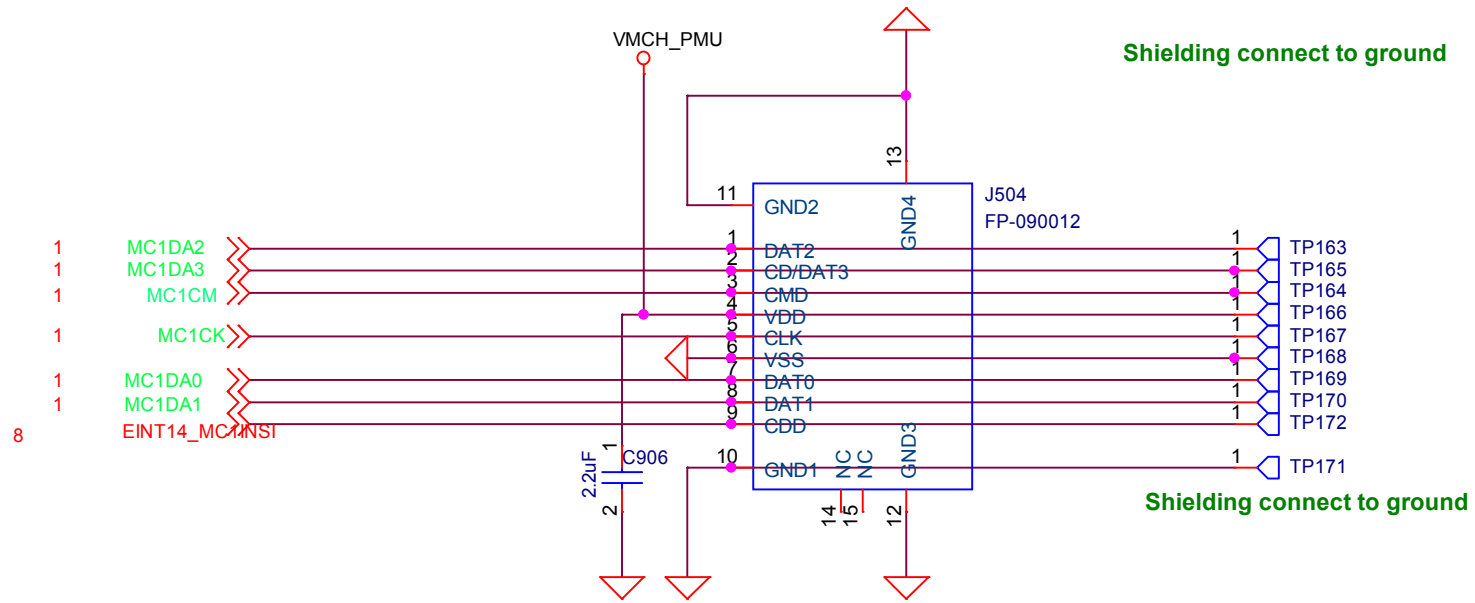


I2C Address: 0x4C (Write:0x98, Read:0x99)

**MEDIATEK**

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# SD CARD

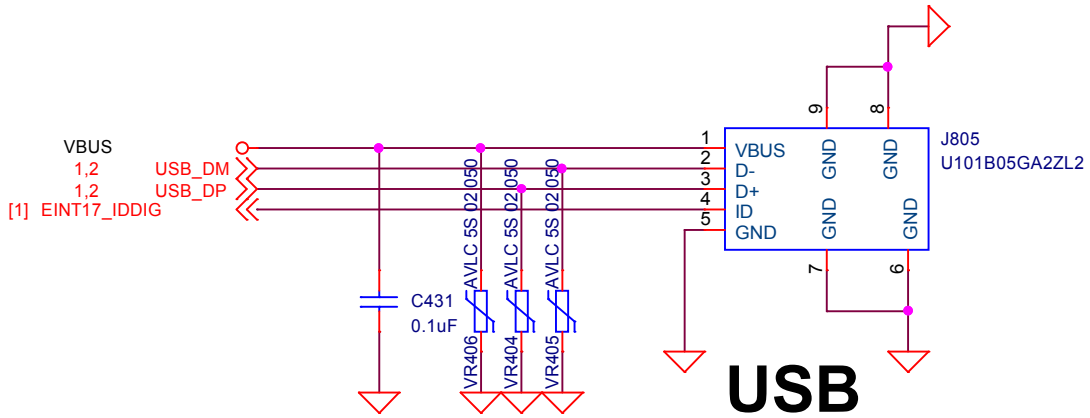
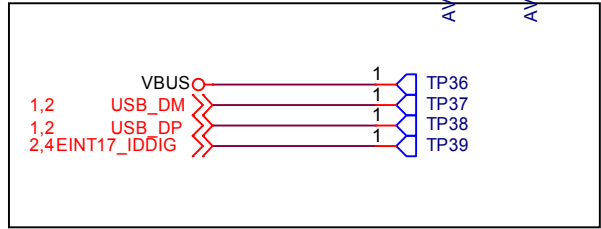
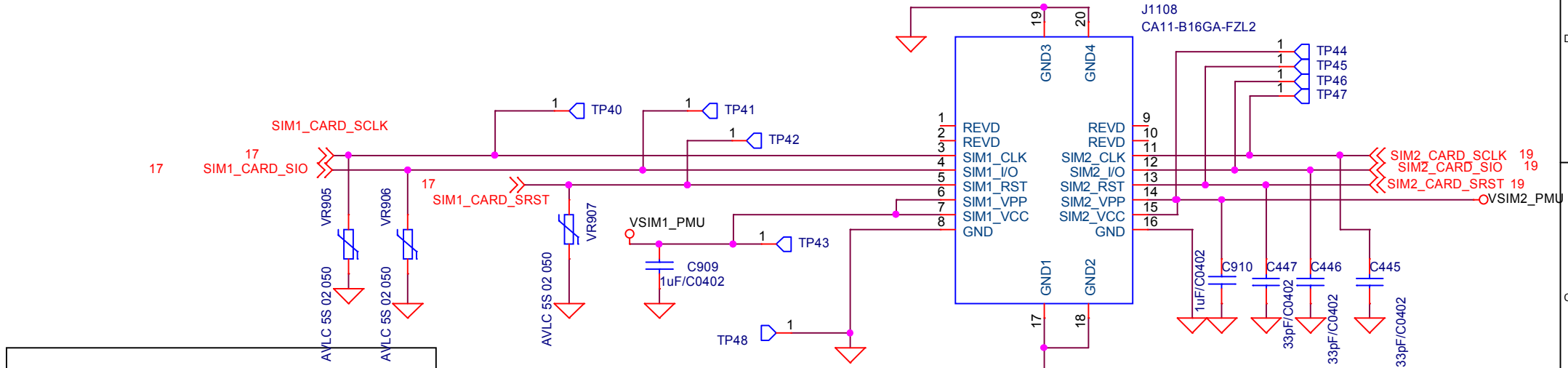


**MEDIA**TEK

Title		
<b>18 Memory CARD</b>		
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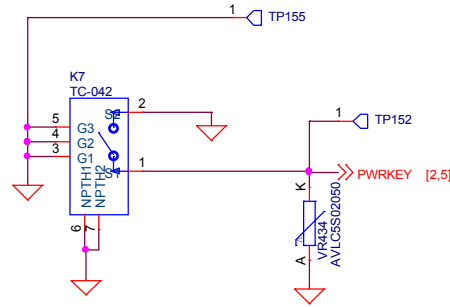
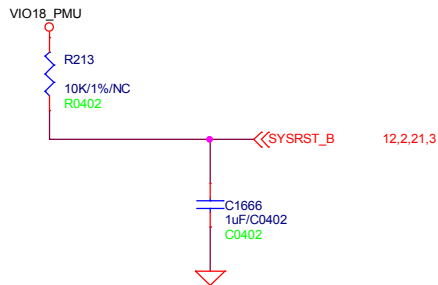
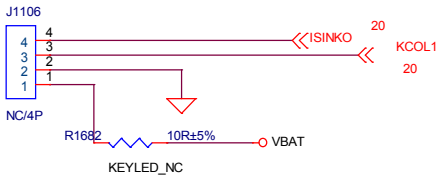
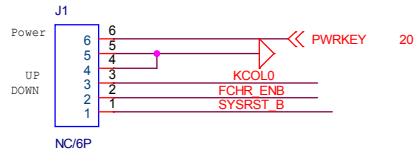


# SIM

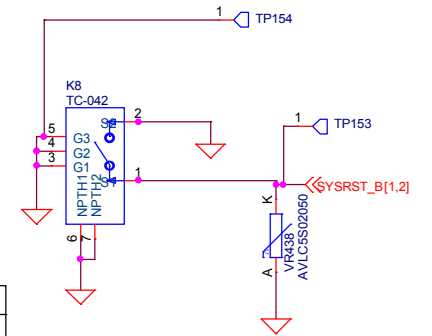
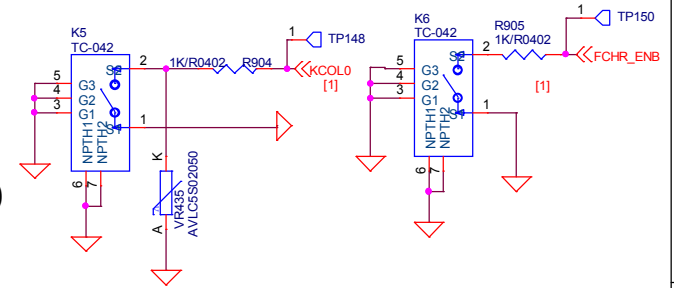


# USB

<b>MEDIATEK</b>		
Title		
<b>19 Dual SIM, IC-USB</b>		
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# LED

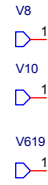
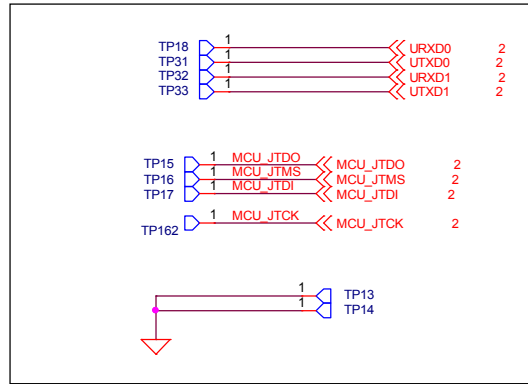


	KCOL0	KCOL1	KCOL2
KROW0		KEY 2	KEY 5
KROW1	KEY 1	KEY 3	KEY 6
KROW2		KEY 4	KEY 7

Notice :  
 There are 3 options for "Long press to shutdown" function  
 1.PWRKEY + FCHR\_ENB  
 2.PWERKEY only  
 3.FCHR\_ENB only

During download mode, default = PWRKEY + FCHR ENB  
 For other case (exclude download mode), default = PWERKEY only

<b>MEDIATEK</b>		
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Net	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5
JTMS	GPIO76	B1:JTMS	I1:CONN_MCU_TMS			
JTCK	GPIO77	I0:JTCK	I0:CONN_MCU_TCK1			
JTDI	GPIO78	I1:JTDI	I0:CONN_MCU_TDI			
JTDO	GPIO79	O:JTDO	O:CONN_MCU_TDO			
EINT1	GPIO1	O:PWM2	O:DPI_D5	I0:MD_EINT1	O: TDD_TDO	O:CONN_MCU_TDO
EINT2	GPIO2	O:CLKM0	O:DPI_D6	I0:MD_EINT2		O:CONN_MCU_DBGACK_N
EINT3	GPIO3	O:CLKM1	O:DPI_D7	I0:SPI_MI	I0:MD_EINT3	I1:CONN_MCU_DBGI_N
EINT4	GPIO4	O:CLKM2	O:DPI_D8	O:SPI_MO	I1:TDD_TCK	I0:CONN_MCU_TCK0
EINT5	GPIO5	I1:UCTS2	O:DPI_D9	O:SPI_CS	I1: TDD_TDI	I0:CONN_MCU_TDI
EINT6	GPIO6	O:URTS2	O:DPI_D10	O:SPI_CK	I0:TDD_TRSTN	O:CONN_MCU_TRST_B
EINT7	GPIO7	I1:UCTS3	O:DPI_D11	B1:SDA1	I1: TDD_TMS	I1:CONN_MCU_TMS
ANT_SEL0	GPIO47	O:ANT_SEL0	O:PWM0	O:CONN_MCU_DBGACK_N		
ANT_SEL1	GPIO48	O:ANT_SEL1	O:PWM1	I1:CONN_MCU_DBGI_N		
ANT_SEL2	GPIO49	O:ANT_SEL2	O:PWM2	I0:CONN_MCU_TRST_B		

**MEDIATEK**

Title: **97 Debug**

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