As is evident in the above block diagram, this product employs dual-conversion superhet architecture for its receiver. The first IF (Intermediate Frequency) is 21.4MHz. The second IF is 450kHz. The local oscillator signal is PLL-synthesized to ensure accuracy and stability. A microcontroller with appropriate firmware is designed to program the PLL to the desirable user-selected channel for either transmit or receive.

Circuit Description

Receive mode

The antenna is connected to the low noise amplifier Q14 via the T/R switch formed by D8 and D7, L1, C69 and C70. During reception (RX), D7 and D8 are off. The incoming RF signal is routed to Q14 via the pi-network formed by L1, C69 and C70. The amplified RF signal is coupled to the first mixer Q15. The first local oscillator signal is PLL-synthesized. Q18 is the VCO which is tuned by the filtered error voltage from the PLL chip U5. Channel selection is accomplished by sending appropriate data to U5 via a 3-wire serial bus. This is taken care of by microcontroller U1. The 21.4MHz crystal filter at the mixer output selects the desirable IF signal while rejecting other mixing products. The first IF signal is amplified by Q16 and then passed to U6 which contains the second mixer/local oscillator, IF amplifier/limiter and quadrature FM demodulator. The demodulated FM signal is filtered by the deemphasis network and low-pass filter formed by R1,R2,C25 and an internal OP-AMP in U7. The filtered audio signal is then routed to the power amplifier (U4) which drives the loudspeaker.