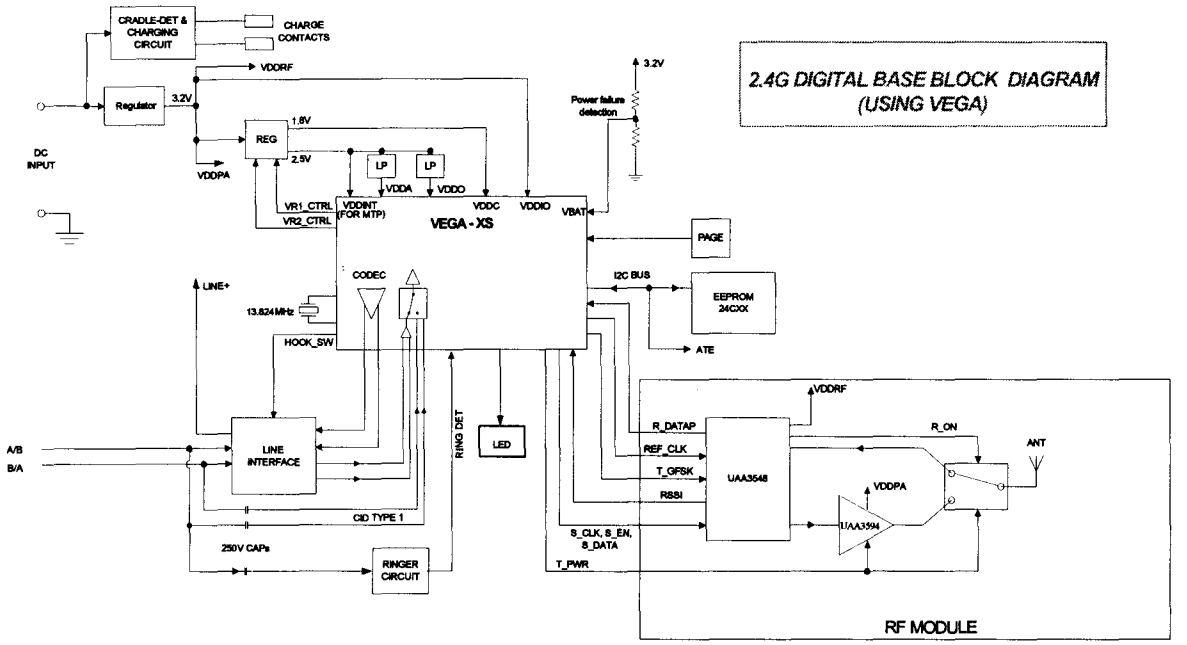
Theory of Operation for 27902XX1-A /27903XX1-A

FCC ID: G9H2-7903A
Marstech Report No. 26224D/26226D
EXHIBIT C(1)-1

1 BASE UNIT BASEBAND



1.1 The Hybrid Circuit

The line interface circuit used in US 2.4 DCT is no Hi-Pot isolation. So, a special mechanical design is needed to avoid accessibility of metallic parts (like charge contacts) by human fingers.

1.2 The Ringer Detection Circuit

Ringer detection is done by Q8 through the high voltage capacitors. Detection logic is fed into the Vega chip.

1.3 The Vega Chip in Base

The Vega chip is a base-band controller. It handle all the detection & control in base which including ringer detection, power drop detection, cradle detection, page key press, RF control, LED control and line-interface control.

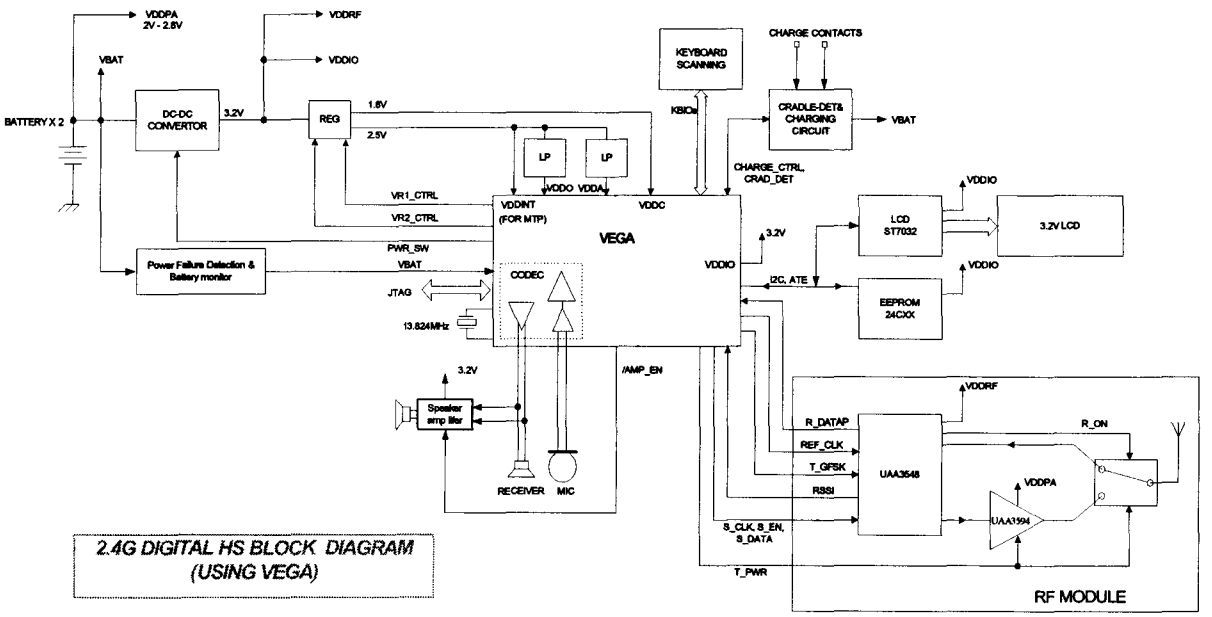
1.4 Power Supply & charging in the Base

A regulator U1 is used to regulate the DC adaptor to 3.2V supply for the system. There are two sub-regulators (Q9, D5, Q11, Q13) are used to generate the necessary voltages for the sub-system (VDDA, VDDO, VDDINT & VDDC) in Vega chip. For the VDDIO, the Vega chip gets from 3.2V output directly.

A resistor is used for the supply of charging circuit.

FCC ID: G9H2-7903A
Marstech Report No. 26224D/26226D
EXHIBIT C(1)-2

2 HANDSET BASEBAND



2.4G DIGITAL HS BLOCK DIAGRAM (USING VEGA)

2.1 LCD Module

The LCD module is using COG (Chip-On-Glass) technology and interface with Vega chip through IIC bus.

2.2 The Vega Chip in Handset

The Vega chip is a base-band controller. It handle all the detection & control in handset which including charge detection, power drop detection, keyboard scan, RF control, LCD control and charging control.

2.3 Power Supply Design in the Handset

A build-in DC-DC controller in Vega chip up-converts the 2-cell voltage up to 3.2V with the external inductor, diode D6 and FET Q5. Same as base, two sub-regulators (Q9, D4, Q1 & Q2) are used to generate the necessary voltages for the sub-system (VDDA, VDDO, VDDINT & VDDC) in Vega chip. For the VDDIO, the Vega chip gets from 3.2V output directly.

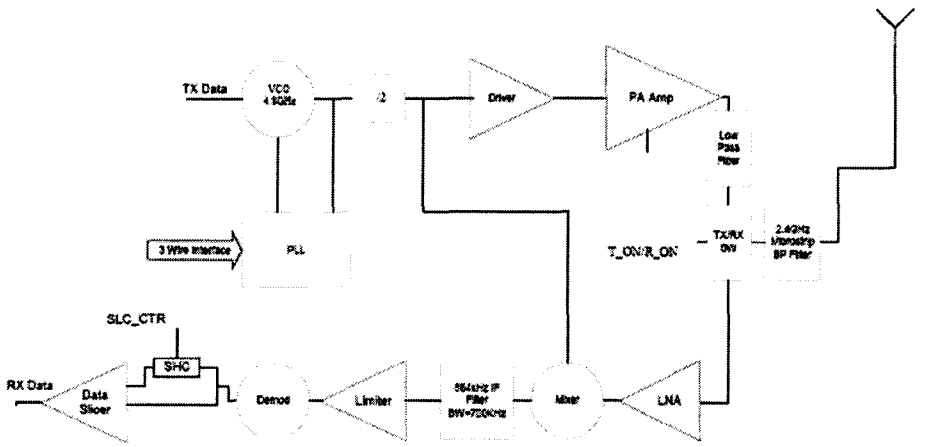
2.4 The Charging Circuit

Q10, D1 and D2 forms a regulator like charging circuit which including over-voltage protection when the handset is placed on cradle without the battery. Slow charge is achieved by turn-off Q10 periodically.

FCC ID: G9H2-7903A
Marstech Report No. 26224D/26226D
EXHIBIT C(1)-3

The RF Module

The same RF module is used in both handset and base. It is including a transceiver U1 and a power amplifier U2 and both are controlled by the Vega chip.



2.5 VCO/PLL Section

The UAA3548 is designed with an oscillator. The tank circuit including the inductors and varactor diode are internal build-in inside the IC. The VCO operates at 4.8GHz and is then divided to 2.4GHz.

The PLL uses a pre-scalar to divide down the 2.4GHz signal. The baseband crystal frequency (13.824MHz) is buffered by the baseband ASIC and routed to the RF module. This crystal frequency is divided down to the phase comparator reference frequency of 864kHz. The transmitter uses open loop modulation. As a result, the loop filter capacitors are required to be COG to minimize their voltage decay during the tri-state mode of the PLL. The VCO is supplied by an on-chip regulator, which minimizes frequency disturbances due to VCC variations.

At the beginning of the guard slot, the UAA3548 is turned on and the synthesiser program word is loaded into the IC setting the desired frequency in TX or RX mode. The VCO then locks and settles during the remaining guard slot time just before the beginning of the active slot, a falling edge of S_EN is sent. The PLL is then switched off and the IC is ready for an active slot. If it is a receive slot, the LNA and mixer will be activated. If it is a TX slot, the driver will be enabled by the SLICE signal. During the RX slot the SLICE is used for the data slicer calibration.

2.6 TX Chain

The TX DATA is a Gaussian shaped (ß=0.8) signal that directly modulates the VCO. The data rate is 1.152Mbps. The TX DATA is applied to the anode of the tank varactor diode. This modulation can be accomplished because during the TX active slot, the charge pump from the PLL goes tri-state. The use of COG capacitors in the loop filter ensures a frequency drift of less then 10kHz during an active slot. The modulated carrier is a GFSK signal at 4.8GHz. This modulated carrier is then divided to 2.4 GHz.

The 2.4GHz signal is amplified through a pre-amplifier inside the UAA3548. The output from the driver has differential amplitude of +3dBm. This differential signal is fed to balun circuit and is then fed to the UAA3594 providing an output level of +24dBm. The output of the power amplifier goes through a low pass filter to remove any harmonic content (e.g. 4.8GHz, 7.2GHz). After the LP filter is the TX/RX switch controlled by the UAA3548. The signal, T_ON, goes high to switch the diode and the circuit is selected to the TX path. The output of the switch is connected to a 2.4 GHz printed bandpass filter. The printed bandpass filter is further filter out harmonic content of the signal.

The output of the printed BPF is routed to the antenna with a power level of <1W conducted in to the antenna as per the FCC requirement.

2.7 RX Chain

The front end circuitry is the same as the TX Chain. The antenna is connected to the bandpass filter.

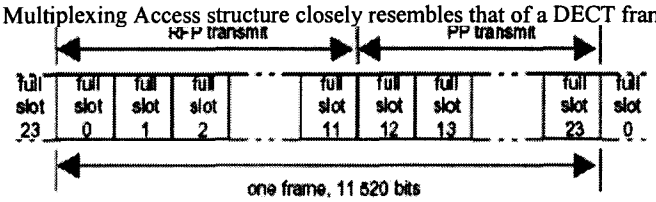
The bandpass filter connects to the TX/RX Switch. In RX mode, R_ON goes high to switch the diode to RX path. The output of the switch fed into a balun to change the signal to differential-ended. Then it is connected to the LNA. The LNA input is differential and the LNA matching incorporates phase shifting and noise figure matching. The output of the LNA is connected to the input of the image reject mixer. The mixer achieves >35dB of image rejection. The mixer's LO is set by the VCO. The output of the mixer is at 864kHz, the IF frequency.

The 864kHz output from the mixer is passed through an internal IF bandpass filter. The output of this filter connects to a limiter stage. The limiter amplifies the signal and its output connects to the demodulator. The demodulator FM demodulates the 864kHz to a baseband analogy signal. The recovered signal is fed through a low pass post detection filter. The recovered data is then separated to two paths. One is the data going directly to the data slicer. The second is the reference voltage for the data slicer. The 0101 preamble at the beginning of each RX slot is used to determine the average DC voltage of the incoming data. This voltage is charged on the reference capacitor, CSHC, and locked by the falling edge of the SLICE signal. Once locked, this voltage is used by the data slicer as a reference to shape the data. The output of the data slicer is the signal that is delivered to the Baseband section.

3 System description

3.1 TDMA Structure

The Time Division Multiplexing Access structure closely resembles that of a DECT frame structure.



*RFP stands for Radio Fixed Part, in this application; it refers to a base station (BS).

*PP stands for Portable Part, in this application; it refers to a handset (HS).

One frame is 10ms long and repeat at the end of a frame. Each frame consists of 24 full slots. The 24 full slots, defined by DECT protocol, are combined into 12 individual operating slots. The 12 operating slots are divided into 2 sections each having 6 slots. The first section handles BS transmission traffics and the second section handles HS transmission traffics.

Each operating slot occupies 833.3us in a single 10ms frame. A single TX operating slot consists of 416.7us of guard time and 416.7us of transmission traffic time. i.e., each single slot will occupy 416.7us spectrum resource in 10ms time frame, or 4.2% duty cycle per slot for particular frequency.

Each system consists of **1 base and 1 handset only**. The base transmits a dummy bearer on the 1st slot. The handset registered to the system is able to receive and synchronise to the dummy bearer. The handset periodically wakes up and receives the dummy bearer from the base. If required, the handset transmits a packet back to the base on the dummy bearer's corresponding receive slot time.

When a dedicated link between the base and a handset is required, a traffic bearer is created on one of the slot-pairs. The handset and base then begin exchanging data using the traffic bearer. The channel frequency will not change until a handover occurs. The dummy bearer remains. At the end of the link, the traffic bearer is released and the handset returns to the dummy bearer.

The slot-pairs (a RFP/BS and a PP/HS TX operating slot) are not permanently assigned to a handset but instead are dynamically assigned to a handset/base link as necessary.

At the busiest condition, three communication links in the system can be active at the same time. They may use the same frequencies but different time slots. Including the dummy bearer, BS may transmit at 2 slots at the same frequency or duty cycle is 4.2% x 2 = 8.2% in worst case. HS will only transmit at 1 slot or duty cycle is 4.2% in worst case.

3.2 Handover during interference

Whenever interference is detected by the baseband error detection algorithm, handover procedure starts to operate. The handover procedure may switch to a different frequency channel and a different time slot that is less prone to interferences.

3.3 Channel Frequency Plan

Channels	2.4GHz Freq Plan
*0	2406.24
1	2410.56
2	2419.20
3	2427.84
4	2436.48
*5	2445.12
6	2453.76
7	2462.40
8	2471.04
*9	2475.36

*note: Ch0, 5, 9 is the three channels for FCC part 15(c) measurement.