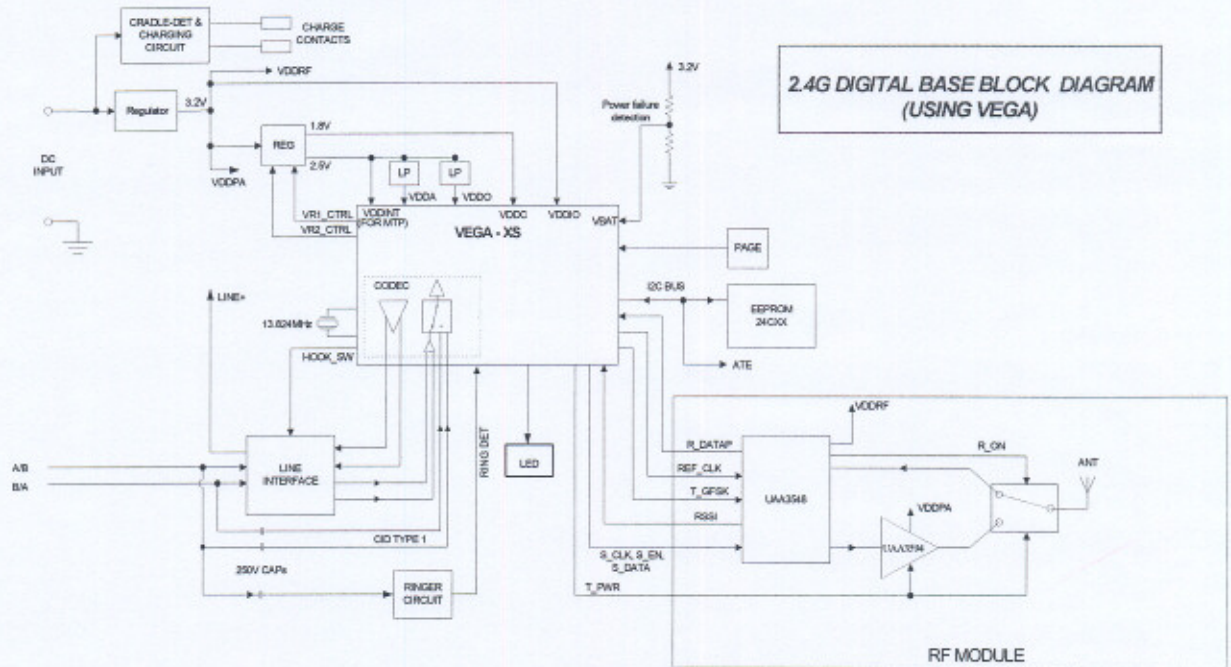
1 BASE UNIT BASEBAND



1.1 The Hybrid Circuit

The line interface circuit used in US 2.4 DCT is no Hi-Pot isolation. So, a special mechanical design is needed to avoid accessibility of metallic parts (like charge contacts) by human fingers.

1.2 The Ringer Detection Circuit

Ringer detection is done by Q8 through the high voltage capacitors. Detection logic is fed into the Vega chip.

1.3 The Vega Chip in Base

The Vega chip is a base-band controller. It handle all the detection & control in base which including ringer detection, power drop detection, cradle detection, page key press, RF control, LED control and line-interface control.

1.4 Power Supply & charging in the Base

A regulator U1 is used to regulate the DC adaptor to 3.2V supply for the system. There are two sub-regulators (Q9, D5, Q11, Q13) are used to generate the necessary voltages for the sub-system (VDDA, VDDO, VDDINT & VDDC) in Vega chip. For the VDDIO, the Vega chip gets from 3.2V output directly.

A resistor is used for the supply of charging circuit.

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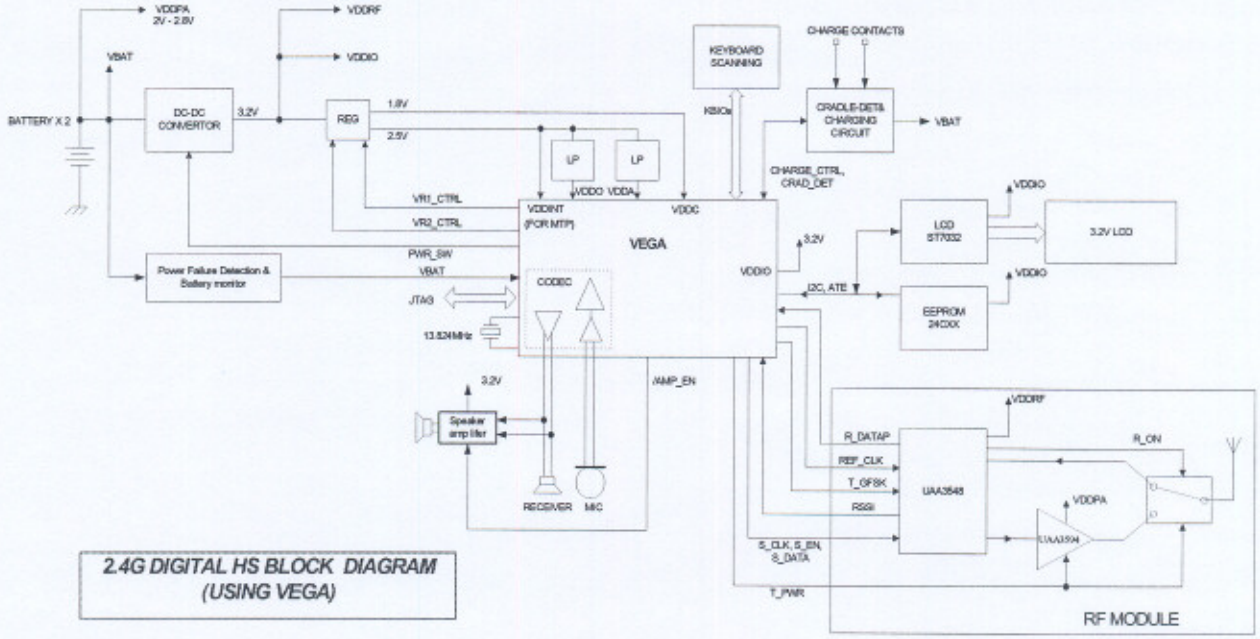
2 HANDSET BASEBAND



2.4G DIGITAL HS BLOCK DIAGRAM (USING VEGA)

2.1 LCD Module

The LCD module is using COG (Chip-On-Glass) technology and interface with Vega chip through IIC bus.

2.2 The Vega Chip in Handset

The Vega chip is a base-band controller. It handle all the detection & control in handset which including charge detection, power drop detection, keyboard scan, RF control, LCD control and charging control.

2.3 Power Supply Design in the Handset

A build-in DC-DC controller in Vega chip up-converts the 2-cell voltage up to 3.2V with the external inductor, diode D6 and FET Q5. Same as base, two sub-regulators (Q9, D4, Q1 & Q2) are used to generate the necessary voltages for the sub-system (VDDA, VDDO, VDDINT & VDDC) in Vega chip. For the VDDIO, the Vega chip gets from 3.2V output directly.

2.4 The Charging Circuit

Q10, D1 and D2 forms a regulator like charging circuit which including over-voltage protection when the handset is placed on cradle without the battery. Slow charge is achieved by turn-off Q10 periodically.

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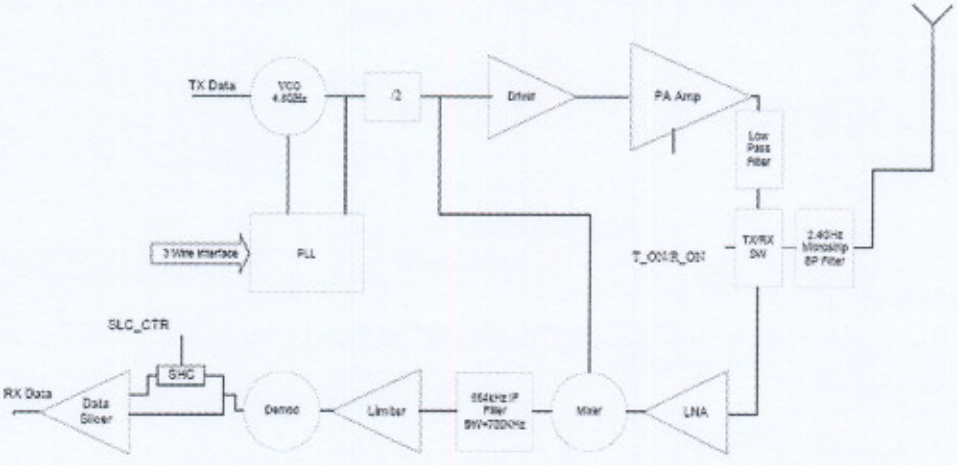
The RF Module

The same RF module is used in both handset and base. It is including a transceiver U1 and a power amplifier U2 and both are controlled by the Vega chip.

The transceiver handles all the 2.4G RF transmit and receive. The power amplifier increase the transmit power to increase the range of the system.



2.5 VCO/PLL Section

The UAA3548 is designed with an oscillator. The tank circuit including the inductors and varactor diode are internal build-in inside the IC. The VCO operates at 4.8GHz and is then divided to 2.4GHz.

The PLL uses a pre-scalar to divide down the 2.4GHz signal. The baseband crystal frequency (13.824MHz) is buffered by the baseband ASIC and routed to the RF module. This crystal frequency is divided down to the phase comparator reference frequency of 864kHz. The transmitter uses open loop modulation. As a result, the loop filter capacitors are required to be COG to minimize their voltage decay during the tri-state mode of the PLL. The VCO is supplied by an on-chip regulator, which minimizes frequency disturbances due to VCC variations.

At the beginning of the guard slot, the UAA3548 is turned on and the synthesiser program word is loaded into the IC setting the desired frequency in TX or RX mode. The VCO then locks and settles during the remaining guard slot time just before the beginning of the active slot, a falling edge of S_EN is sent. The PLL is then switched off and the IC is ready for an active slot. If it is a receive slot, the LNA and mixer will be activated. If it is a TX slot, the driver will be enabled by the SLICE signal. During the RX slot the SLICE is used for the data slicer calibration.