EXHIBIT B

[FCC Ref. 2.1033(b)(4)]

"Description of Circuit Functions"

Exhibit B(1)-1 to B(1)-3 - Circuit Description and
Statement of Digital Security Code

27673A CIRCUIT DESCRIPTION

The following circuit description is for model 27673A which are base on the circuit diagram & block diagram.

1. RECEIVING SECTION (BASE)

a. LNA, MIXER, LO and IF amp.

The received frequency will pass through a band pass filter (F16). A low noise amplifier (Q18) will amplify this signal and will be mixed with 2nd LO (local oscillator) frequency derived from the second harmonics of the 1st LO. The mixer (Q23) will amplify the output signal which is the difference between the received frequency and the 2nd LO and will pass through a band pass filter (F18). It will be mixed with the 1st LO signal to attain the IF (10.7MHz) signal. This IF will be filtered further by CF1. The filtered IF will be amplified by the built-in LNA of the COMBO chip IC (U1) and filtered by F2 before demodulation. The LO frequency is generated by the PLL circuit of the combo IC and the VCO circuit (Q20).

b. *Demodulator, Expander, Audio Amp*

The demodulated signal will be filtered by a low-pass filter to remove residual IF frequency. The filtered audio will pass through a built-in expander then amplified by a built-in amplifier.

c. Final AUDIO amp, Hybrid, RELAY

The audio output from the module will be amplified by the final amplifier (IC1-B). This will also amplify the DTMF signal of the system before sending it to the PSTN. Hybrid provides isolation and a line match to the PSTN. This would also couples the audio to the network and provide the desired side-tone signal to the near-end party. Q3 and IC8 provide the line switch. This also provides the line break and pulse dialing.

2. TRANSMITTING SECTION (BASE)

a. Compressor, Splatter, Modulator

The received line audio and side tone signal from the hybrid will go to the audio input of the combo chip. It will pass through a compressor. From the output of the compressor, it will go to the splatter circuit. The audio will then modulate the Tx VCO (Transmit Voltage Controlled Oscillator) frequency of the modulator (Q13) which is controlled by the PLL of the combo IC.

b. Pre-Amp, Final Amp

The 3rd harmonics of the Tx VCO frequency is extracted by pre-amp (Q11) and amplified by Q7. The final Tx signal is then passed through a filter F15 to reduced unwanted harmonics. It is then transmitted through the antenna.

3. RECEIVING SECTION (HANDSET)

a. LNA, MIXER, LO and IF Amp.

The received frequency from the antenna will pass through a band pass filter (F16). A low noise amplifier (Q18) will amplify this signal and will be mixed with 2nd LO (local oscillator) frequency derived from the second harmonics of the 1st LO. The mixer (Q23) will amplify the output signal which is the difference between the received frequency and the 2nd LO and will pass through a band pass filter (F18). It will be mixed with the 1st LO signal to attain the IF (10.7MHz) signal. This IF will be filtered further by CF1. The filtered IF will be amplified inside the built-in LNA of the COMBO chip IC (U1) and filtered by F2 before demodulation. The LO frequency is generated by the PLL circuit of the combo IC and the VCO circuit (Q20).

b. Demodulator, Expander, Audio Amp, Receiver

The demodulated signal will be filtered by a low-pass filter to remove residual IF frequency. The filtered audio will pass through a built-in expander then amplified by a built-in amplifier and finally to the receiver.

4. TRANSMITTING SECTION (HANDSET)

a. Compressor, Splatter, Modulator

The received line audio and side tone signal from the hybrid will go to the audio input of the combo chip. It will pass through a compressor. From the output of the compressor, it will go to the splatter circuit. The audio will then modulate the Tx VCO (Transmit Voltage Controlled Oscillator) frequency of the modulator (Q13) which is controlled by the PLL of the combo IC.

b. Pre-amp, Final amp

The 3rd harmonics of the Tx VCO frequency is extracted by pre-amp (Q11) and amplified by Q7. The final Tx signal is then passed through a filter F15 to reduced unwanted harmonics.

5. CVSD CIRCUIT OPERATION

a. Clock recovery scheme H/S to B/S;

The MXCOM CMX639 CVSD chip has an internal divider of 16K, 32K, 64K. Our circuit used 16K to get the maximum data rate for better resolution of the audio signal (High S/N) The 8MHz oscillator for MCU X1 is fed to an external divider U7 74HC4040 using its 8th divider to obtain 1MHz, this will be divided by CMX 639 with its internal divider (16K) resulting clock frequency is 62.5KHz which is then fed to an EX-OR together with the encoded audio signal. The clock is then embedded in the CVSD data stream and will be recovered on the base with our clock recovery system.

Our clock recovery circuit is composed of an EX-OR 74HC86 charge pump, a phase detector using D flip-flop 74HC74, a self oscillating ceramic controlled VCO (Fc = 4MHz) a hyper active varactor diode SMV1255 to track the variations and an external divider 74HC4040. The demodulated audio from the combo chip's AF output is fed to a data slicer 74HC04 for signal reconditioning, the output of which is fed to the hold/release circuit of 74HC74 to force the data to latch to our target frequency of 4MHz, the other

side is connected to the integrator 74HC86 which also happens to be the charge pump. The output of the charge pump goes to the LPF RC lead/lag circuit chosen for fast lock. Varactor diode D30 tunes the output to variations of the recovered information. The 4MHz corrected clock is then divided by 16 by U7 74HC4040, so the resulting clock is 250KHz, this 250KHz is further trimmed by U8 74HC74 with it's 4th divider thus 62.5KHz is obtained and will be used as an input to the encoder/decoder clock input of U6 CMX639 CVSD encoder/decoder. The 62.5 clock is then used to by CMX639 to decode the audio encoded in CVSD format from the voice origin.

6. TELEPHONE LINE INTERFACE

The telephone line interface circuit is established by below sections:

a. Audio power amplifier

Operational Amplifier, LM324 are built as a power amplifier, according to high current output requirement of line interface.

b. Telephone line relay and isolation transformer

T1 is the line isolation transformer, both audio input and output are passing through this transformer. RL1, Relay is for line-seize, which controlled by Q1.

c. Ring-detect circuit

IC3-A and IC3-B are used as differential amplifier for picking up the ring signal, which input from two 20MΩ resistors (R37 and R38) as an isolation from the telephone line.

7. 27673A DIGITAL SECURITY CODE SYSTEM:

The handset and base of 27673A will exchange a random generated 16-bit digital security code when every time the handset put back on the charging cradle of the base unit. This is to fulfill FCC Part 15.214(d) requirement regarding there must be at least 256 possible discrete digital codes.

***** End *****