CCT TELECOM

Date: 21 February,2005
Rev: 1.0a

Description of Cell Docking System

Introduction

With the intensively use of Cell phone, the system cost for leasing a fixed line is even lower than those of traditional land line. With this advantage issue, a residential phone and Cell phone integrated product will be outcomed which can provide the advanced features of likes Multi-handset feature. The multi-handset part will use our mature system of DSPG platform. We are now using the 2.4GHz Frequency Hopping System on the multi-handset systems.

System Block Diagram Description

Cell-Docking Station

(1) Multi-handset Baseband Part

We use the chip DSPG DLH36107 which always used in the 2.4GHz and 5.8GHz multi-handset digital platform. The Cell Docking cradle part will be treated as a separated handset system which is always synchronizing to the base of the multi-handset. With multi-time slots system, a base system can register up to four handsets include the cell docking part. The baseband controller DLH36107 is responsible for burst-mode controller of the system (i.e the system timing for the multi-handsets system such as TDD time control. It also includes the features for the audio part switching and codec functions.

(2) RF Transceiver part

RF signal is picked up by a solid wire antenna, then goes to DH24RF17B transceiver IC which includes LNA, Mixer, Synthesizer, RF power amplifier and TDD switches for 2.4GHz RF part.

The baseband controller DLH36107 is responsible for burst-mode controller of the system (i.e the system timing for the multi-handsets system such as TDD time control. It also includes the features for the audio part switching and codec functions.

The hopping sequence algorithm is same for caller ID and Voice Transmission. Voice and Data can be in same slot. No specific test mode is needed because in frame structure, only data is handled in different field in one frame.

(3) Cell phone Interface

We have used a MCU TMP92CH21 to act as the interface chip for the cell phone. With this chip, we can preform the software upgradable by using the on-chip USB function. With this software upgradable feature, we can easily upgrade the firmware whenever there have new cellphones introducing to market after the cell docking systems purchased or manufactured. The software upgrade features is used to upgrade the support feature (new phones and/or new features). It won't affect the data rates of the USB.

The cell phone interface based on the concept of the UART and FBUS. Most of the cell phones have integrated with either UART or FBUS configurations. And all these configurations are software re-configurable, the determination of the UART or FBUS will be selected with the cell phone manual selected on the panel of the cell docking and indicated on the LCD.

(4) TMP92CH21 to DLH36107 interface

We planned to have a quite a lot of data transfer (CID data, phone book, etc) between the TMP92CH21 and the DLH36107, a software-simulated SPI interface will be used which has comparatively high data rate handling.

(5) UART interface for ATE setup

ATE means the Automatic Testing setup which is used for the production setup likes parameters tuning, system parameters updating, ID codes, etc. The cell docking system will interface with Personal Computer (tester) by software UART port.

(6) Programming Charger

The charger comprises of a DC-DC convertor. With different cellphones, the input voltage is different. The corresponded information will be stored in Flash ROM inside the Cell Docking System. The voltage output of the DC-DC convertor can be controlled by setting the feedback resistors. The selection is controlled by TMP92CH21 controller.

Handset Unit

RF signal is picked up by a solid wire antenna, then goes to DH24RF17B transceiver IC which includes LNA, Mixer, Synthesizer, RF power amplifier and TDD switches for 2.4GHz RF part.

The baseband controller DLH36107 is responsible for burst-mode controller of the system (i.e the system timing for the multi-handsets system such as TDD time control. It also includes the features for the audio part switching and codec functions.

Base Unit

(1) RF Transceiver part

RF signal is picked up by a solid wire antenna, then goes to DH24RF17B transceiver IC which includes LNA, Mixer, Synthesizer, RF power amplifier and TDD switches for 2.4GHz RF part.

The baseband controller DLH36119 is responsible for burst-mode controller of the system (i.e the system timing for the multi-handsets system such as TDD time control. It also includes the features for the audio part switching and codec functions.

(2) Antenna Diversity

Antenna diversity is implemented by CR2, CR3 (BAR64-02V) to select alternately the two antennas ANT_A, ANT_B respectively for TX/RX.

(3) Telephone Line interface

The telephone line interface circuit is established by below sections

Line seize and isolation

Line isolation is mainly preformed by Q10, Q13 and Q12. Q12 also has a function of controlling Line-seize. Both audio input and output will though Q10 and Q13.

Ring detect and CID circuit

The ring and CID signal will input though R113, R114 470K ohm and C43, C44 1nF/500V as DC isolation from telephone line.

EDCT

FCC Submission For 2.4GHz FHSS System

D30006 Rev 0.2

Pub: EDCT Rev: 0.2 Amendment: 0
Issue Date: 9 November 2004

Generation Summary

Property	Value
File Name	D30006 FCC Submission For FHSS System rev 0.2.doc
File Type	Microsoft Word 2000
Author	Steven Dickinson

Revision	Issue Date	Description
0.1	13 March 2003	Preliminary
0.2	9 Novemeber 2004	Removed statement about channel 71 (no longer valid)
0.2a	23 February 2005	Channel 71 is valid again

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DEFINITIONS, ACRONYMS AND ABBREVIATIONS

Channel collision	The simultaneous occupancy of a hopping channel by multiple transmitters.
DECT	Digital Enhanced Cordless Telecommunications.
EIRP	Equivalent isotropically Radiated Power.
ETSI	European Telecommunications Standards Institute.
FCC	Federal Communications commission (the body in the USA that regulates the use of the radio spectrum).
FH	Frequency Hopper: the name of the software component responsible for frequency hopping.
FHSS	Frequency Hopping Spread Spectrum.
FP	Fixed Part or base-station.
Hand-over	A process by which a second traffic bearer is established to carry an existing call. Once established the first traffic bearer can be released.
HSI	Hope Sequence Index: used to index into the pattern table.
ISM	Industrial, Scientific, Medical band: a radio frequency band in the range 2400 – 2483.5 MHz
LCG	Linear Congruential Generator: a type of random number generator
LDC	Low Duty Cycle: a power saving feature.
OET	Office of Engineering and Technology, a division of the FCC.
PP	Portable Part or handset.
PSCN	Primary Scan Carrier Number; used in DECT.
PSPN	Primary Scan Pattern Number; the analogue of the PSCN for frequency hopping.
Radio Cell	The area covered by a single FP.
RFPI	Radio Fixed Part Identity
RNG	Random Number Generator; more accurately a Pseudo-Random Number Generator or PRNG.
RSSI	Received Signal Strength Indication.
Sequence collision	When two transmitters, with overlapping radio cells, are using the same slot, pattern and phase within the pattern. Channel collisions will occur on every frame, until the slot, pattern or phase is changed.
TDD	Time Division Duplexing.
TDMA	Time Division Multiple Access.

1 INTRODUCTION

In the US the 2400 – 2483.5 MHz band (henceforth the 2.4 GHz band) is subject to FCC regulations, in particular Part 15 Section 247.

DSP Group has developed a base-band chip, RF solution and protocol stack for the cordless telephony market that uses the 2.4 GHz band. This system is known as EDCT. The EDCT protocol stack is based on a DECT standard protocol stack that has been modified to use frequency hopping spread spectrum (FHSS) techniques in order to meet the FCC requirements.

1.1 Scope

This document describes the salient features of the EDCT protocol stack as they relate to the FCC requirements for using the 2.4 GHz band.

2 BRIEF SYSTEM DESCRIPTION

The basic system is a cordless telephone system, based on DECT. Because DECT is such a fundamental part of the proposed system, a brief description of this is given first.

DECT is a low-power two-way digital wireless communications system. Whilst DECT is a general digital communications system, it is most commonly used for cordless telephone systems. In particular it is used for residential telephone systems.

DECT uses TDMA to provide two-way communication between a base-station and multiple hand-sets. In this document the base-station is referred to as the Fixed Part (FP) and the hand-set is referred to as the Portable Part (PP).

Unlike a DECT system, the EDCT system does not have exclusive use of the spectrum. It has to share the spectrum with other users. The EDCT system uses frequency hopping to share the spectrum with other users according to the requirements specified by the FCC.

It is the frequency hopping requirement that creates the biggest difference between a DECT and an EDCT system. The other main difference between the two systems is the TDMA frame structure (EDCT has to use fewer 'slots' in the frame due to a lower bit rate).

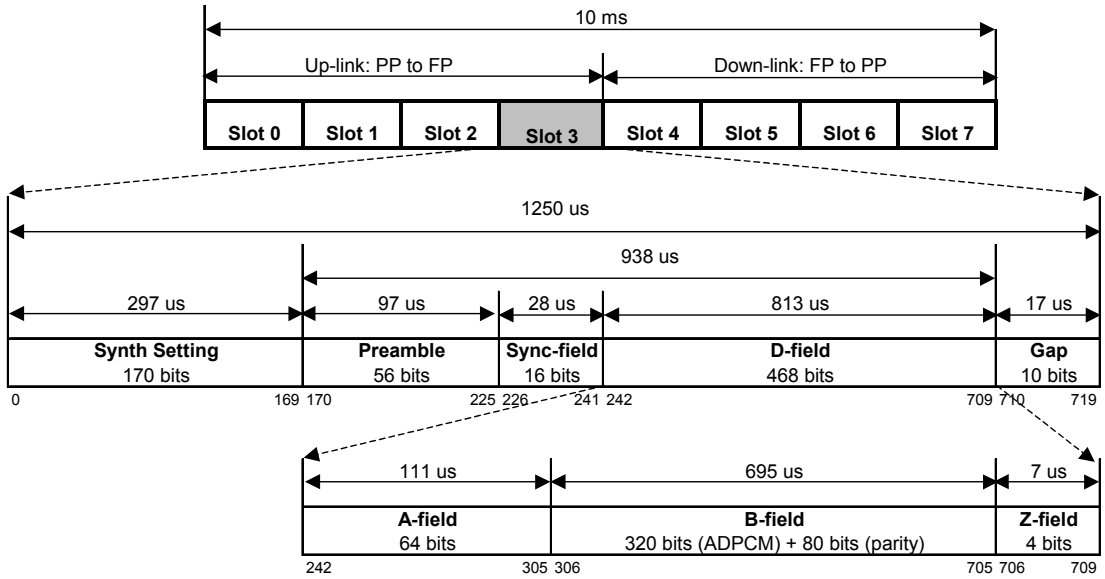
2.1 Frequency channels

EDCT uses carriers whose centre frequencies are shown in "Appendix A – Channel Centre Frequencies".

This gives 87 possible hopping channels, lying between 2401.808203 MHz and 2478.509033 MHz. For the purposes of this document, the channels are numbered 1 … 87.

2.2 TDMA frames structure

The EDCT TDMA frame structure is shown below:



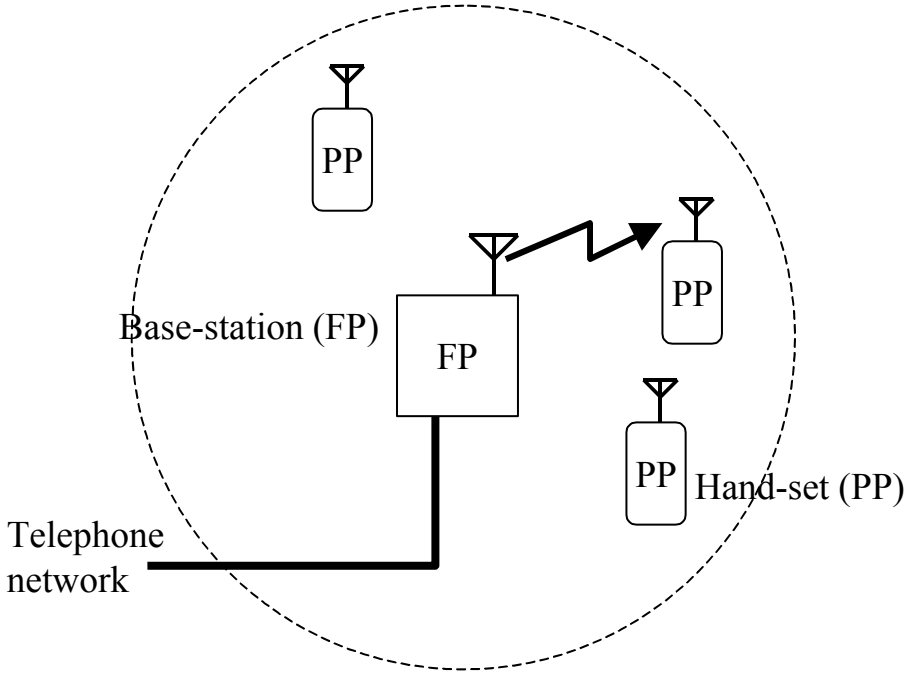
The basic, repeating, frame structure is 10 ms long. It is sub-divided into 8 slots, each 1250 µs long. The active transmission time is 937.5 µs. The first 4 slots form the 'up-link', when the PPs transmit to the FP. The last 4 slots form the 'down-link', when the FP transmits to the PPs.

EDCT uses TDD to carry a two-way voice communication. This is always by using slot-pairs: 0 and 4, 1 and 5, 2 and 6, 3 and 7. In this way the down-link transmission of the duplex communication is always 5ms after the corresponding up-link transmission.

There is only one transceiver in FP or PP therefore in any single slot, the FP or PP can only ever be receiving or transmitting.

2.3 Residential / domestic system

A residential or domestic system is for use in the home. A single FP is used with multiple PPs. There can be any number of PPs, although only 4 simultaneous duplex connections to the FP are allowed; this limit is due to the number of slot-pairs in the TDMA frame structure. The figure illustrates the basic system configuration.



2.4 Bearers

An important concept in DECT and EDCT is the notion of a “bearer”. A bearer is the medium used for carrying a communication.

In a DECT system a bearer is defined by a combination of channel number and slot number. However, because EDCT is a frequency hopping system, a bearer is defined by a hopping sequence and slot number.

There are two types of bearer in the EDCT system:

Dummy bearer

- This is used to carry a ‘beacon’ and other broadcast information.
- The FP will broadcast a dummy bearer all the time it is powered up and operating.
- Only the FP transmits a dummy bearer.
- As it is a simplex transmission, only a down-link slot is used.
- The broadcast information is contained in the ‘A-field’ section of the transmission (the ‘B-field’ section is not required, and is therefore not transmitted).

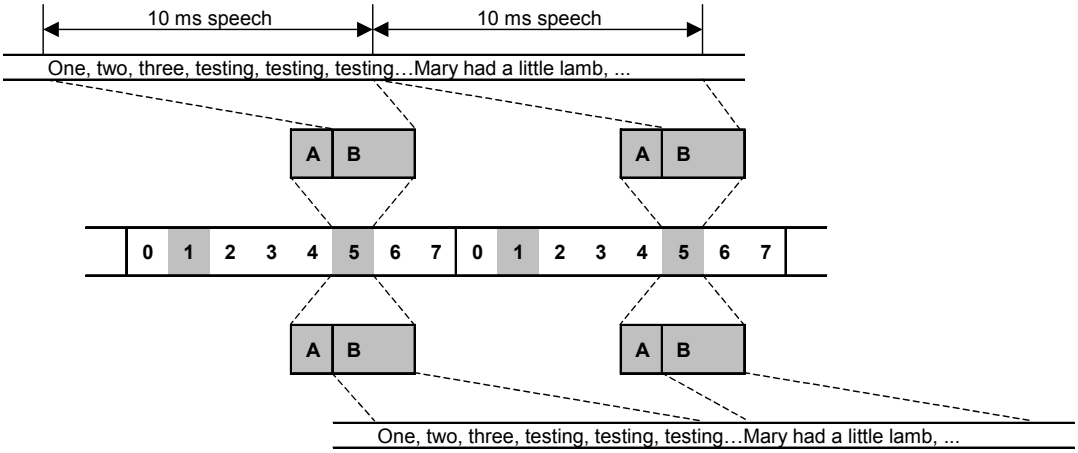
Traffic bearer

- This is used to carry a voice call.
- As it is a duplex transmission both a down-link and up-link slot are used. The slots used are always a slot-pair.
- The ‘A-field’ section contains the same information as the dummy bearer, with the addition of extra signalling required for the call. The voice data is contained in the ‘B-field’ section.

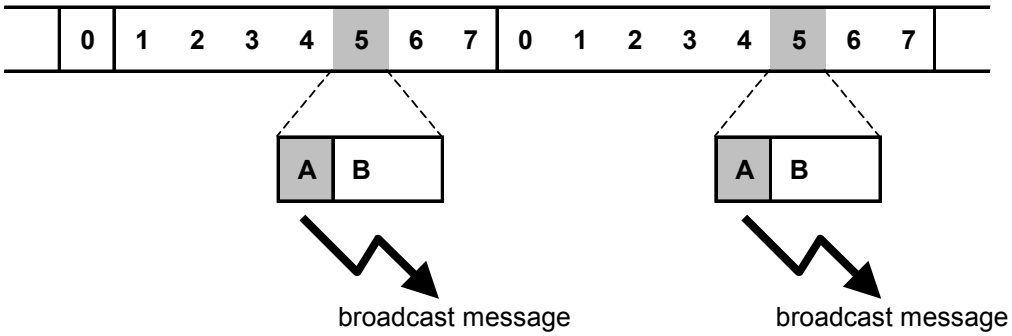
In EDCT the dummy bearer is usually separate to the traffic bearers, i.e. they are on different slots. In the case that 4 traffic bearers are required (the maximum number that can be supported by the FP) then one of the traffic bearers will also take over the responsibilities of the dummy bearer. In the remainder of the document this shall be referred to as a ‘combined dummy/traffic bearer’.

Since the traffic bearer is already carrying the same information as the dummy bearer, the 'combined dummy/traffic bearer' is the same length as a normal traffic bearer. However, the combined dummy/traffic bearer has some restrictions (compared to a normal traffic bearer) with regards to frequency hopping as detailed later.

The following diagram shows the down-link transmission of a traffic bearer; the up-link transmission is in slot 1.



The following diagram shows a dummy bearer transmission. Note, that it uses only a down-link slot and the A-field of the packet.



3 OVERVIEW OF FREQUENCY HOPPING ALGORITHM

3.1 Hopping rate

Each bearer will change frequency channel, or hop, once per frame, i.e. the bearer hopping rate is 100 hops/second.

In the case of a traffic bearer this means that in a particular frame, both the down-link and up-link slots will use the same frequency channel.

With 4 active traffic bearers, each hopping at 100 hops/sec, there will be 800 frequency changes/second. However, because down-link and up-link use the same channel, this is only actually 400 channels/second.

3.2 Hopping Sequence

There are two methods employed for generating the hopping sequences: tables and random number generators (RNGs). Tables are hand-crafted to have specific properties and reverse table-lookup can be used to deduce the position in the table. RNGs generate very long period sequences which are less prone to 'sequence collision'. Both methods are employed in the EDCT system.

3.2.1 Hopping pattern base-table

A dummy bearer or combined dummy/traffic bearer uses a table-generated hop sequence.

A single base-table is constructed containing a permutation of the channel numbers 0, 1, 2,…,74 (there are no repeats in the sequence). An extract is shown in the following table where 'i' is the index, and 'F_0' is the base-table sequence.

i	$F_0(i)$
0	0
1	27
2	38
3	14
…	…
74	44

(This is only an extract; the full base table is shown in "Appendix B – Base-Table Hopping Sequence").

From this one base-table, additional sequences are generated using the formula:

$$F_x(i) = (F_0 (i) + x) \bmod 75$$

The sequence index 'i' in the above formula is incremented, modulo 75, each frame. The value 'x' is used to select the required pattern. Due to the modulus there are 75 unique patterns permuted from this single base-table.

The following table shows an extract of the patterns.

i	$F_0(i)$	$F_1(i)$	$F_2(i)$	$F_3(i)$	…	$F_{74}(i)$
0	0	1	2	3	…	74
1	27	28	29	30	…	26
2	38	39	40	41	…	37
3	14	15	16	17	…	13
…	…	…	…	…	…	…
8	73	74	0	1	…	72
…	…	…	…	…	…	…
74	44	45	46	47	…	43

The base-table is hand-crafted to meet the following criteria:

- Pseudo-random.
- When any pattern is time-shifted with respect to any other pattern, the number of direct and adjacent channel collisions is minimised. In this context, because of the expected RF performance, adjacent should be taken to mean within 3 channels or less.
- When any pattern is time-shifted with respect to any other pattern, the number of direct or adjacent channel collisions on consecutive hops is minimised. Collisions are minimised for 2, 3 and 4 (or more) consecutive hops.
- Successive channels in the sequence are separated sufficiently to avoid microwave oven interference. In this context, a minimum channel separation of 6 or 8 MHz should be considered sufficient.

3.2.2 LCG random number generator

Traffic bearers use a pseudo-random number generated hop sequence. The random number generator (RNG) is a Linear Congruential Generator (LCG). The general form of an LCG is:

$$R_{n+1} = (a \times R_n + c) \mod m$$

A channel number in the range 0…74 is obtained by applying:

Channel number = $(75 \times R_n) / m$

In the above formula integer division is used. A particular LCG is denoted by LCG(m, a, c, R_0). The proposed RNG for EDCT is LCG(3000, $(2\times3\times4\times5\times7+1) = 841$, 787, R_0):

The modulus (m) is less than 2^{16} so that the 'state' can be stored in a single word (16 bits).

This is a full period generator, with a period of 3000, equivalent to 30 seconds and is also a multiple of 75. As such, all channels are used equally and all channels are used equally over a 30 second period.

The full 3000-long sequence is shown in "Appendix C – LCG Random Hopping Sequence".

3.2.3 Logical and physical channel numbers

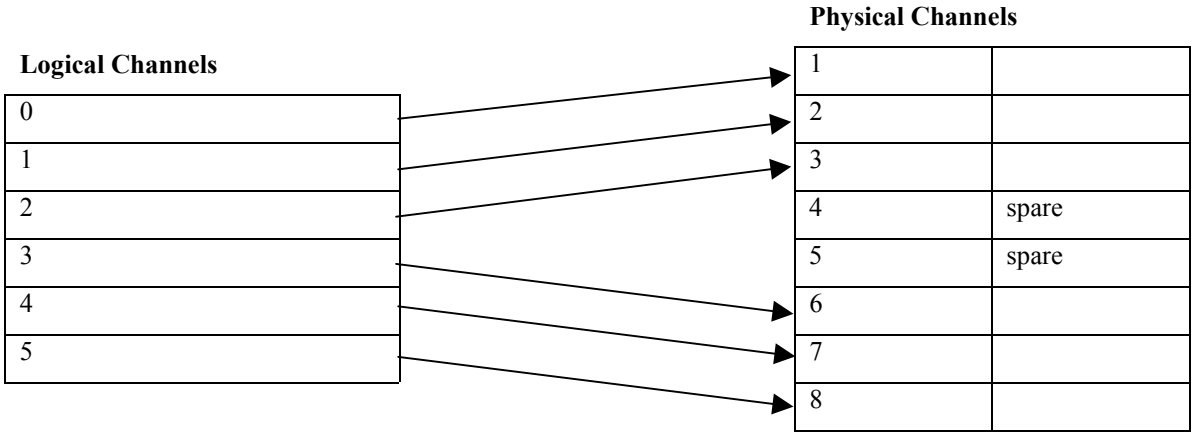
The techniques described so far generate channel numbers in the range 0…74. The EDCT system can use a total of 87 hopping channels (numbered from 1… 87). This results in 12 channels that are not part of the normal sequence and these are reserved as 'spare channels'.

The spare channels are used to adapt the hop sequence, which is a method used by EDCT to avoid noisy frequency channels (see later).

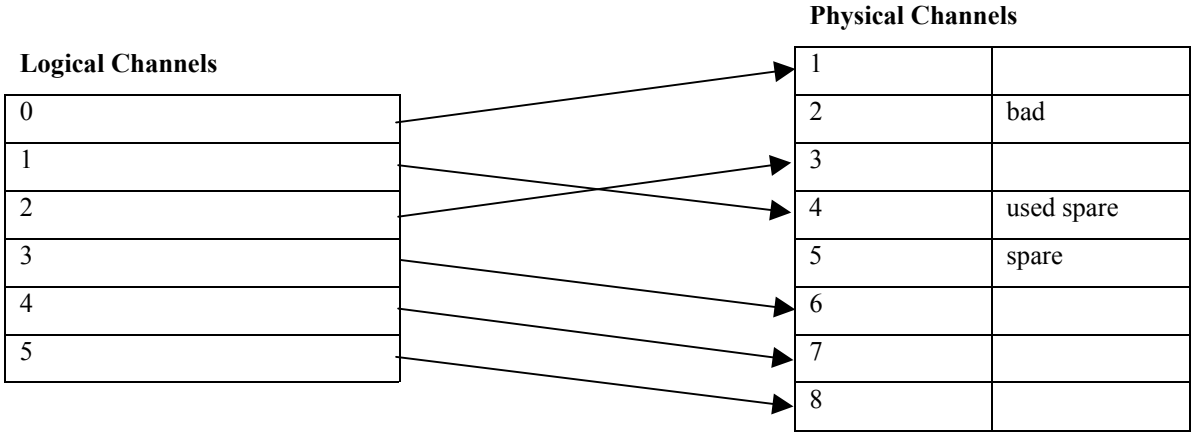
A mapping table is used to convert the 'logical channel number' (in the range 0 … 74) given by the hopping sequence to the 'physical channel number' (in the range 1 … 87) that is actually used.

An important feature of the mapping table is that it is always a one-to-one mapping, i.e. a physical channel is only ever 'mapped-onto' by one logical channel. In this way the channel usage characteristics of the hop sequence are preserved.

For example, consider the following scenario for a small number of logical and physical channels:



Noisy channels can be adapted out of the sequence by 'channel swapping', i.e. swapping a good spare channel for a noisy channel. For example, swapping physical channels 1 and 3 gives:



Obviously, the above mapping table is an example. The actual mapping table is shown in "Appendix D – Logical To Physical Mapping Table". It satisfies the following criteria:

It maps the 75 logical channels onto 87 physical channels, with a one-to-one mapping. This leaves 12 spare channels that are not used in the unadapted hopping sequence.

The spare channels are only positioned around the 2.45 GHz area. The reason for this is that interference from microwave ovens is most likely[1] to be centred on 2.45 GHz.

To facilitate robust 'sequence adaptation' a requirement is that the basic underlying pattern should be changed as little as possible. This is achieved by always ensuring that the channels are swapped back to their original positions when the channel stops being noisy.

3.3 Identifying channel interference

Both the FP and PP can determine channel interference. Interference can be determined by:

- CRC errors on received packets.
- RSSI measurements.

Due to other users of the 2.4 GHz band, the EDCT system has to be tolerant to some interference. EDCT will not be able to avoid the 'random interference' produced by other frequency hopping systems such as Bluetooth or even other EDCT systems. However, it is possible to avoid 'relatively static interference' such as that caused by residential microwave ovens.

In order to distinguish between 'random interference' and 'relatively static interference' it is necessary to detect several successive CRC errors or take several RSSI measurements on a suspect channel. Only then is a channel flagged as being 'bad' – and therefore a candidate for adapting out of the sequence.

3.4 Hop sequence adaption

The hopping sequence will be adapted by channel swapping as described already in section 3.2.3.

In this system, there are only 12 spare channels. Therefore, a maximum of 12 channels can be adapted at any one time.

Only traffic bearers and combined dummy/traffic bearers will have their hop sequence adapted.

The FP decides which channels to swap based on information obtained about channel interference (see section 3.3). The FP will send a message to the PP to indicate the swapped channels. When the PP has acknowledged the message both the FP and the PP will adapt their mapping tables and hence their hopping sequences.

3.5 Starting a dummy bearer

As already mentioned, a FP will broadcast a dummy bearer all the time it is powered up and operating.

When creating a dummy bearer, the FP will select a slot and initial pattern at random.

In addition the FP will select an initial 'hop sequence index' (HSI) at random. The HSI indexes into the base table to select a logical channel. The HSI is incremented (modulo 75) each frame thereafter.

Once the slot, pattern and initial HSI are selected, a sequence of logical channels can be produced at the bearer hopping rate i.e. one hop *per* frame or 100 hops/sec.

The randomising of slot, pattern and HSI helps to spread out the use of hopping sequences amongst different FPs. However, because each FP will select their own slot, pattern and HSI independently there will be the occasional 'sequence collision'.

[1] Actual interference from residential microwave ovens varies greatly with model, loading, environment, time, etc. However, this is a good starting point – the spare channels have to go somewhere!

3.5.1 Avoiding dummy bearer 'sequence collision'

Prior to starting a dummy bearer the FP takes RSSI measurements using the proposed slot and pattern. If these indicate no sequence collision then the dummy bearer is started on the proposed slot and pattern combination. Otherwise, a different slot/pattern pair will be selected, until no sequence collision is detected (or a maximum number of attempts).

Once the dummy bearer has been established, no further action is taken to detect (or correct for) sequence collision on the dummy bearer.

3.6 Gaining sync with a dummy bearer

A PP needs to gain sync with a FP's dummy bearer. This involves:

- Synchronising in time, to align the TDMA frame structure.
- 'Locking-on' to the dummy bearer hopping sequence.

In order to align the TDMA frame structure the PP selects an initial channel to start searching. It then waits on that channel until a valid packet is received; this requires the hard-ware to lock onto the 'sync-field' at the start of the packet, which results in the TDMA frame structure being aligned. If a valid packet is not received in a certain time period then the PP will move to another channel and repeat the process.

The most frequently broadcast message on the dummy bearer is the N_T message. It is transmitted slightly less than every other frame. This message is used to convey the information required for a PP to 'lock-onto' a FP's dummy bearer. However, the PP can only lock-onto a table-generated hopping sequence and so the PP can not use all N_T messages.

When an N_T message is received the PP checks he contents to see if it is from a table-generated hopping sequence. If it is then the PP can determine the dummy bearer pattern and the HSI (see section 3.6.1).

Searching continues, with the PP changing slot and/or channel until it receives an N_T message that it is able to use to 'lock-onto' an FP's dummy bearer.

3.6.1 Determining the pattern and HSI from an N_T message

A dummy bearer hop sequence is table-generated. The sequence is 75 hops long. Knowing only the pattern number, which is encoded in the N_T message, and the channel number that the N_T message was received on, then the HSI can be found directly by reverse table-lookup. Only channels that are in the unadapted sequence are checked, as a PP can not deduce the HSI on an adapted channel.

Once the pattern number and HSI are determined the PP is able to follow the FP's dummy bearer and it is said to be 'locked-onto' the FP.

3.7 Following a dummy bearer

Once the PP has locked-onto a FP's dummy bearer it follows the dummy bearer hop sequence and receives broadcast messages from the FP. During this process it collects system information broadcast by the FP, including the dummy bearer slot number and PSPN (see later).

Any number of PPs can be locked-onto a particular FP's dummy bearer.

A PP can enter into Low Duty Cycle (LDC) mode. In this mode the PP saves battery power by only receiving dummy bearer transmissions every 16 or 64 frames. This is sufficiently frequent for the PP to stay synchronised and to pick up 'paging messages' which contain information on incoming calls (and other system status information).

3.8 Starting a traffic bearer

In DECT and EDCT it is the PP that initiates the establishment of a traffic bearer. The PP does this by transmitting an ACCESS_REQUEST message to the FP. The FP constantly listens for ACCESS_REQUEST messages from PPs on all idle up-link slots, i.e., up-link slots that are not already being used for other traffic bearers.

Successive attempts to establish a traffic bearer use different patterns. This is achieved by the use of the Primary Scan Pattern Number (PSPN). The PSPN determines which pattern is used for a traffic bearer started in the current frame. The FP listens for ACCESS_REQUESTs on the channel determined by the PSPN pattern and its HSI.

The PSPN is incremented (modulo 75) in each frame whilst the FP is powered up and operating.

The PSPN is known to the PP because it is periodically transmitted on the dummy bearer. Thus once a system's PSPN is known and a FP's HSI is determined, the PP can determine what channel the FP will be listening to during its idle up-link slots.

The PP will select a pattern and slot to use and when the PSPN indicates the selected pattern, the ACCESS_REQUEST is transmitted on the appropriate channel and slot. To avoid a long latency whilst the selected pattern 'comes around' on the PSPN, the PP selects a pattern that will occur in N frames time. Where N is both small and determined randomly so as to avoid multiple PPs continually colliding whilst trying to establish traffic bearers.

The ACCESS_REQUEST message contains the identity of the FP to indicate which FP the message is directed at. The requested FP must respond in the next half-frame either with a WAIT or with a BEARER_CONFIRM or with a RELEASE.

(This system may seem obscure, but it is a direct consequence of the DECT protocol from which the EDCT protocol was derived.)

In EDCT there are two possible modes of operation:

- The selected pattern is only used for the very first frame. After which both the FP and PP will have synchronised their RNG with the same 'seed' and the random sequence is started and used for the next frame's channel.
- The FP and PP never switch to using a RNG generated hop sequence and instead continue to use the selected table-based pattern.

Traffic bearers normally use a RNG generated hop sequence.

3.8.1 Avoiding traffic bearer 'sequence collision'

Due to the longer period of a RNG-generated hop sequence, the probability of 'sequence collision' on a traffic bearer is much lower than on a table-generated sequence.

Prior to starting a traffic bearer RSSI measurements are taken using the proposed slot and pattern. If these indicate no sequence collision then the traffic bearer is started on the proposed slot and pattern combination. No further action is taken to detect (or correct for) sequence collision.

3.9 Starting a combined dummy/traffic bearer

The PP may require to establish a traffic bearer on the slot currently carrying the dummy bearer, usually only when it is the last slot available to it. The PP must use the same pattern that the dummy bearer is currently using.

If the PP has to wait for the dummy bearer pattern to 'come around' on the PSPN this might introduce a long latency. To avoid this, the FP always listens to the channel dictated by the dummy bearer pattern on the slot that is the pair of the dummy bearer transmission.

3.9.1 Avoiding combined dummy/traffic bearer 'sequence collision'

No action is taken to avoid sequence collision.

3.10 Seamless bearer hand-over & "multi-slot mode"

The 2.4 GHz band is prone to interference. In order to improve the robustness of the EDCT system it has the option to operate in a 'multi-slot mode', whereby two traffic bearers are used simultaneously to carry the same voice data. This achieved by operating in a state of permanent 'bearer hand-over'.

To do this the PP establishes a second traffic bearer with the FP, in the manner already described. In doing so, the PP indicates that this bearer is associated with an existing connection, and as a result, the voice data will get routed accordingly. This second traffic bearer uses a different frequency pattern to that of the first traffic bearer.

In a DECT system bearer hand-over normally occurs between a PP and two different FPs and simultaneous traffic bearers are only present for a short period. In EDCT with multi-slot mode enabled the bearer hand-over occurs between a PP and the same FP and the simultaneous traffic bearers are present, in principle, for the duration of the connection.

3.11 Handset-to-handset mode

The EDCT protocol stack supports a 'handset-to-handset' mode in which two handsets can be used to communicate independently of any FP. This is achieved by one of the handsets acting as a FP for the duration of the handset-to-handset call.

All links to the base-station (true FP) are released when a PP is switched to handset-to-handset mode.

The operation of the handset-to-handset mode is as described above for a regular PP / FP system (the part of the FP is effectively played by one of the PPs). The only difference is that a traffic bearer is always started on the dummy bearer slot, i.e. handset-to-handset communications always use a combined dummy/traffic bearer.

3.12 Scanning for noise

The PP will occasionally use spare TDMA slots to take RSSI measurements on frequency channels. These channels are not associated with a specific transmitter and therefore do not follow a specific hopping sequence.

4 CONFORMANCE TO FCC REQUIREMENTS

The following sections show how the EDCT system conforms to the appropriate FCC requirements:

4.1 Section 15.247(a)(1)

The hopping channel carrier frequencies are separated by 891.871 kHz.

Each bearer is independent and hops at a rate of 100 hops/sec.

The hopping sequence is either table generated or RNG generated:

A table-generated hop sequence is 75 hops long, each channel is used exactly once in the sequence. Therefore, in a 30 second period each frequency channel is used exactly 40 times in that sequence.

An RNG-generated hop sequence is 3000 hops long, each channel is used exactly 40 times in the entire sequence. Therefore, in a 30 second period each frequency channel is used exactly 40 times in that sequence.

The hopping sequence contains 75 logical channels these are mapped-onto 75 physical channels using a mapping table (see section 3.2.3 and "Appendix D – Logical To Physical Mapping Table").

The highest channel occupancy occurs when a FP has 4 traffic bearers, i.e. 8 slots utilised, each using the same hopping sequence. As shown previously, for a given sequence, in a 30 second period each frequency channel is used exactly 40 times. The active transmission time in a slot is 937.5µs. Therefore the average time of occupancy on any frequency channel in a 30 second period is:

$T = 937.5\mu s \times 40 \times 8 = 300.0$ ms

As a comparison, the lowest channel occupancy occurs when only a single dummy bearer is being transmitted. Because only the A-field is used on a dummy bearer, the transmission is only 236.1µs long, therefore the average time of occupancy on any frequency channel in a 30 second period is:

$T = 236.1\mu s \times 40 \times 1 = 9.444$ ms

The maximum 20 dB bandwidth of the hopping channel is less than 891.871 kHz.

A packet is sent once *per* frame *per* bearer for the duration of the bearer; packets are not resent.

See section 3.6 for a description of how the receiver gains synchronisation with the transmitter, i.e. a dummy bearer and has a 900kHz bandwidth IF filter matching transmitted signal bandwidth.

4.2 Section 15.247(b)(1)

The maximum peak output power of the intentional radiator is 200mW

4.3 Section 15.247(g)

In the case of the dummy bearer, which the FP transmits all the time it is powered up and operating, the hopping sequence cycles through the 75 hops in the selected hopping pattern and then repeats.

In the case of a traffic bearer presented with continuous data, which is the normal case --- as this is a voice system, the hopping sequence cycles through either 3000 hops before repeating for a RNG based sequence or cycles through 75 hops before repeating for a table-based sequence.

In the case of a traffic bearer transmitting short bursts, for example, which may happen if a PP has several failed attempts[2] to establish a traffic bearer, then successive traffic bearers will start on different patterns because the PSPN is incremented each frame – see section 3.8.

Note that this system is a voice system and short burst transmissions are not typical.

4.4 Section 15.247(h)

There is no coordination between transmitters for the purpose of avoiding the simultaneous occupancy of hopping frequencies by transmitters in multiple EDCT systems.

Communication only ever takes place between one FP and a PP, never between two FPs or two PPs. (In handset-to-handset mode a PP becomes effectively a FP.) It is actually impossible for a FP to receive a FP packet or a PP to receive a PP packet because their respective 'sync-fields' are different.

An FP and a PP that have an active traffic bearer between them share a common hopping sequence and hop sequence adaption information, i.e. swapped channels. However, neither the FP nor the PP transmits this information to a third party, for any purpose whatsoever.

In actual fact, channel collisions between FPs and PPs can and will take place. These may result in reduced voice quality, but this has to be tolerated.

When two transmitters with overlapping radio cells are using the same slot, pattern and phase within the pattern there is sequence collision. This is detected by the occurrence of multiple, consecutive, corrupted packets. If sequence collision happens on a dummy bearer or a combined dummy/traffic bearer then the FP will randomly select a new pattern. If sequence collision happens on a traffic bearer no action is taken.

[2] The protocol actually limits the number of re-tries to 11 before giving up on the connection.

APPENDIX A – CHANNEL CENTRE FREQUENCIES

The following table lists the channel centre frequencies as detailed in section 2.1.

Physical Channel Number	Centre Frequency (MHz)	Physical Channel Number	Centre Frequency (MHz)	Physical Channel Number	Centre Frequency (MHz)
1	2401.808203	31	2428.564307	61	2455.320410
2	2402.698096	32	2429.454199	62	2456.210303
3	2403.591943	33	2430.348047	63	2457.104150
4	2404.481836	34	2431.237939	64	2457.994043
5	2405.375684	35	2432.131787	65	2458.887891
6	2406.265576	36	2433.021680	66	2459.777783
7	2407.159424	37	2433.915527	67	2460.671631
8	2408.050000	38	2434.805420	68	2461.561523
9	2408.943164	39	2435.699268	69	2462.455371
10	2409.833057	40	2436.589160	70	2463.345264
11	2410.726904	41	2437.483008	71	2464.239111
12	2411.616797	42	2438.372900	72	2465.129004
13	2412.510645	43	2439.266748	73	2466.022852
14	2413.400537	44	2440.156641	74	2466.912744
15	2414.294385	45	2441.050488	75	2467.806592
16	2415.184277	46	2441.940381	76	2468.696484
17	2416.078125	47	2442.834229	77	2469.590332
18	2416.968018	48	2443.724121	78	2470.480225
19	2417.861865	49	2444.617969	79	2471.374072
20	2418.751758	50	2445.507861	80	2472.263965
21	2419.645605	51	2446.401709	81	2473.157813
22	2420.535498	52	2447.291602	82	2474.047705
23	2421.429346	53	2448.185449	83	2474.941553
24	2422.319238	54	2449.075342	84	2475.831445
25	2423.213086	55	2449.969189	85	2476.725293
26	2424.102979	56	2450.859082	86	2477.615186
27	2424.996826	57	2451.752930	87	2478.509033
28	2425.886719	58	2452.642822		
29	2426.780566	59	2453.536670		
30	2427.670459	60	2454.426563		

APPENDIX B – BASE-TABLE HOPPING SEQUENCE

The following table, arranged as an 8 × 10 grid, is the base table for the hopping sequence as detailed in section 3.2.1. The sequence is 75 hops long.

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	0	27	38	14	26	49	13	33	73	55
10	16	1	11	54	8	64	2	48	28	61
20	4	40	65	6	23	67	57	42	12	29
30	62	36	47	5	71	43	32	56	21	59
40	39	15	53	18	45	37	74	63	46	3
50	51	31	72	58	9	70	35	69	25	34
60	50	60	68	22	52	24	41	7	17	30
70	19	10	20	66	44					

APPENDIX C – LCG RANDOM HOPPING SEQUENCE

The following table, is the random channel sequence produced by the LCG random number generator as detailed in section 3.2.2. The sequence is 3000 hops long.

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	0	19	66	20	60	68	73	29	43	69
10	61	51	68	66	2	55	29	31	15	10
20	48	8	69	38	19	41	61	33	61	27
30	35	39	71	10	35	28	18	34	33	44
40	22	71	73	57	52	15	50	36	5	61
50	8	28	0	28	69	2	6	38	52	2
60	70	60	1	0	11	63	38	40	23	19
70	57	16	3	47	27	50	70	41	70	36
80	44	48	5	19	44	37	27	43	42	53
90	30	5	7	65	61	24	58	45	14	69
100	17	37	8	37	3	10	15	47	60	11
110	4	68	10	9	19	72	47	48	32	28
120	66	25	12	56	36	59	4	50	4	45
130	52	57	14	27	53	46	35	52	51	61
140	39	14	15	74	70	32	67	54	22	3
150	26	45	17	46	11	19	24	55	69	20
160	13	2	19	18	28	6	56	57	41	37
170	74	34	21	64	45	68	12	59	13	53
180	61	66	22	36	62	54	44	61	59	70
190	48	22	24	8	3	41	1	62	31	12
200	35	54	26	55	20	28	33	64	3	29
210	21	11	28	26	37	15	64	66	50	45
220	8	43	29	73	54	1	21	68	21	62
230	70	74	31	45	70	63	53	69	68	4
240	57	31	33	17	12	50	10	71	40	21
250	43	63	35	63	29	37	41	73	12	37
260	30	20	36	35	46	23	73	0	58	54
270	17	51	38	7	62	10	30	1	30	71
280	4	8	40	54	4	72	62	3	2	13
290	65	40	42	25	21	59	18	5	49	29

300	52	72	43	72	38	45	50	7	20	46
310	39	28	45	44	54	32	7	8	67	63
320	26	60	47	16	71	19	39	10	39	5
330	12	17	49	62	13	6	70	12	11	21
340	74	49	50	34	30	67	27	14	57	38
350	61	5	52	6	46	54	59	15	29	55
360	48	37	54	53	63	41	16	17	1	72
370	34	69	56	24	5	28	47	19	48	13
380	21	26	57	71	22	14	4	21	19	30
390	8	57	59	43	38	1	36	22	66	47
400	70	14	61	15	55	63	68	24	38	64
410	56	46	63	61	72	50	24	26	10	5
420	43	3	64	33	14	36	56	28	56	22
430	30	34	66	5	30	23	13	29	28	39
440	17	66	68	52	47	10	45	31	0	56
450	3	23	70	23	64	72	1	33	47	72
460	65	55	71	70	6	58	33	35	18	14
470	52	11	73	42	22	45	65	36	65	31
480	39	43	0	14	39	32	22	38	37	48
490	25	0	2	60	56	19	53	40	9	64
500	12	32	3	32	73	5	10	42	55	6
510	74	63	5	4	14	67	42	43	27	23
520	61	20	7	51	31	54	74	45	74	40
530	47	52	9	22	48	41	30	47	46	56
540	34	9	10	69	65	27	62	49	17	73
550	21	40	12	41	6	14	19	50	64	15
560	8	72	14	13	23	1	51	52	36	32
570	69	29	16	59	40	63	7	54	8	48
580	56	61	17	31	57	49	39	56	54	65
590	43	17	19	3	73	36	71	57	26	7
600	30	49	21	50	15	23	28	59	73	24
610	16	6	23	21	32	10	59	61	45	40
620	3	38	24	68	49	71	16	63	16	57
630	65	69	26	40	65	58	48	64	63	74
640	52	26	28	12	7	45	5	66	35	16

650	38	58	30	58	24	32	36	68	7	32
660	25	15	31	30	41	18	68	70	53	49
670	12	46	33	2	57	5	25	71	25	66
680	74	3	35	49	74	67	57	73	72	8
690	60	35	37	20	16	54	13	0	44	24
700	47	67	38	67	33	40	45	2	15	41
710	34	23	40	39	49	27	2	3	62	58
720	21	55	42	11	66	14	34	5	34	0
730	7	12	44	57	8	1	65	7	6	16
740	69	44	45	29	25	62	22	9	52	33
750	56	0	47	1	41	49	54	10	24	50
760	43	32	49	48	58	36	11	12	71	67
770	29	64	51	19	0	23	42	14	43	8
780	16	21	52	66	17	9	74	16	14	25
790	3	52	54	38	33	71	31	17	61	42
800	65	9	56	10	50	58	63	19	33	59
810	51	41	58	56	67	45	19	21	5	0
820	38	73	59	28	9	31	51	23	51	17
830	25	29	61	0	25	18	8	24	23	34
840	12	61	63	47	42	5	40	26	70	51
850	73	18	65	18	59	67	71	28	42	67
860	60	50	66	65	1	53	28	30	13	9
870	47	6	68	37	17	40	60	31	60	26
880	34	38	70	9	34	27	17	33	32	43
890	20	70	72	55	51	14	48	35	4	59
900	7	27	73	27	68	0	5	37	50	1
910	69	58	0	74	9	62	37	38	22	18
920	56	15	2	46	26	49	69	40	69	35
930	42	47	4	17	43	36	25	42	41	51
940	29	4	5	64	60	22	57	44	12	68
950	16	35	7	36	1	9	14	45	59	10
960	3	67	9	8	18	71	46	47	31	27
970	64	24	11	54	35	58	2	49	3	43
980	51	56	12	26	52	44	34	51	49	60
990	38	12	14	73	68	31	66	52	21	2

1000	25	44	16	45	10	18	23	54	68	19
1010	11	1	18	16	27	5	54	56	40	35
1020	73	33	19	63	44	66	11	58	11	52
1030	60	64	21	35	60	53	43	59	58	69
1040	47	21	23	7	2	40	0	61	30	11
1050	33	53	25	53	19	27	31	63	2	27
1060	20	10	26	25	36	13	63	65	48	44
1070	7	41	28	72	52	0	20	66	20	61
1080	69	73	30	44	69	62	52	68	67	3
1090	55	30	32	15	11	49	8	70	39	19
1100	42	62	33	62	28	35	40	72	10	36
1110	29	18	35	34	44	22	72	73	57	53
1120	16	50	37	6	61	9	29	0	29	70
1130	2	7	39	52	3	71	60	2	1	11
1140	64	39	40	24	20	57	17	4	47	28
1150	51	70	42	71	36	44	49	5	19	45
1160	38	27	44	43	53	31	6	7	66	62
1170	24	59	46	14	70	18	37	9	38	3
1180	11	16	47	61	12	4	69	11	9	20
1190	73	47	49	33	28	66	26	12	56	37
1200	60	4	51	5	45	53	58	14	28	54
1210	46	36	53	51	62	40	14	16	0	70
1220	33	68	54	23	4	26	46	18	46	12
1230	20	24	56	70	20	13	3	19	18	29
1240	7	56	58	42	37	0	35	21	65	46
1250	68	13	60	13	54	62	66	23	37	62
1260	55	45	61	60	71	48	23	25	8	4
1270	42	1	63	32	12	35	55	26	55	21
1280	29	33	65	4	29	22	12	28	27	38
1290	15	65	67	50	46	9	43	30	74	54
1300	2	22	68	22	63	70	0	32	45	71
1310	64	53	70	69	4	57	32	33	17	13
1320	51	10	72	41	21	44	64	35	64	30
1330	37	42	74	12	38	31	20	37	36	46
1340	24	74	0	59	55	17	52	39	7	63

1350	11	30	2	31	71	4	9	40	54	5
1360	73	62	4	3	13	66	41	42	26	22
1370	59	19	6	49	30	53	72	44	73	38
1380	46	51	7	21	47	39	29	46	44	55
1390	33	7	9	68	63	26	61	47	16	72
1400	20	39	11	40	5	13	18	49	63	14
1410	6	71	13	11	22	0	49	51	35	30
1420	68	28	14	58	39	61	6	53	6	47
1430	55	59	16	30	55	48	38	54	53	64
1440	42	16	18	2	72	35	70	56	25	6
1450	28	48	20	48	14	22	26	58	72	22
1460	15	5	21	20	31	8	58	60	43	39
1470	2	36	23	67	47	70	15	61	15	56
1480	64	68	25	39	64	57	47	63	62	73
1490	50	25	27	10	6	44	3	65	34	14
1500	37	57	28	57	23	30	35	67	5	31
1510	24	13	30	29	39	17	67	68	52	48
1520	11	45	32	1	56	4	24	70	24	65
1530	72	2	34	47	73	66	55	72	71	6
1540	59	34	35	19	15	52	12	74	42	23
1550	46	65	37	66	31	39	44	0	14	40
1560	33	22	39	38	48	26	1	2	61	57
1570	19	54	41	9	65	13	32	4	33	73
1580	6	11	42	56	7	74	64	6	4	15
1590	68	42	44	28	23	61	21	7	51	32
1600	55	74	46	0	40	48	53	9	23	49
1610	41	31	48	46	57	35	9	11	70	65
1620	28	63	49	18	74	21	41	13	41	7
1630	15	19	51	65	15	8	73	14	13	24
1640	2	51	53	37	32	70	30	16	60	41
1650	63	8	55	8	49	57	61	18	32	57
1660	50	40	56	55	66	43	18	20	3	74
1670	37	71	58	27	7	30	50	21	50	16
1680	24	28	60	74	24	17	7	23	22	33
1690	10	60	62	45	41	4	38	25	69	49

1700	72	17	63	17	58	65	70	27	40	66
1710	59	48	65	64	74	52	27	28	12	8
1720	46	5	67	36	16	39	59	30	59	25
1730	32	37	69	7	33	26	15	32	31	41
1740	19	69	70	54	50	12	47	34	2	58
1750	6	25	72	26	66	74	4	35	49	0
1760	68	57	74	73	8	61	36	37	21	17
1770	54	14	1	44	25	48	67	39	68	33
1780	41	46	2	16	42	34	24	41	39	50
1790	28	2	4	63	58	21	56	42	11	67
1800	15	34	6	35	0	8	13	44	58	9
1810	1	66	8	6	17	70	44	46	30	25
1820	63	23	9	53	34	56	1	48	1	42
1830	50	54	11	25	50	43	33	49	48	59
1840	37	11	13	72	67	30	65	51	20	1
1850	23	43	15	43	9	17	21	53	67	17
1860	10	0	16	15	26	3	53	55	38	34
1870	72	31	18	62	42	65	10	56	10	51
1880	59	63	20	34	59	52	42	58	57	68
1890	45	20	22	5	1	39	73	60	29	9
1900	32	52	23	52	18	25	30	62	0	26
1910	19	8	25	24	34	12	62	63	47	43
1920	6	40	27	71	51	74	19	65	19	60
1930	67	72	29	42	68	61	50	67	66	1
1940	54	29	30	14	10	47	7	69	37	18
1950	41	60	32	61	26	34	39	70	9	35
1960	28	17	34	33	43	21	71	72	56	52
1970	14	49	36	4	60	8	27	74	28	68
1980	1	6	37	51	2	69	59	1	74	10
1990	63	37	39	23	18	56	16	2	46	27
2000	50	69	41	70	35	43	48	4	18	44
2010	36	26	43	41	52	30	4	6	65	60
2020	23	58	44	13	69	16	36	8	36	2
2030	10	14	46	60	10	3	68	9	8	19
2040	72	46	48	32	27	65	25	11	55	36

2050	58	3	50	3	44	52	56	13	27	52
2060	45	35	51	50	61	38	13	15	73	69
2070	32	66	53	22	2	25	45	16	45	11
2080	19	23	55	69	19	12	2	18	17	28
2090	5	55	57	40	36	74	33	20	64	44
2100	67	12	58	12	53	60	65	22	35	61
2110	54	43	60	59	69	47	22	23	7	3
2120	41	0	62	31	11	34	54	25	54	20
2130	27	32	64	2	28	21	10	27	26	36
2140	14	64	65	49	45	7	42	29	72	53
2150	1	20	67	21	61	69	74	30	44	70
2160	63	52	69	68	3	56	31	32	16	12
2170	49	9	71	39	20	43	62	34	63	28
2180	36	41	72	11	37	29	19	36	34	45
2190	23	72	74	58	53	16	51	37	6	62
2200	10	29	1	30	70	3	8	39	53	4
2210	71	61	3	1	12	65	39	41	25	20
2220	58	18	4	48	29	51	71	43	71	37
2230	45	49	6	20	45	38	28	44	43	54
2240	32	6	8	67	62	25	60	46	15	71
2250	18	38	10	38	4	12	16	48	62	12
2260	5	70	11	10	21	73	48	50	33	29
2270	67	26	13	57	37	60	5	51	5	46
2280	54	58	15	29	54	47	37	53	52	63
2290	40	15	17	0	71	34	68	55	24	4
2300	27	47	18	47	13	20	25	57	70	21
2310	14	3	20	19	29	7	57	58	42	38
2320	1	35	22	66	46	69	14	60	14	55
2330	62	67	24	37	63	56	45	62	61	71
2340	49	24	25	9	5	42	2	64	32	13
2350	36	55	27	56	21	29	34	65	4	30
2360	23	12	29	28	38	16	66	67	51	47
2370	9	44	31	74	55	3	22	69	23	63
2380	71	1	32	46	72	64	54	71	69	5
2390	58	32	34	18	13	51	11	72	41	22

2400	45	64	36	65	30	38	43	74	13	39
2410	31	21	38	36	47	25	74	1	60	55
2420	18	53	39	8	64	11	31	3	31	72
2430	5	9	41	55	5	73	63	4	3	14
2440	67	41	43	27	22	60	20	6	50	31
2450	53	73	45	73	39	47	51	8	22	47
2460	40	30	46	45	56	33	8	10	68	64
2470	27	61	48	17	72	20	40	11	40	6
2480	14	18	50	64	14	7	72	13	12	23
2490	0	50	52	35	31	69	28	15	59	39
2500	62	7	53	7	48	55	60	17	30	56
2510	49	38	55	54	64	42	17	18	2	73
2520	36	70	57	26	6	29	49	20	49	15
2530	22	27	59	72	23	16	5	22	21	31
2540	9	59	60	44	40	2	37	24	67	48
2550	71	15	62	16	56	64	69	25	39	65
2560	58	47	64	63	73	51	26	27	11	7
2570	44	4	66	34	15	38	57	29	58	23
2580	31	36	67	6	32	24	14	31	29	40
2590	18	67	69	53	48	11	46	32	1	57
2600	5	24	71	25	65	73	3	34	48	74
2610	66	56	73	71	7	60	34	36	20	15
2620	53	13	74	43	24	46	66	38	66	32
2630	40	44	1	15	40	33	23	39	38	49
2640	27	1	3	62	57	20	55	41	10	66
2650	13	33	5	33	74	7	11	43	57	7
2660	0	65	6	5	16	68	43	45	28	24
2670	62	21	8	52	32	55	0	46	0	41
2680	49	53	10	24	49	42	32	48	47	58
2690	35	10	12	70	66	29	63	50	19	74
2700	22	42	13	42	8	15	20	52	65	16
2710	9	73	15	14	24	2	52	53	37	33
2720	71	30	17	61	41	64	9	55	9	50
2730	57	62	19	32	58	51	40	57	56	66
2740	44	19	20	4	0	37	72	59	27	8

2750	31	50	22	51	16	24	29	60	74	25
2760	18	7	24	23	33	11	61	62	46	42
2770	4	39	26	69	50	73	17	64	18	58
2780	66	71	27	41	67	59	49	66	64	0
2790	53	27	29	13	8	46	6	67	36	17
2800	40	59	31	60	25	33	38	69	8	34
2810	26	16	33	31	42	20	69	71	55	50
2820	13	48	34	3	59	6	26	73	26	67
2830	0	4	36	50	0	68	58	74	73	9
2840	62	36	38	22	17	55	15	1	45	26
2850	48	68	40	68	34	42	46	3	17	42
2860	35	25	41	40	51	28	3	5	63	59
2870	22	56	43	12	67	15	35	6	35	1
2880	9	13	45	59	9	2	67	8	7	18
2890	70	45	47	30	26	64	23	10	54	34
2900	57	2	48	2	43	50	55	12	25	51
2910	44	33	50	49	59	37	12	13	72	68
2920	31	65	52	21	1	24	44	15	44	10
2930	17	22	54	67	18	11	0	17	16	26
2940	4	54	55	39	35	72	32	19	62	43
2950	66	10	57	11	51	59	64	20	34	60
2960	53	42	59	58	68	46	21	22	6	2
2970	39	74	61	29	10	33	52	24	53	18
2980	26	31	62	1	27	19	9	26	24	35
2990	13	62	64	48	43	6	41	27	71	52

APPENDIX D – LOGICAL TO PHYSICAL MAPPING TABLE

The following table, is the logical to physical mapping table, as detailed in section 3.2.3.

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	1	2	3	4	5	6	7	8	9	10
10	11	12	13	14	15	16	17	18	19	20
20	21	22	23	24	25	26	27	28	29	30
30	31	32	33	34	35	36	37	38	39	40
40	41	42	43	44	45	46	47	48	49	50
50	51	52	53	54	55	56	57	58	72	73
60	74	75	76	77	78	79	80	81	82	83
70	84	85	86	87						

PRELIMINARY

DH24RF17B

Digital FHSS RFIC for 2.4GHz ISM Band supporting Multi-Handset Applications

DISTINCTIVE CHARACTERISTICS:

- 0.25μ CMOS Technology
- Integrated Rx Channel Filters
- FM Discriminator and Data Slicer
- Integrated PLL Synthesizer, including VCO and PLL Loop Filter
- +20 dBm Tx Output Power
- On-Board "Trimmable" XTAL Oscillator
- EDCT Protocol is DSPG Proprietary

GENERAL DESCRIPTION

The DH24RF17B Digital FHSS RFIC for 2.4GHz ISM Band supporting Multi-Handset Applications is a member of DSPG's EDCT™ family, which also contains the DLH36K Baseband Processor. This two-chip solution provides a complete solution for a 2.4 GHz cordless telephone chip set. The DH24RF17B is a CMOS Radio Frequency Integrated Circuit (RFIC) that incorporates all of the transmit and receive functions required for a Frequency Hopping Spread Spectrum (FHSS) Digital Cordless transceiver architecture, operating in the 2.4–2.5 GHz Industrial, Scientific, and Medical (ISM) band. The FHSS protocol used by the system utilizes Time Division Duplexing (TDD), in which the transceiver alternately transmits and receives in a burst-like nature.

The receive path uses a single-conversion architecture which image-reject mixes the 2-level FSK-modulated receive signal to a low IF frequency of 2 MHz. Integrated bandpass filters provide rejection of unwanted signals. The IF signal is amplified and limited prior to demodulation by an integrated FM discriminator that requires no external components or adjustment. The resulting demodulated audio signal is then filtered, sliced, and output to the baseband chip for further processing.

Because the transmitter and receiver are never on at the same time, it is possible to use a single local oscillator (LO) for both transmit and receive modes. This is done by quickly shifting the LO frequency in the gap time between the transmit and receive bursts. The LO is generated by an integrated VCO and Δ-Σ Fractional-N PLL synthesizer. The transmit FSK data is shaped by a Gaussian low-pass filter and modulated directly into the Δ-Σ data stream. The transmit path contains an integrated power amplifier capable of delivering +20 dBm in CW mode. The power amplifier is adjustable in output level to minimize current consumption under strong signal conditions. Ramping of the rising and falling edges of the burst signal prevents unwanted spectral splatter.

The TDD architecture of the system makes it possible to integrate both transmit and receive functions in a single chip. The chip is well suited for building digital communication links when used with baseband integrated circuits such as the DLH36K from DSPG.

Pub: US2.4GFHSS Rev: 1 Amendment: /3
Issue Date: **December 2002**

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REVISION LOG

Table 1. Revision Log

Revision	Date	Description
1.0	July 2002	Original Release. Summary of changes from DH24RF17A Rev 1.5: Increased **P.A. Output Power** to +20 dBm nominal, +18.5 dBm minimum. Modified **RX Gain Step** to 30 dB. Modified **RX BER Sensitivity** in LOW_GAIN mode to –75 dBm. Modified **IIP3** in LOW_GAIN mode to –17 dBm. Deleted **Signal-to-Noise-Ratio** spec. All Production Testing directly screens for BER performance. Deleted **PA_RAMP** pin 26. All P.A. ramp control is now done internally to the chip. Modified how the **RX Input Level Range** is specified, separating out the end-of-range sensitivity spec from the strong signal "zero BER" spec. Modified **TX Mode currents** to reflect increased output power level.
1.1	October 2002	Modified **RSTN-to-CAL Power-On Time** from 500 µsec to 350 µsec. Clarified that the **RSTN** pin may be held low during power-up, in addition to simply pulsing RSTN low after power-up. Clarified that the **transmit deviation** is not a function of the amplitude of the **TXMOD** signal; the deviation is set internal to the RFIC. Clarified that the static logic level applied to the TXMOD input pin affects the observed "unmodulated" carrier frequency. Modified the **Functional Description** of the **IF Channel Selection Bandpass Filter** to adjust the counter values used during the **CAL algorithm**. Clarified that a negative **AFC LO Offset** results in an increase in IF frequency due to use of a low-side injection scheme. Clarified that the **FM discriminator lowpass data filter** and the **PLL loop filter** "borrow" and use the calibration result from the BPF CAL algorithm. Fixed an error in the **EDCT Protocol** section that mistakenly referred to the nominal deviation of the system as ±60 kHz. Modified Figure 7 **Crystal Oscillator Block Diagram** to more accurately reflect the circuit architecture. Corrected Table 7 **STANDBY, IDLE & ACTIVE Modes** to show that the **IDLE** mode is Not Applicable when the BBIC generates the system clock, and that the **OSCOFF** bit should be LOW in ACTIVE mode. Modified Table 2 **Pin Descriptions** and Functional Description to clarify the recommended drive conditions for the **XIN** pin. Modified Table 10 **Synthesizer AC Electrical Characteristics** to spec a 700 mVpp minimum drive level for the **External Oscillator Input Level**. Modified all **Electrical Characteristics** table to specify testing at this 700 mVpp minimum drive level. Deleted **Synthesizer TX Pulling** spec. Modified Table 11 **Receiver AC Electrical Characteristics** to change **RX Gain Step** back to 22 dB, **IIP3** in LOW_GAIN mode back to –23 dBm, and **RX Sensitivity** in LOW_GAIN mode back to –79 dBm. Corrected references to RX gain control by the (non-existent) **GAIN[1:0] bits** to control by the **RXGAIN** pin. Deleted the **LNA Input Return Loss** spec (the LNA has required external matching components since Revision 1.1). Modified Table 12 **Transmitter AC Electrical Characteristics** to add **Transmit Modulation Data Rate** and **Transmit Modulation Data Polarity** specs. Corrected **P.A. RF Output Power Level** in PWR0 mode (7 power steps in 4 dB increments yields a 28 dB range, not 32 dB range). Removed TBDs from **Serial Interface Timing Parameter** specs. Added several figures of measured data to the **Typical Operating Characteristics** section.

Revision	Date	Description
1.2	October 2002	Modified Table 10 **Synthesizer AC Electrical Characteristics** to specify the drive conditions for the **XIN** pin separately, depending upon whether DC-coupling or AC-coupling is used. Modified Table 4 **Serial Control Bit Definition** to clarify that the WAKEUP state of the **PWRCTR[2:0]** bits is '010' (PWR2), and serves as a **Revision ID** function. Modified Table 2 **Pin Descriptions** to change the pin description of the **VCC_PLL2B** pin to recommend a bypass capacitor of 0.1 μF to match the Application Schematic. Modified Figure 11 **Application Schematic** to delete the 18Ω resistor on the **VCC_PLL1B** input line as no longer necessary. Added a 10Ω resistor on the **VCC_DIG** line to match the reference design schematic. Modified Table 11 **Receiver AC Electrical Characteristics** to increase the **Demodulated Audio** output level from 175 mVpp to 300 mVpp. Modified the **Functional Description** of the **IF Channel Selection Bandpass Filter** to clarify that the residual error after the COARSE trim sequence is limited to approximately ±50 kHz, not ±100 kHz. Corrected the **counter values** used during the **CAL algorithm** (the values indicated in Revision 1.1 of the spec were in error). Modified Table 3 **Control Register Bit Mapping** and 4 **Serial Control Bit Definition** to add an **RXOFST[6:0]** word. Modified Table 2 **Pin Descriptions** and Table 4 **Serial Control Bit Definition** to show that the only internal test signal that is buffered prior to connection to the Analog Test Bus is the **Slicer Reference Voltage** at ATBSEL[3:0]='1100'.
1.3	December 2002	Modified part marking from **DH24RF17BNC** to **DH24RF17BANC**. Modified pinout to restore the **PA_RAMP** pin, as it is necessary to meet ramp time requirements. Modified Table 3 **Control Register Bit Mapping** and 4 **Serial Control Bit Definition** to add a **SLOWRAMP** bit to extend the P.A. ramp-down timing. Clarified the setting of the **RESERVED** bit. Modified Table 8 **ACTIVE Mode Detail** to clarify that the logic level of the **TC_CTRL** pin is not important during **TUNE** mode. Modified Table 9 **DC Electrical Characteristics** to increase the **IDLE Mode** current as a result of increasing the bias current of the crystal oscillator to improve oscillation characteristics. Modified Table 11 **Receiver AC Electrical Characteristics** to add a **Receive Processing Delay** spec (i.e., group delay plus data lowpass filter delay). Increased the **Demodulated Audio** output level from its previous erroneous value of 300 mVpp to 360 mVpp. Modified Figure 1 **Block Diagram** and the **Functional Description** to show the **RX Gain Step** correctly as 22 dB. Modified Figure 6 **PLL Block Diagram** and **Functional Description** to provide further detail regarding the **wideband PLL mode**. Modified the **Application Overview** section to update the reference BOM parts count. Modified the **EDCT Protocol** section to correctly show the **PP-to-FP Uplink** slots before the **FP-to-PP Downlink** slots (to allow Antenna Diversity algorithm in the FP unit). Modified Figure 11 **Application Schematic** to slightly modify the **TX output matching** components. Updated Figure 27 **PLL Synthesizer Settling Time** with improved measured data. Updated Figure 36 **BER vs RF Level** with data taken with a **GFSK BT=0.6** signal, rather than NRZ data. Also clarified the conditions of the BER test. Added Figure 38 **LNA Input Impedance**.

RFIC BLOCK DIAGRAM

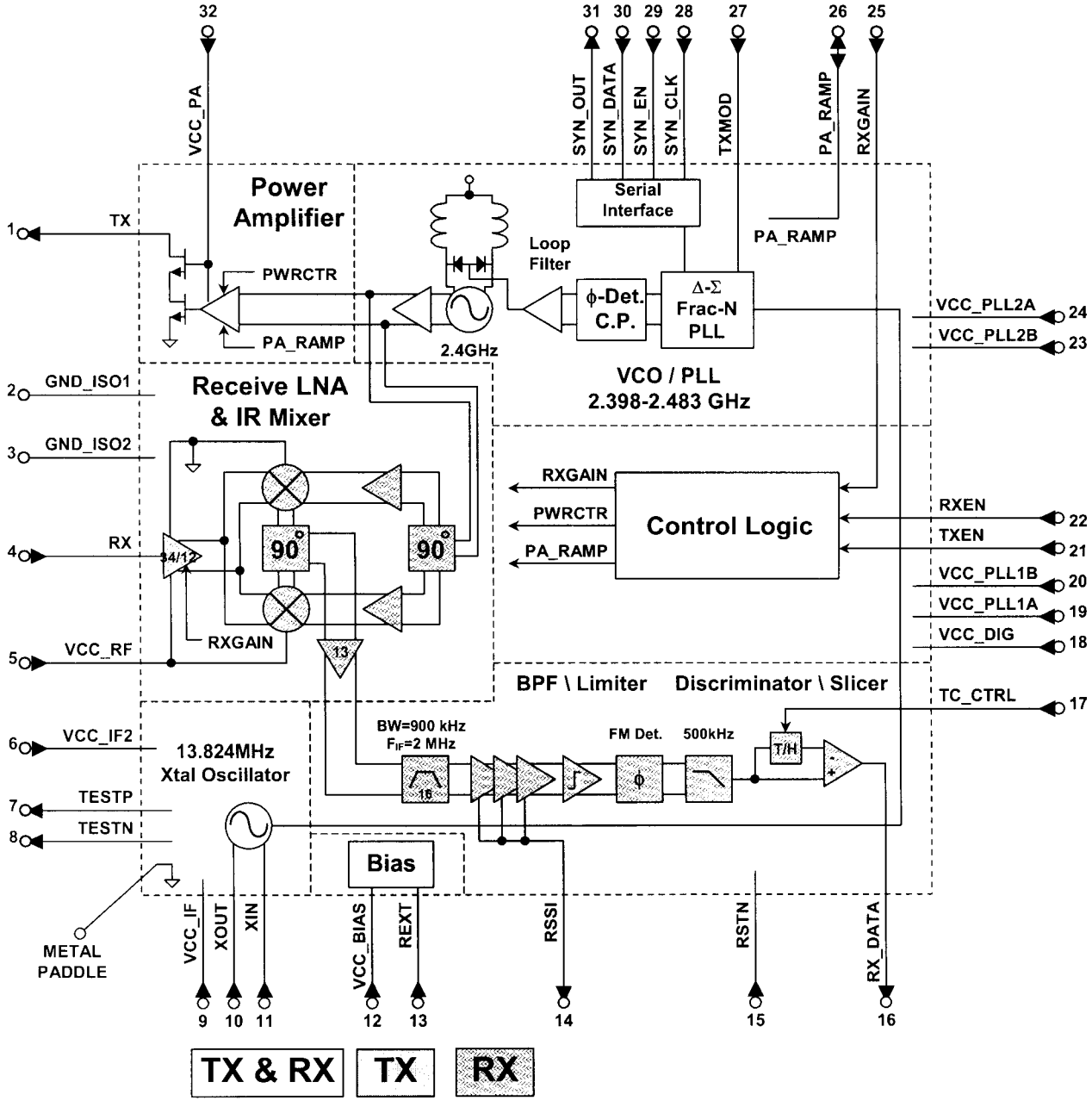


Figure 1. DH24RF17B Block Diagram

SYSTEM BLOCK DIAGRAM

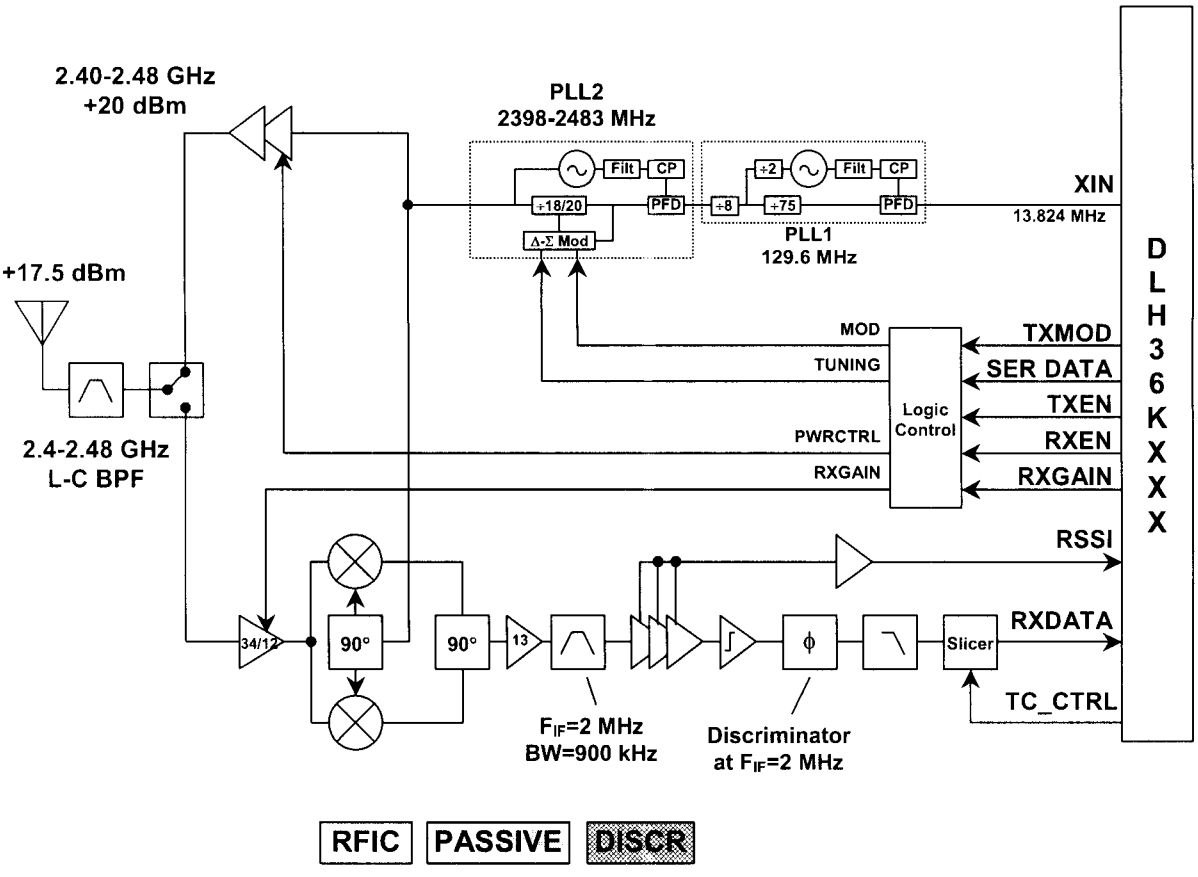


Figure 2. 2.4 GHz Multi-Handset FHSS System Architecture

PIN CONNECTION DIAGRAM

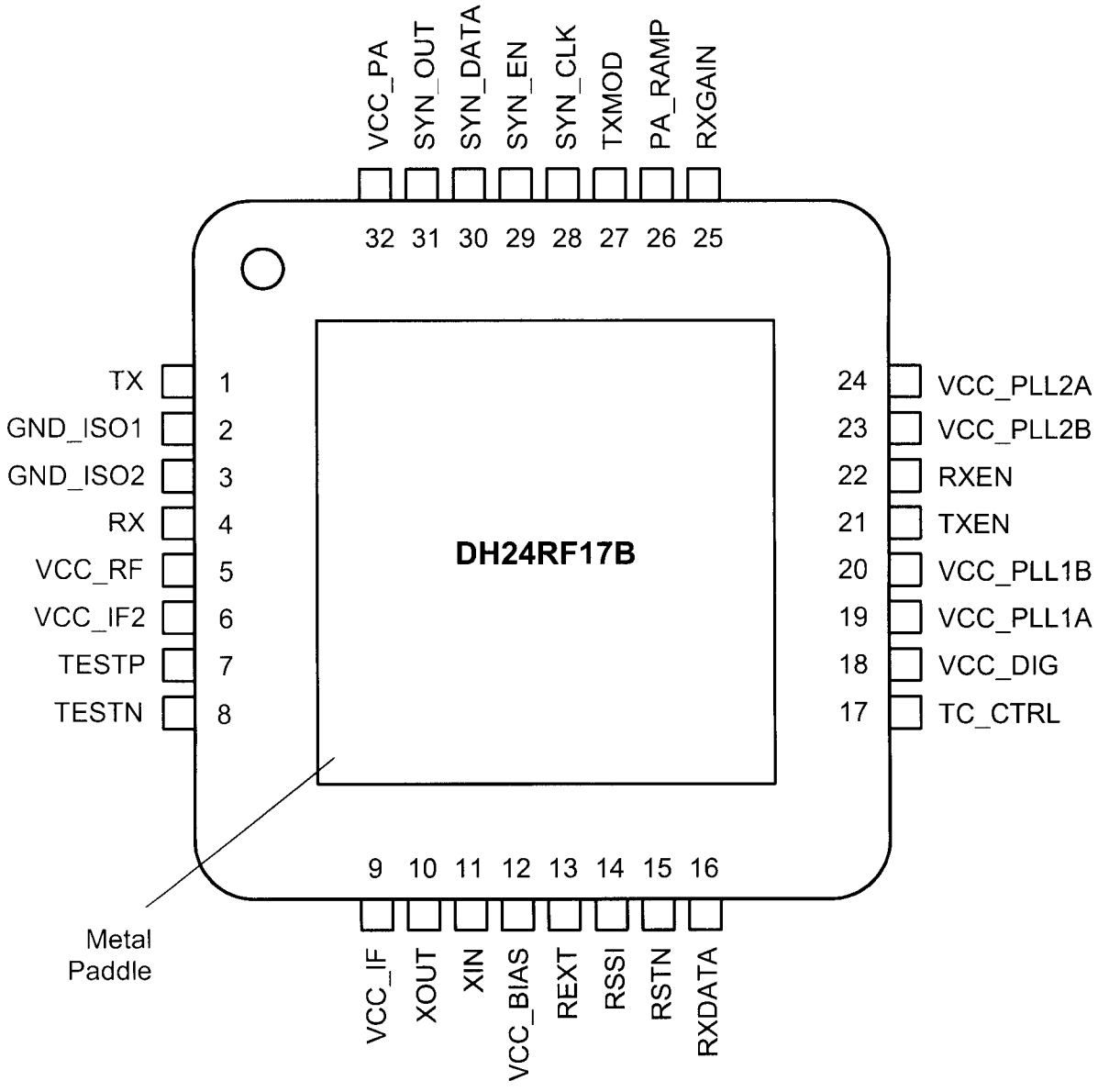


Figure 3. DH24RF17B Pinout

PIN DESCRIPTIONS

Table 2. Pin Descriptions

Pin	Pin Name	I/O	Description
1	TX	O & VCC	TX output at a nominal output level of +20 dBm (maximum power mode). Requires an external L-C match to 50Ω (see the Application Schematic of Figure 11). This is an open-drain output; the external L-C match must also supply V_{CC} (+2.0 to +3.3 VDC, +2.5 VDC nominal) to this pin.
2	GND_ISO1	GND	Ground isolation pin between the TX and RX pins. These pins primarily improve the isolation between the TX output and the RX input on the PCB layout. These ground isolation pins are not connected internally to the chip. Note that this chip has no explicit pins for circuit ground; all of the important RF grounds of the chip are obtained through internal bond wires to the exposed paddle underneath the chip, which is soldered directly to the board.
3	GND_ISO2	GND	Ground isolation pin between the TX and RX pins. These pins primarily improve the isolation between the TX output and the RX input on the PCB layout. These ground isolation pins are not connected internally to the chip. Note that this chip has no explicit pins for circuit ground; all of the important RF grounds of the chip are obtained through internal bond wires to the exposed paddle underneath the chip, which is soldered directly to the board.
4	RX	I	Receive RF input pin to the LNA. Driven single-ended, externally matched to the 50Ω output of the preceding preselector filter. DC-bias is provided internally to the chip; the input signal must be coupled capacitively to this pin.
5	VCC_RF	VCC	+2.5V supply voltage input to the LNA and image-reject mixer circuitry. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at 2.4 GHz at this pin (22 pF).
6	VCC_IF2	VCC	+2.5V supply voltage input to the IF circuitry. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at 2.0 MHz at this pin (0.1 μF to 1.0 μF).
7	TESTP	O	General Purpose Test output pin. A variety of internal test points may be muxed out onto the TESTP and TESTN lines by programming the ATBSEL[3:0] control word. The internal test points are connected to the TESTP and TESTN lines through analog switches without buffering (with the exception of the Slicer Reference Voltage ATBSEL[3:0]='1100'), so any external load on these lines may affect the internal circuit operation.
8	TESTN	O	General Purpose Test output pin. A variety of internal test points may be muxed out onto the TESTP and TESTN lines by programming the ATBSEL[3:0] control word. The internal test points are connected to the TESTP and TESTN lines through analog switches without buffering (with the exception of the Slicer Reference Voltage ATBSEL[3:0]='1100'), so any external load on these lines may affect the internal circuit operation
9	VCC_IF	VCC	+2.5V supply voltage input to the IF circuitry. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at 2.0 MHz at this pin (0.1 μF to 1.0 μF).
10	XOUT	XI/XO	Crystal Oscillator Output. Connect a 13.824 MHz crystal between XOUT and XIN. Alternatively, when using an external clock source, leave this pin unconnected.
11	XIN	XI/XO	Crystal Oscillator Input. Connect a 13.824 MHz crystal between XIN and XOUT. Alternatively, this pin can be driven with an external 13.824 MHz signal source. DC coupling with a nominal 1.2 VDC level is recommended, with a minimum AC amplitude of 700 mVpp. However, a weak internal DC bias is present at the XIN pin and therefore AC coupling is feasible. In this case, a minimum AC drive level of 1.0 Vpp is recommended.
12	VCC_BIAS	VCC	+2.5V supply voltage input to the bandgap and bias circuitry. Connect to regulated +2.5VDC. Provide a good AC bypass to ground at this pin (1 nF).
13	REXT	I	Bandgap resistor connection. Connect a precision (1%) 10.0 kΩ resistor between this pin and ground.

Pin	Pin Name	I/O	Description
14	RSSI	O	Receive Signal Strength Indicator output pin. Provides a voltage output that is proportional to the log of the received signal strength. The RSSI response is linear within a range of 50 dB in both the HIGH_GAIN and LOW_GAIN States, for an overall effective RSSI dynamic range of greater than 80 dB. The RSSI output voltage compliance range is 0.2-2.0 VDC.
15	RSTN	I	External RESET input. This input pin should be held LOW during power-up to cause the RFIC to awaken in a known state, and may be released after the power supply and clock input signal are stable. Alternatively, the same RESET function may be obtained at any time after power-up (or after shutdown into DSLEEP mode) by applying an active LOW pulse of 1 μsec (minimum) to this pin. After RESET, the RFIC awakens into WAKEUP mode. Note that although the RFIC awakens into a known state (WAKEUP), a CAL command must be issued before the PLL(s) are guaranteed to lock to a commanded frequency.
16	RXDATA	O	0-2.5V digital output representing a sliced or "squared-up" version of the analog FM demodulator output. When not in RX mode, this output is at a logic LOW state.
17	TC_CTRL	I	0-3V digital input that switches the time constant of the data slicer decision threshold circuit. This pin must be asserted HIGH during the preamble to enable fast acquisition of the DC average of the incoming data pattern (e.g., '0101'). Switching this pin LOW enables a slow time constant that allows the data slicer to track any slow change of the DC level of the data during the current RX slot. The actual values of the time constant(s) are selectable by bits in the serial control stream.
18	VCC_DIG	VCC	+2.5V supply voltage input to the digital control circuitry. Connect to regulated +2.5VDC. Provide a good AC bypass to ground at this pin (10 nF to 0.1 μF).
19	VCC_PLL1A	VCC	+2.5V supply voltage input to the analog circuitry of PLL1. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at this pin (1 nF to 10 nF).
20	VCC_PLL1B	VCC	+2.5V supply voltage input to the digital circuitry of PLL1. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at this pin (1 nF to 10 nF).
21	TXEN	I	Transmit Enable control input pin. 0-3V digital input. LOW = transmit disabled, HIGH = transmit enabled.
22	RXEN	I	Receive Enable control input pin. 0-3V digital input. This pin enables the receive circuitry (RX LNA/Mixer and IF chain). LOW = receive disabled, HIGH = receive enabled. Note that the OFFSET bit must also be reprogrammed to shift the RX LO frequency downwards prior to entering receive mode.
23	VCC_PLL2B	VCC	+2.5V supply voltage input to the digital circuitry of PLL2. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at this pin (0.1 μF).
24	VCC_PLL2A	VCC	+2.5V supply voltage input to the analog circuitry of PLL2. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at this pin (1 nF to 10 nF).
25	RXGAIN	I	0-3V digital input controlling the gain state of the LNA. HIGH = High Gain and LOW = Low Gain.
26	PA_RAMP	I	P.A. Ramp control input. The ramp waveform at this pin is used to smoothly turn the P.A. on and off during TDD operation. Connect a 470 pF capacitor between this pin and ground.
27	TXMOD	I	0-3V transmit modulation signal from the BBIC. The nominal data rate is 576 kbps. The FM deviation is set internally to the RFIC and is not a function of the amplitude of this signal.
28	SYN_CLK	I	Serial Clock input pin. 0–3V digital input. This pin provides the serial data clock function for the 3-line serial data bus. Data is clocked into the RFIC on positive edge transitions. The nominal serial clock rate is 6.912 MHz.
29	SYN_EN	I	Latch Enable input pin. 0–3V digital input. This pin provides the Data Latch Enable function for the 3-line serial data bus. Data is latched into the RFIC on a positive edge transition.
30	SYN_DATA	I	Serial Data input pin. 0–3 V digital input. This pin provides the serial data stream for the 3-line serial data bus.

Pin	Pin Name	I/O	Description
31	SYN_OUT	O	0-2.5V digital output that provides a serial readback function of the internal control registers.
32	VCC_PA	VCC	+2.5V supply voltage input to the power amplifier circuitry. Connect to regulated +2.5VDC. Provide a good RF bypass to ground at this pin (1 nF).
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the RFIC supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the RFIC.

FUNCTIONAL DESCRIPTION

RX LNA

The received signal within the 2.400–2.4835 GHz ISM band is typically band-pass filtered by an external preselector filter before application to the 2.4 GHz low-noise amplifier (LNA) integrated on-chip. The LNA nominally provides 34 dB of gain with a typical noise figure of 4 dB, thus suppressing the noise contributions of subsequent stages. The LNA input pin is externally matched to 50Ω by an L-C network. The LNA is implemented as a cascode amplifier with constant Gm bias to reduce gain variation. The LNA is followed by a single-ended to differential converter stage to provide the appropriate differential drive signals to the subsequent image-reject mixer. The LNA is internally DC-biased and requires AC-coupling with an external capacitor.

RX Gain Switching

The instantaneous dynamic range of the RFIC is approximately 50 dB. In order to provide a much larger effective dynamic range, the chip provides a method of switching (reducing) the gain of the LNA by nominally 22 dB. By overlapping the dynamic ranges of each gain state, the chip is able to achieve an overall effective dynamic range of greater than 75 dB.

RX Image-Reject Mixer

The output of the LNA is fed internally to the input of the receive mixer. The receive mixer is implemented as an image-reject mixer (IRM) that suppresses the image noise and signal bands, thus greatly reducing the need for additional band-pass filtering. The IRM consists of two double-balanced mixers whose RF inputs are driven in parallel, local oscillator (LO) inputs are driven in quadrature, and intermediate frequency (IF) outputs are combined in quadrature. The receive LO signal is supplied by an integrated VCO and PLL synthesizer operating within the 2.3987–2.4837 GHz ISM band. The necessary quadrature LO signals are obtained by applying the receive LO signal to a two-stage R-C polyphase filter that provides a 90° phase shift across its outputs. The resulting IF mixer outputs are summed together in another R-C polyphase filter such that the desired signal is reinforced and the image signal is cancelled. In this device, the outputs are summed in a fashion as to always select the upper sideband as the desired signal while providing rejection of the lower sideband. The double-balanced mixers are implemented as a pair of Gilbert-cell active mixers that not only provide reasonable linearity at low current consumption, but also provide an additional amount of conversion gain (~13 dB) that helps improve sensitivity. Overall, the typical gain of the combined LNA/mixer block is 47 dB (in the HIGH_GAIN mode) with a noise figure of 6.5 dB. In the LOW_GAIN mode the typical IIP3 of the combined LNA/mixer block is -23 dBm. A minimum of 20 dB (typically 25 dB) of rejection is obtained at the image frequency.

The output of the receive image-reject mixer is at an IF frequency of 2 MHz. This choice of low IF allows integration of the high-Q channel-selection filters. The R-C polyphase combiner at the mixer output is aligned to a center frequency of 2 MHz by "borrowing" the result from calibration of the 2 MHz channel selection bandpass filter (see discussion below) and applying the same correction factor to its capacitors.

As the subsequent IF chain contains over 70 dB of gain, it is very important to provide a good RF bypass to ground at 2 MHz at the VCC_IF input pin. A capacitance value of 0.1 μF to 0.47 μF is suggested. The receive LNA/mixer block is switched with the RXEN input and is powered down when not in RX mode.

IF Channel Selection Bandpass Filter

After down-conversion to an IF frequency of 2 MHz, the receive signal is filtered by an integrated bandpass channel selection filter. This bandpass filter rejects adjacent channel signals and determines the noise bandwidth of the desired signal. The filter is implemented as five active R-C bi-quad amplifier stages. This approach results in lower noise and higher dynamic range than a GmC or switched-cap filter. Additionally, the Q of each stage remains relatively low, which results in better performance over processing variations. The nominal 3 dB bandwidth of the filter is 900 kHz. The bandpass filter also provides approximately 16 dB of gain. The IF bandpass filter frequency response is shown in Figure 32.

The channel selection bandpass filter has been implemented with a novel alignment scheme. Because the absolute values of the integrated resistors and capacitors can vary considerably over process variations, it is necessary to calibrate the center frequency of the filter prior to use. To accomplish this, the final bi-quad stage can also be configured as an oscillator. When the CAL mode is entered, the oscillator is enabled and its output frequency is digitally counted. This is done by gating the 129.6 MHz high-speed clock from PLL1 to a counter for exactly 7 periods of the oscillation frequency of the bi-quad oscillator. Since the frequency of PLL1 is known exactly, the value of the counter should theoretically equal (7/2.0 MHz)*(129.6 MHz). Any deviation from this theoretical value indicates a residual error in the nominal 2.0 MHz frequency of the bi-quad oscillator (and thus the frequency of the IF bandpass filter). If the frequency of oscillation differs from 2 MHz, small amounts of capacitance are added or removed from the bi-quad oscillator circuit until the frequency error is (nearly) removed. The same amount of capacitive adjustment is then made to the remaining bi-quads in the bandpass filter, with the result that the frequency response of the filter is also (nearly) centered at 2 MHz. The trim capacitance is switched in binary-weighted increments, and the resulting coarse trim value may be read back in the BPFTRIM[3:0] register (see *Control Logic & Serial Interface*). The value of trim capacitance may also be manually controlled by setting the bandpass filter override bit (BPFOVER) and then manually writing the desired value of BPFTRIM[3:0].

At the end of the coarse trim sequence, there may be some residual error in the tuning of the IF bandpass filter as the resolution of the trim capacitors can only guarantee tuning to within ±2.5% (roughly ±50 kHz) of the desired 2 MHz center frequency. To further improve accuracy, a secondary operation is performed to measure the residual frequency offset. This is again done by gating the 129.6 MHz high-speed clock from PLL1 to a counter for exactly 31 periods of the oscillation frequency of the bi-quad oscillator. Since the frequency of PLL1 is known exactly, the value of the counter should theoretically equal (31/2.0 MHz)*(129.6 MHz). Any deviation from this theoretical value indicates a residual error in the nominal 2.0 MHz frequency of the bi-quad oscillator (and thus the frequency of the IF bandpass filter). The value in this counter is used to offset the frequency of the Δ-Σ PLL synthesizer in RX mode to remove this residual error. As an example, if the coarse trim operation succeeds in tuning the IF bandpass filter to a center frequency of 2.02 MHz, there is a residual error of +20 kHz. The residual error is measured and used to offset the RX LO so that the frequency of the received signal (after down-conversion) is also centered at 2.02 MHz. This means that the actual frequency of the IF signal may not be known exactly at any given time. However, the frequency of the IF signal tracks the tuned frequency of the IF bandpass filter, so the operation is transparent to the user. The offset is applied to the Δ-Σ PLL synthesizer only in RX mode; the output frequency in TX mode is unaffected. The value of frequency offset may be read back in the AFC[5:0] register (see *Control Logic & Serial Interface*). The value of frequency offset may also be manually controlled by setting the bandpass filter override bit (BPFOVER) and then manually writing the desired value of AFC[5:0]. The value in the AFC[5:0] register is treated as a signed integer, ranging in value from –32 to +31. The resolution of the RX LO frequency offset is in increments of 3.95 kHz, for a total AFC adjustment range of ±122.5 kHz. Note that a negative value of RX LO frequency offset will result in an increase in IF frequency due to the use of a low-side injection scheme in the image-reject mixer.

In addition to the AFC control word, an additional RX offset register (RXOFST[6:0]) is provided to allow tuning of the IF signal at positions other than the center of the channel selection filter. Again, the resolution of the RX offset adjustment is in increments of 3.95 kHz, for a total RX offset adjustment range of ±248.9 kHz.

Both the coarse trim sequence (capacitor adjustment) and fine trim sequence (PLL automatic frequency control adjustment) are accomplished by setting the CAL bit via the serial port.

IF Limiter

The output signal from the channel selection bandpass filter is fed to the IF limiter. The IF limiter is a 4-stage amplifier chain that provides approximately 60 dB of additional gain to the 2 MHz IF signal. When the front-end gains of the LNA, mixer, and channel selection filter are added, this is sufficient to ensure that the IF output signal is hard-limited under all signal conditions. The limiter stages also contain full-wave peak detectors whose current outputs are summed together to obtain the RSSI signal.

RSSI

A Receive Signal Strength Indication (RSSI) is provided on the RSSI output pin. This output provides a voltage that is proportional to the log of the received signal strength. The slope of the RSSI signal is nominally 30 mV/dB, with a linear range of approximately 50 dB in both the HIGH_GAIN and LOW_GAIN RX gain states. Because the dynamic ranges of these two gain states overlap, this allows the chip to achieve an overall effective RSSI dynamic range in excess of 70 dB. The output range of the RSSI voltage is approximately 0.2-2.0 VDC. A plot showing typical RSSI voltage as a function of input signal level is shown in Figure 23. As the RSSI circuit responds quite rapidly, the RSSI voltage becomes noisy at low signal levels. Some small amount of 2.0 MHz ripple voltage may also be present on the RSSI output signal. Placing a capacitor to ground at this pin can filter the RSSI voltage. Internally, a 500Ω resistor is placed between the RSSI detector circuitry and the RSSI output pin. Thus placing an external capacitor at this pin completes an R-C filter circuit. A capacitance value of approximately 2.2 nF is recommended. Much larger values of capacitance may degrade the RSSI response time.

FM Discriminator

The limited 2 MHz IF signal is internally applied to an integrated dual one-shot type FM discriminator. In this circuit, each edge (rising and falling) of the limited IF signal drives an independent one-shot whose pulse width is nominally set at $T_{IF}/4$ = (1/2.0 MHz)/4 = 125 nsec. The outputs of the two one-shots are logically OR'ed together to produce a pulse train at twice the input frequency. When the IF input signal is at 2 MHz the resultant pulse train will have a nominal 50% duty cycle. This is illustrated in Figure 4. The pulse train is passed through a lowpass filter that removes the 2X frequency component (at 4 MHz) and leaves a DC component proportional to the duty cycle of the pulse train. The lowpass filter is a 5th order Bessel filter with a cutoff frequency of 500 kHz. The data filter is implemented using active bi-quad stages similar to those used in the channel selection filter; thus the data filter "borrows" the result from calibrating the 2 MHz channel selection bandpass filter and applies the same correction factor to its own trim capacitance banks.

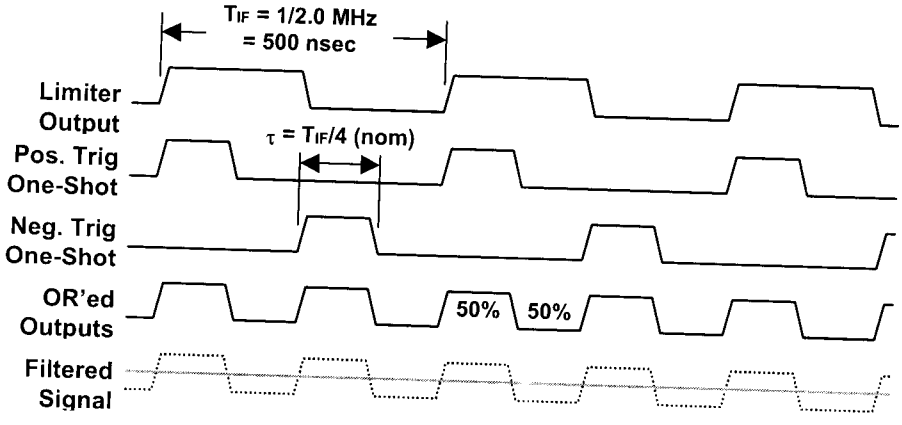


Figure 4. One-Shot FM Discriminator—F_{IF}=2 MHz

When the frequency of the IF signal is varied (i.e., frequency modulated), the one-shots will be triggered more rapidly or less rapidly. Because τ is fixed, the duty cycle of the pulse train will vary with F_{IF}. After filtering, what remains is an audio (near-DC) component whose amplitude is proportional to F_{IF}. Thus the circuit operates as an FM detector. This is shown in Figure 5.

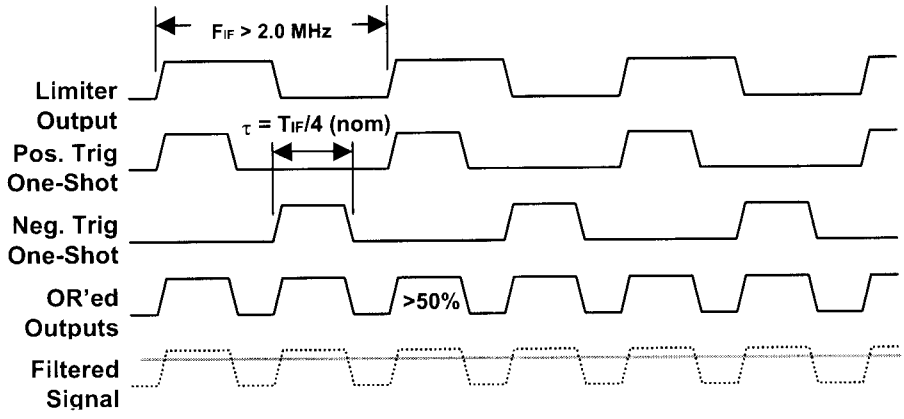


Figure 5. One-Shot FM Discriminator—F_{IF}>2.0 MHz

Although the operational frequency range of the detector is quite wide, it is desired to calibrate the discriminator to ensure that the average analog DC output voltage (corresponding to the IF center frequency) is maintained near 1.0 VDC. This ensures that the analog demodulated output voltage is centered in the operational range of the A/D converter in the baseband chip. Calibration is accomplished by demodulating the 2.0 MHz output of the calibration oscillator in the channel selection bandpass filter. The delay periods of the one-shots are adjusted until the resulting DC output voltage is centered at 1.0 VDC. The demodulated audio is available at the TESTP and TESTN output pin(s) by selecting ATBSEL[3:0]='1001', and is nominally at an output level of 300 mVpp (single-ended) for the specified frequency deviation of ±190 kHz.

Data Slicer

The filtered FSK audio from the discriminator is directly applied internally to one input of the data slicer. The data slicer is a comparator that compares the recovered audio to a reference voltage threshold, and outputs a CMOS-compatible logic signal if the audio voltage is above or below the threshold. The reference voltage is derived from the average DC voltage of the demodulated audio. This way, the data slicer always tracks the average carrier frequency of the received signal, and reduces the requirement for precise frequency synchronization between the base and the handset. During the EDCT preamble (a perfectly balanced '01010'...bit stream), the TC_CTRL line is asserted HIGH and the average DC voltage of the demodulated audio is extracted by passing the signal through a switched-capacitor lowpass filter with a relatively fast time constant. After the preamble is completed and the DC voltage has settled at the proper threshold, the TC_CTRL line is switched from HIGH to LOW and the lowpass filter is switched to a low time constant such that the data slicer threshold now only tracks very slow changes in the DC offset of the incoming signal (i.e. "open loop drift" of the transmitter) and not DC offset due to a long string of 0's or 1's in the incoming data stream. The cutoff frequency (i.e., time constant) of the switched-capacitor filter is adjusted internally by changing the clock frequency to the filter.

The absolute values of the fast and slow time constants are selectable by bits in the serial control stream. The selectable values of the slow time constant are ~270 µsec, 546 µsec, 820 µsec, and infinite µsec (HOLD mode). The selectable values of the fast time constant are ~8.5 µsec, 17 µsec, 25 µsec, and 34 µsec.

The sliced, or "squared-up", representation of the demodulated audio is provided on the RXDATA output pin as a 0-2.5V CMOS-compatible logic signal. If the RXEN input pin is set LOW, the RXDATA output is held in a logic LOW state.

VCO(s) & PLL Synthesizer

An integrated PLL synthesizer capable of operating within the ISM band of 2.400–2.4835 GHz is provided on-chip. The PLL is implemented as a Fractional-N synthesizer that uses the Delta-Sigma (Δ-Σ) method of frequency control. This approach has several advantages. First, fine-tuning resolution may be obtained while maintaining the wide loop bandwidth necessary to support the fast frequency-hopping protocol. Additionally, transmit modulation may be applied to the loop in the digital domain (by simply modifying the Δ-Σ control data stream), which results in very precise control over the transmit deviation.

The dual PLL scheme and Δ-Σ modulator is designed to support the channel spacing (891.871 kHz), Gaussian filtering (B_bT = 0.6), TX data rate (576 kbps), and PLL synthesizer lock time required by the EDCT protocol. The synthesizer consists of two cascaded PLLs, as shown in Figure 6. The first loop (PLL1) operates at a fixed frequency of 129.6 MHz. Its purpose is to provide the high frequency reference and over-sampling clock required by the Δ-Σ architecture. This PLL uses a differential L-C oscillator VCO operating at 2073.6 MHz, followed by a ÷16 circuit. The loop filter is of a standard lead-lag topology, comprised of discrete passive components integrated on-chip (R_1, C_1, & C_2 in Figure 6). The loop filter components have been chosen to achieve a PLL1 loop bandwidth of approximately 375 kHz. Although PLL1 operates at a fixed frequency, the wide loop bandwidth is necessary to suppress the phase noise of the VCO.

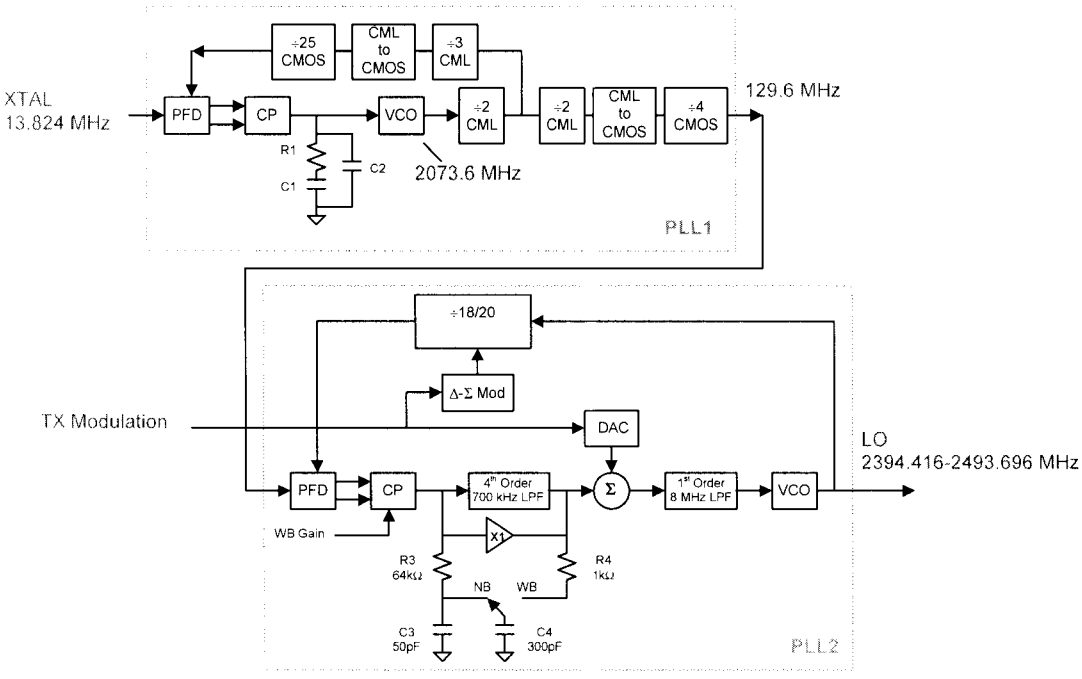


Figure 6. PLL Synthesizer Block Diagram

The 129.6 MHz output from PLL1 serves as the reference frequency for the Δ-Σ modulator and 2.4 GHz PLL (PLL2). PLL2 operates over the 2.400–2.4835 GHz range. This PLL uses an N-channel differential L-C VCO. The spiral inductors for the VCO are also integrated on-chip. The output of the VCO is fed back to a ÷18/20 divider stage. The modulus of this divider stage is controlled dynamically by the output from the Δ-Σ modulator. Intuitively, one can see that if the counter was commanded only to ÷20, the resulting output frequency would be 129.6 MHz x 20 = 2592.0 MHz. Similarly, the lower bound on output frequency is calculated as 129.6 MHz x 18 = 2332.8 MHz. The data stream from the Δ-Σ modulator controls the proportion of time spent dividing by 18 or 20. The result is an output frequency (between the limits calculated previously) with an average frequency proportional to the time spent dividing by 18 or 20. Practical limitations of the loop filter and digital control circuitry restrict the actual output frequency range to less than the calculated limits, but it is still easily possible to synthesize frequencies over the required 2398.00-2483.5 MHz band (2400.0-2483.5 MHz ISM band less 2.0 MHz in RX mode). In fact, the RFIC provides coverage of extra channels above and below the ISM band for test purposes. Thus it is actually possible to command the PLL synthesizer over the frequency range of 2392.320-2492.925 MHz. The desired channel number is selected by the FREQ[7:0] bits in the serial data stream. The FREQ[7:0] word is decoded internally so that Channel 0=2391.106 MHz, Channel 1=2391.996 MHz etc. up to Channel 116=2494.563 MHz. In normal operation, only Channels 11-103 will be used (2400.914-2482.966 MHz). The channel spacing is nominally 891.871 kHz. The tuning resolution of the Δ-Σ modulator is determined largely by the over-sampling rate (129.6 MHz) and the number of bits carried internally. The tuning resolution in the current implementation is sufficient to tune to the commanded frequency with an accuracy of 3.955 kHz anywhere in the band. However, one should note that the resultant output frequency may not be an exact multiple of the channel spacing; there is an error of uncertainty equal to the 3.955 kHz tuning resolution.

A characteristic of Fractional-N synthesizers is high in-band instantaneous phase error due to quantization errors (noise). This arises from dividing the output frequency by a "variable" divider modulus. At any given instant, the output of the ÷18/20 divider stage may be greater or less than 129.6 MHz, resulting in a phase error from the phase-frequency detector (PFD) and charge pump. Only when viewed over a longer period of time does the average output frequency appear correct. Fortunately, digital filtering techniques inside the Δ-Σ modulator can "push" this quantization noise above the loop bandwidth, where conventional R-C filtering techniques can easily remove it. This is shown in Figure 6. The zero of the loop filter transfer function is set by discrete integrated components R_3, C_3, and C_4. The location of the zero is the dominant factor in determining the loop bandwidth of PLL2, and is set to result in a loop bandwidth of approximately 45 kHz. This choice of loop bandwidth is primarily determined by the phase noise requirements of the system. However, during a frequency hop to a new channel the loop bandwidth is briefly switched automatically to a wider bandwidth in order to meet the fast settling time requirements of the frequency hopping protocol. This is done by simultaneously increasing the gain of the charge pump and increasing the frequency of the loop filter zero, as shown in Figure 6. The loop filter zero is followed by a 4^{th} order Butterworth active lowpass filter, implemented as two cascaded Sallen-Key filters. This filter rolls off the quantization noise that has been pushed out to higher frequencies by the Δ-Σ modulator. The cutoff frequency of this filter is approximately 500 kHz, and is calibrated by again "borrowing" the CAL result from the 2 MHz channel selection bandpass filter and applying the same correction factor to its own trim capacitance banks.

It is obvious that if an average divide ratio of ÷19 is desired, the Δ-Σ modulator must command the variable divider stage to spend equal amounts of time dividing by 18 or 20. One possible divider modulus control stream that would accomplish this would be a '101010…" Δ-Σ modulator output stream. However, such a predictable modulus pattern gives rise to discrete spectral lines in the synthesizer output spectrum. It is possible to "dither" the modulus control stream in a pseudo-random fashion to spread out these discrete tones while still maintaining the desired average division ratio. The dithering factor may be selected by programming the DITHPROG[2:0] control word.

In a similar fashion, the transmission zero of the Δ-Σ modulator's digital filter transfer function can be varied slightly to best suppress the high frequency quantization noise. The location of this resonator may be varied by programming the RESPROG[1:0] word.

Another potential source of phase noise is the contribution of the current noise from the charge pumps. One way to reduce the effect of this noise source is to reduce the tuning sensitivity of both the PLL1 and PLL2 VCOs. The tuning sensitivity (K_V) of a VCO may be reduced while still maintaining full frequency coverage by partitioning the frequency band into a number of smaller sub-bands. Within each sub-band, a smaller frequency range is covered for the same change in tuning voltage, thus effectively reducing K_V. Each sub-band is constructed to overlap the adjacent sub-band, thus guaranteeing overall coverage of the entire desired frequency range. The mapping of a desired frequency channel to a VCO sub-band is determined during the CAL operation, and is stored away for subsequent use. The VCO sub-band value for the currently-tuned frequency may be read back in the VCO1TRIM[4:0] or VCO2TRIM[4:0] register (see *Control Logic & Serial Interface*). The value of a VCO sub-band may also be manually controlled by setting the VCO override bit (VCO1OVER or VCO2OVER) and then manually writing the desired value of VCO1TRIM[4:0] or VCO2TRIM[4:0].

As the output frequency of the synthesizer is determined by adjusting the digital control stream to the dual modulus divider, it is relatively simple to frequency modulate the PLL. A digital word (proportional to the instantaneous amplitude of the TX modulation data) is simply summed with the digital control stream output of the Δ-Σ modulator. This causes the output frequency to increase or decrease proportional to the input modulation. It should be noted that this digital modulation word is ALWAYS applied to the Δ-Σ modulator. This means that even when time-varying modulation data is not applied to the TXMOD input pin, the frequency of the unmodulated carrier signal will be at $F_C + \Delta F$ or $F_C - \Delta F$ (depending upon the static logic level applied to TXMOD).

One difficulty in modulation arises from the fact that the loop bandwidth (~45 kHz) is less than the data rate (576 kbps). Thus the closed-loop action of the PLL tends to roll off or distort the higher frequency components of the TX modulation. To counteract this effect, the TX modulation is applied to two points in the loop: 1) the digital control stream of the Δ-Σ modulator, and 2) the VCO tuning voltage input. The polarities of the two signals are controlled in such a fashion that the modulation introduced into the VCO tuning voltage input is cancelled in the feedback path by the modulation pattern applied to the Δ-Σ modulator. Thus although the modulation appears on the VCO output signal, the error signal out of the phase-frequency detector is ideally zero regardless of the TX modulation sequence. To achieve perfect cancellation, it is necessary to accurately adjust the amplitude of the modulation signal applied to the VCO tuning voltage input. This modulation signal is provided by a DAC with adjustable gain. An automatic calibration routine prior to every transmit frame adjusts the gain of the DAC via the GAINTRIM[4:0] word to provide (nearly) perfect cancellation.

Transmit Power Amplifier

The RFIC contains an integrated power amplifier capable of producing +20 dBm output power. The P.A. is implemented as a two-stage complementary overdriven amplifier, operating between Class AB and Class C (depending upon the desired output level). The output stage is an open-drain cascode transistor and is externally matched to 50Ω using a shunt inductor to V_{CC} (+2.5VDC nominal, +3.3VDC maximum), a small shunt capacitor, and a small series capacitor.

The output of the power amplifier may be reduced from the maximum output level in order to reduce current consumption and extend the battery life. The power amplifier allows for 8 levels of output power. The nominal maximum power level is full power (+20 dBm) and the nominal minimum power level is -12 dBm. The intermediary gain steps are available in approximately 4 dB increments. The power amplifier output level is adjusted as a function of the PWRCTR[2:0] bits in the serial data stream. Typically, the power amplifier output level will be reduced when the quality of the link is high enough to operate at reduced signal-to-noise ratios. The power control is implemented by use of a digitally-switched amplifier. The rising and falling edges of the P.A. output signal are ramped to prevent unwanted spectral splatter. The time constant(s) of the rising and falling edges may be adjusted by varying the value of the C_{RAMP} capacitor connected to the PA_RAMP output pin, as shown in the Application Schematic of Figure 11.

The power amplifier is powered down when not in TX mode.

Crystal Oscillator

A 13.824 MHz crystal oscillator is integrated in the RFIC. The circuit requires an external 13.824 MHz crystal blank and two capacitors. The crystal blank with a specified value of C_{LOAD} (i.e. 10 pF, 18 pF or 32 pF) is placed across the XIN and XOUT pins. The effective C_{LOAD} presented to the crystal blank by the internal RFIC circuitry and any external shunt capacitance can be computed by the equation:

$$C_{Load} = \{(C_{p1} + C_{t1} + C_{s1})^{-1} + (C_{p2} + C_{t2} + C_{s2})^{-1}\}^{-1} + C_{pf}.$$

This is illustrated in Figure 7. Some internal parasitic capacitance (C_{p1} and C_{p2}) exists at each node due to the ESD diodes and bond pads. A small internal capacitance (C_{pF}~ 1 pF) is integrated across the inverter of the oscillator. Additionally, two banks of digitally programmable capacitances (C_{t1} and C_{t2}) are integrated in the RFIC, one at each XIN or XOUT node. Each bank consists of 256 capacitors in parallel with each individual capacitor 282 fF in value. These banks of capacitors are controlled by the 6-bit OSCCAPS[5:0] programming word. Setting OSCCAPS[5:0]='000000' means $C_{t1}=C_{t2}=0$ pF, setting OSCCAPS[5:0]='000001' means $C_{t1}=C_{t2}=282$ fF ±15%, and so on up to OSCCAPS[5:0]='111111' means $C_{t1}=C_{t2}=17.766$ pF ±15%. In this fashion, a cheaper crystal with a looser frequency tolerance may be used, as the BBIC can tune the crystal to the desired frequency.

The OSCCURR bit in the serial control stream may be used to adjust the bias current of the crystal oscillator circuitry. An increased level of bias current may be required to support a strong mode of oscillation with some crystal blanks.

In normal ACTIVE mode operation, the crystal oscillator remains enabled at all times. However, when the RFIC is placed into IDLE mode by setting the RADIOEN bit to a logic LOW, the oscillator may be disabled by setting the OSCOFF bit HIGH, resulting in even lower current consumption. Note that it may take a significant amount of time for the crystal oscillator to turn ON and OFF, due to the high Q of the crystal blank.

It is also possible to use an external crystal oscillator. In this scenario, the external oscillator signal is injected on XIN. DC coupling with a nominal 1.2 VDC level is recommended, with a minimum AC amplitude of 700 mVpp. However, weak DC bias exists at the XIN pin due to the internal 1 MΩ NMOS resistor biasing the oscillator block, and therefore AC coupling is feasible. In this case, a minimum AC drive level of 1.0 Vpp is recommended. Note that the OSCOFF bit should be set to a logic LOW when using an external clock signal, as this bit controls the analog buffer in addition to the oscillator gain block.

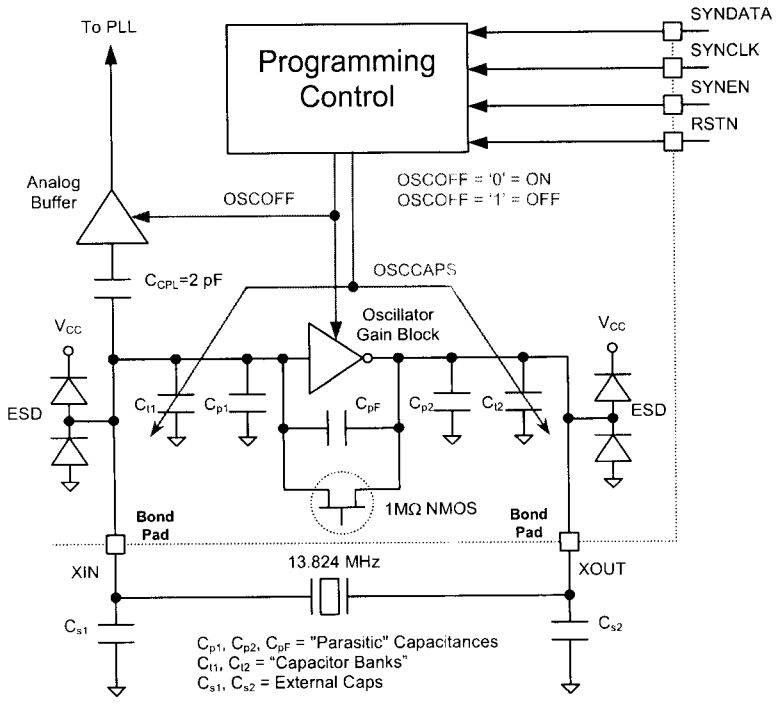


Figure 7. Crystal Oscillator Block Diagram

Control Logic & Serial Interface

The control logic block contains the circuitry that accepts control words over a 3-wire serial interface and latches them into the appropriate internal registers. This block also contains combinatorial logic that accepts time-critical signals (such as TXEN, RXEN, and SHCTRL) and routes them directly to the required functional blocks. The control words sent over the serial interface consist of a READ/WRITE bit, a 3-bit address header and an 8-bit data field. The 3-bit address header allows addressing of eight unique 8-bit control words. The timing of the serial interface signals in WRITE mode is shown in Figure 8 below. The SYN_DATA and SYN_CLK lines may be shared by other peripheral devices (such as a serial EEPROM). Data bits intended for other devices may be clocked into the shift register of the RFIC without affecting its operation, as long as the SYN_EN strobe unique to the RFIC is not also sent. When the unique SYN_EN strobe is received, the last 12 bits (R/W bit + 3 ADDR bits + 8 DATA bits) are latched and interpreted. The serial interface is placed into WRITE mode by setting the READ/WRITE bit LOW. The data bits are clocked into the shift register on the rising edge of SYN_CLK.

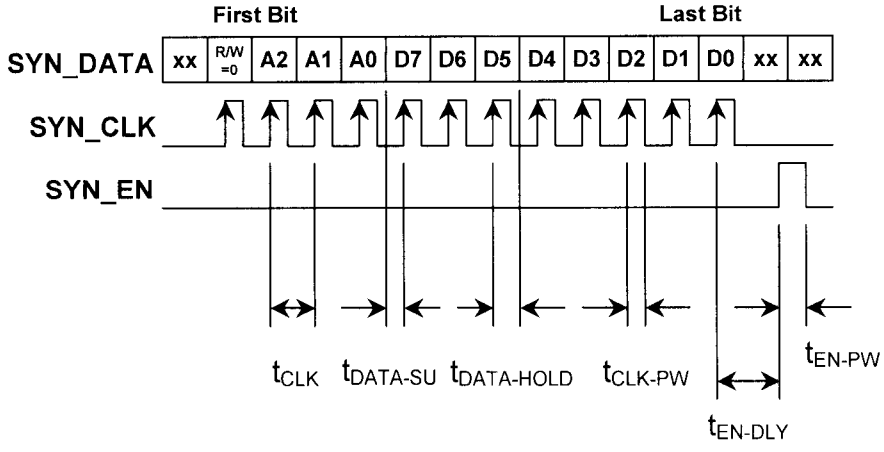


Figure 8. Serial Interface Timing—WRITE Mode

The serial interface may also be used to read data back from the RFIC. The serial interface is placed into READ mode by setting the READ/WRITE bit HIGH. When a 12-bit word is received that contains the READ/WRITE bit set HIGH, the address field is remembered but the 8-bit contents of the data field are ignored (i.e., NOT latched into the addressed register upon receipt of the SYN_EN pulse). The next eight positive edge transitions of the SYN_CLK signal will clock out the contents of the register addressed by this previous control word. This is illustrated in Figure 9. When placed into READ mode, the contents of the register are output on the SYN_OUT pin. It is envisioned that the READ mode will only be used for test purposes.

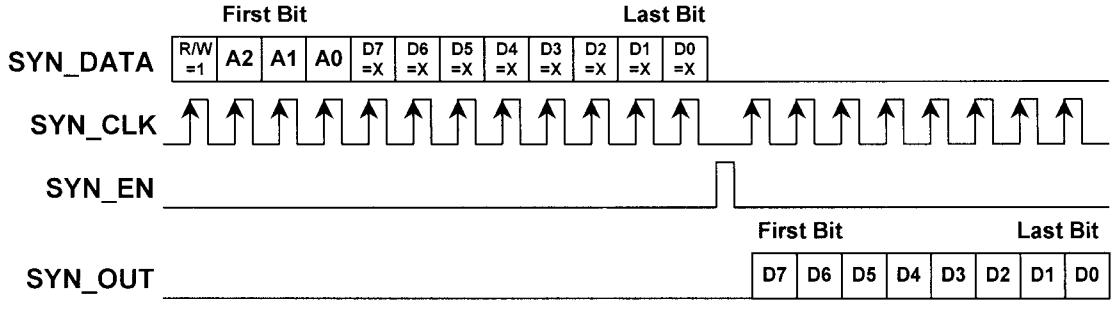


Figure 9. Serial Interface Timing—READ Mode

The mapping of the control bits into the eight addressable control words is shown in Table 3 below. A detailed explanation of each control bit is shown in Table 4 below.

Table 3. Control Register Bit Mapping

A[2:0]	D7	D6	D5	D4	D3	D2	D1	D0
000	OFFSET	OPENPLL	RADIOEN	OSCCURR	OSCOFF	SPARE	(RESERVED)	DSLEEP
001	SPARE	SPARE	OSCCAP[5]	OSCCAP[4]	OSCCAP[3]	OSCCAP[2]	OSCCAP[1]	OSCCAP[0]
010	FREQ[7]	FREQ[6]	FREQ[5]	FREQ[4]	FREQ[3]	FREQ[2]	FREQ[1]	FREQ[0]
011	CAL	PWRCTR[2]	PWRCTR[1]	PWRCTR[0]	FASTTC[1]	FASTTC[0]	SLOWTC[1]	SLOWTC[0]
100	0	0	EXTCLKSEL	IOTEST	ATBSEL[3]	ATBSEL[2]	ATBSEL[1]	ATBSEL[0]
100	0	1	MODDIVLOW	**DITHPROG[2]**	DITHPROG[1]	DITHPROG[0]	RESPROG[1]	RESPROG[0]
100	1	0	GAINOVER	GAINTRIM[4]	GAINTRIM[3]	GAINTRIM[2]	GAINTRIM[1]	GAINTRIM[0]
100	1	1	WIDEBAND	INVDOUT	INVDIN	BISTDONE	BISTSHORT	BIST
101	DMODOVER	DMODTRIM[6]	DMODTRIM[5]	DMODTRIM[4]	DMODTRIM[3]	DMODTRIM[2]	DMODTRIM[1]	DMODTRIM[0]
110	0	0	VCO1OVER	VCO1TRIM[4]	VCO1TRIM[3]	VCO1TRIM[2]	VCO1TRIM[1]	VCO1TRIM[0]
110	0	1	VCO2OVER	VCO2TRIM[4]	VCO2TRIM[3]	VCO2TRIM[2]	VCO2TRIM[1]	VCO2TRIM[0]
110	1	0	AFC[5]	AFC[4]	AFC[3]	AFC[2]	AFC[1]	AFC[0]
110	1	1	SLOWRAMP	BPFOVER	BPFTRIM[3]	BPFTRIM[2]	BPFTRIM[1]	BPFTRIM[0]
111	0	RXOFST[6]	RXOFST[5]	RXOFST[4]	RXOFST[3]	RXOFST[2]	RXOFST[1]	RXOFST[0]
111	BISTSIG[7]	BISTSIG[6]	BISTSIG[5]	BISTSIG[4]	BISTSIG[3]	BISTSIG[2]	BISTSIG[1]	BISTSIG[0]

Table 4. Serial Control Bit Definition

String Name	Bits	Function
OFFSET	1	When this bit is set HIGH, the PLL synthesizer is offset from the RF Channel by -2.0MHz. This allows the LO to be set below the RF channel for receive mode by setting a single bit, rather than sending an entirely new frequency word. The default value in WAKEUP mode is OFFSET=LOW (no frequency offset).
OPENPLL	1	When this bit is set HIGH, the PLL synthesizer is placed in an open-loop configuration where the VCO is free-running. This is typically done for test purposes only, and allows the free-running properties of the VCO to be characterized. The default value in WAKEUP mode is OPENPLL=LOW (closed-loop operation).
RADIOEN	1	When this bit is set HIGH, the PLL synthesizer is enabled. Note that when RADIOEN is LOW (and DSLEEP is not set HIGH), the crystal oscillator circuitry remains enabled (in one of four operational states). Also note that setting the RADIOEN bit LOW does NOT cause the loss of calibration information resulting from a CAL command, or loss of the channel tuning information. The default value in WAKEUP mode is RADIOEN=HIGH (synthesizer enabled).
OSCCURR	1	When this bit is set HIGH, the bias current to the crystal oscillator circuitry is increased to support a stronger mode of oscillation. The default value in WAKEUP mode is OSCCURR=HIGH (higher current mode).
OSCOFF	1	When this bit is set HIGH and RADIOEN is set LOW, the crystal oscillator is disabled. When RADIOEN is set HIGH, this bit has no effect. The default value in WAKEUP mode is OSCOFF=LOW (crystal oscillator enabled).
(RESERVED)	1	This bit is reserved by the RFIC. The (RESERVED) bit had functionality in a prior revision of the RFIC but is no longer in use. While this bit does not affect current functionality of the chip, current consumption may be reduced in IDLE mode (by about 30 μA) by always setting this bit HIGH (internally disabling the unused circuitry). The default value in WAKEUP mode is (RESERVED)=LOW. Note that the desired programmed value differs from the default WAKEUP value.
DSLEEP	1	When this bit is set HIGH, the RFIC goes into SLEEP mode after a 10 msec delay. A 1 μsec (minimum) active LOW pulse on the RSTN input pin is required to re-awaken the RFIC. The RFIC awakens to the WAKEUP state.
OSCCAPS[5:0]	6	Allows trimming of the crystal oscillator frequency with symmetric shunt capacitor banks on the XIN and XOUT pins. OSCCAPS[5:0]='000000'= 0 pF, '000001'=282 fF.... '111111'=17.766 pF. The default value in WAKEUP mode is OSCCAPS[5:0]='100000' (9 pF).
FREQ[7:0]	8	Tunes the PLL synthesizer to the desired RF channel in 891.871 kHz increments. RF Ch0(2391.106 MHz)='00000000', Ch1(2391.996 MHz)='00000001'.... Ch10(2400.024 MHz)='00001010' up to Ch116(2494.563 MHz)='01110100'. Attempting to tune Ch117 through Ch255 will result in Ch116. The default value in WAKEUP mode is FREQ='00001010' (RF Ch10=2400.024 MHz).
CAL	1	When this bit is set HIGH, a calibration of the RX Chain and VCO is initiated. The RFIC should be placed in TUNE mode prior to entering CAL mode (that is, RXEN=TXEN=LOW). Calibration is performed off-line and requires approximately 300 μsec. This bit is cleared by the RFIC after completion of the calibration sequence. At the end of the CAL sequence, the following parameters will have been adjusted in this given sequence: VCO1TRIM[4:0], VCO2TRIM[4:0], BPFTRIM[3:0], AFC[5:0], and DMODTRIM[6:0]. It is recommended that the RFIC be placed in the TUNE mode prior to starting a CAL operation. (Other modes of operation, such as TX, RX, or serial programming, are not specifically locked out during a CAL cycle, but the results may not be predictable.) The default value in WAKEUP mode is CAL=LOW (not calibrating).
FASTTC[1:0]	2	Allows selection of the absolute value of the fast time constant of the data slicer. FASTTC[1:0]='00' = 8.5 μsec, FASTTC[1:0]='01' = 17 μsec, FASTTC[1:0]='10' = 25 μsec, and FASTTC[1:0]='11' = 34 μsec. The default value in WAKEUP mode is FASTTC[1:0]='01' = 17 μsec. The state of the TC_CTRL line determines whether the fast or slow time constant is used by the RFIC.

String Name	Bits	Function
SLOWTC[1:0]	2	Allows selection of the absolute value of the slow time constant of the data slicer. SLOWTC[1:0]='00' = 270 µsec, SLOWTC[1:0]='01' = 546 µsec, SLOWTC[1:0]='10' = 820 µsec, and SLOWTC[1:0]='11' = infinite µsec (HOLD mode). The default value in WAKEUP mode is SLOWTC[1:0]='01' = 546 µsec. The state of the TC_CTRL line determines whether the fast or slow time constant is used by the RFIC.
PWRCTR[2:0]	3	Transmit output power control. PWRCTR[2:0]='000'=minimum.....'111'=maximum. The default value in WAKEUP mode is PWRCTR[2:0]='010' (third-lowest transmit power level). Note that the default WAKEUP values of these three bits are also used as Revision ID bits, and may be read back through the SYNOUT function by initiating a read of the PWRCTR[2:0] bits over the serial port. If the RFIC is revised in the future, the default WAKEUP value of these three bits will be modified to PWRCTR[2:0]='011', etc.
IOTEST	1	When set HIGH, this bit causes the RXEN, TXEN, TC_CTRL, and TXMOD input signals to be logically OR'ed together and outputs the result on the SYNOUT output. This is to provide a self-test capability of the non-serial portion of the digital control interface.
BIST	1	Built-In Self Test bit. When set HIGH, this bit initiates a self-test of the Δ-Σ modulator digital circuitry. A known pattern is clocked through the modulator circuitry. After 220 number of PLL1 clock cycles (approximately 10 msec), a cyclic redundancy checksum (CRC) is available at the output of the modulator. This pattern may be read back thru the SYN_OUT function by initiating a READ of the BISTSIG[7:0] bits over the serial port. This bit is cleared by the RFIC after completion of the test sequence.
BISTSHORT	1	Similar to BIST, but initiates a shorter sequence of built-in self test.
BISTDONE	1	This bit is set when the BIST or BISTSHORT sequence has been completed. This flag may be read back thru the SYN_OUT function by initiating a READ over the serial port.
EXTCLKSEL	1	In normal operation, the Built-In Self Test (BIST) circuitry derives its clock from the PLL1 VCO. This allows test of the digital circuitry at high speed, but requires the analog PLL1 block to be functioning. When this bit is set HIGH, the clock source for the BIST circuitry is switched to the crystal oscillator reference clock. This allows test of the digital circuitry in an "all-digital" mode. The default value in WAKEUP mode is EXTCLKSEL=LOW (clock selected from PLL1 VCO).
ATBSEL[3:0]	4	Analog Test Bus Select bits. Determines which of 16 pairs of internal test points are muxed onto the TESTP and TESTN output pins. Refer to Table 5 to determine the mapping of ATBSEL[3:0] to the selected internal test point. Note that most of the internal test points are connected to the TESTP and TESTN output pins without buffering. The sole exception is the Slicer Reference Voltage ATBSEL[3:0]='1100'. The default value in WAKEUP mode is ATBSEL[3:0]='0000' (RX IF Ground).
MODDIVLOW	1	In normal operation, the modulus of the 18/20 prescaler in the PLL2 synthesizer is dithered by the Δ-Σ modulator in such a pattern as to obtain the desired average output frequency. Setting this bit HIGH forces the divider modulus to continuously diivde-by-18 (for diagnostic purposes). The default value in WAKEUP mode is MODDIVLOW=LOW (normal automatic modulus control).
DITHPROG[2:0]	3	These three bits select a dithering factor that is used to further "whiten" the spectrum of the quantization noise resulting from operation of the Δ-Σ modulator. The default value in WAKEUP mode is DITHPROG[2:0]='000'.
RESPROG[1:0]	2	These two bits adjust the location of the transmission zero in the digital filter transfer function in the Δ-Σ modulator. It may be advantageous to modify this resonator zero to optimize the spectrum of the quantization noise that falls in-band. The default value in WAKEUP mode is RESPROG[1:0]='00'.
GAINTRIM[4:0]	5	These five bits represent the trim setting for the two-point modulation DAC gain as a result of performing a CAL operation, and may be read back thru the SYN_OUT function by initiating a READ over the serial port. The value of trim setting may also be manually controlled by setting the DAC Gain override bit (GAINOVER) and then manually writing the desired value of GAINTRIM[4:0].
GAINOVER	1	Two-point modulation DAC gain trim calibration override bit. When set HIGH, the value of the GAINTRIM[4:0] bits may be written to manually.

String Name	Bits	Function
WIDEBAND	1	In normal operation, the PLL2 synthesizer is briefly placed into a wide loop bandwidth mode whenever the FREQ[7:0] word is changed. After the PLL2 synthesizer has quickly settled to its new frequency in wideband mode, the loop filter automatically reverts back to a narrower loop bandwidth to improve phase noise performance over the remainder of the frame. Setting this bit HIGH forces the loop filter to continuously operate in wide bandwidth mode (for diagnostic purposes). The default value in WAKEUP mode is WIDEBAND=LOW (normal automatic loop bandwidth control).
INVDOUT	1	Setting this bit HIGH causes the sliced output data on the RXDATA output pin to be inverted. The default value in WAKEUP mode is INVDOUT=LOW (non-inverted data output).
INVDIN	1	Setting this bit HIGH causes the TX modulation input data on the TXMOD pin to be inverted before modulation onto the TX signal. The default value in WAKEUP mode is INVDIN=LOW (non-inverted modulation).
DMODTRIM[6:0]	7	These 7 bits represent the trim setting for the period of the FM demodulator one-shots as a result of performing a CAL operation, and may be read back thru the SYN_OUT function by initiating a READ over the serial port. The trim value may also be manually controlled by setting the demodulator trim override bit (DMODOVER) and then manually writing the desired value of DMODTRIM[6:0].
VCO1OVER	1	VCO for PLL1 trim calibration override bit. When set HIGH, the value of the VCO1TRIM[4:0] bits may be written to manually. The default value in WAKEUP mode is VCO1OVER=LOW (VCO1TRIM bits not over-ridden).
VCO1TRIM[4:0]	5	These five bits represent the trim setting for the PLL1 VCO as a result of performing a CAL operation, and may be read back thru the SYN_OUT function by initiating a READ over the serial port. The value of trim setting may also be manually controlled by setting the VCO1 override bit (VCO1OVER) and then manually writing the desired value of VCO1TRIM[4:0].
VCO2OVER	1	VCO for PLL2 trim calibration override bit. When set HIGH, the value of the VCO2TRIM[4:0] bits may be written to manually. The default value in WAKEUP mode is VCO2OVER=LOW (VCO2TRIM bits not over-ridden).
VCO2TRIM[4:0]	5	These five bits represent the trim setting for the 2.4 GHz VCO of PLL2 as a result of performing a CAL operation, and may be read back thru the SYN_OUT function by initiating a READ over the serial port. The value of trim setting may also be manually controlled by setting the VCO2 override bit (VCO2OVER) and then manually writing the desired value of VCO2TRIM[4:0].
AFC[5:0]	6	These six bits represent the residual frequency error of the IF bandpass filter as a result of performing a CAL operation, and are used to offset the frequency of the PLL synthesizer in RX mode in order to remove this error (Automatic Frequency Control). The value of these bits may be read back thru the SYN_OUT function by initiating a READ over the serial port. The value of PLL automatic frequency control offset may also be manually controlled by setting the bandpass filter override bit (BPFOVER) and then manually writing the desired value of AFC[5:0]. Note that these 6 bits comprise a signed 5-bit control word. Values 0-31 increase the frequency of the PLL synthesizer (and thus decrease the observed IF frequency as low-side injection is used), while values 32-63 decrease the frequency of the PLL synthesizer. The resolution of the AFC control word is in increments of 3.95 kHz, for a total RX AFC adjustment range of ±122.5 kHz.
SLOWRAMP	1	This bit controls the delay between the falling edge of TXEN and the falling edge of an internal PA_RAMP signal. Setting this bit HIGH delays the final shutoff of the ramp-down signal by an extra 8 µsec. The default value in WAKEUP mode is SLOWRAMP=LOW (fast ramp down).
BPFOVER	1	Bandpass filter calibration override bit. When set HIGH, the value of the BPFTRIM[3:0] and AFC[5:0] bits may be written to manually. The default value in WAKEUP mode is BPFOVER=LOW (BPFTRIM and AFC bits not over-ridden).
BPFTRIM[3:0]	4	These four bits represent the coarse trim setting for the IF BPF as a result of performing a CAL operation, and may be read back thru the SYN_OUT function by initiating a READ over the serial port. The value of coarse trim capacitance may also be manually controlled by setting the bandpass filter override bit (BPFOVER) and then manually writing the desired value of BPFTRIM[3:0].

String Name	Bits	Function
RXOFST[6:0]	7	These seven bits are used to offset the frequency of the PLL2 synthesizer in RX mode. This offset is added to that specified by the AFC[5:0] word. This provides the ability to tune the IF signal at positions other than the center of the IF bandpass filter. Note that these seven bits comprise a signed 6-bit control word. Values 0-63 increase the frequency of the PLL2 synthesizer (and thus decrease the observed IF frequency as low-side injection is used), while values 64-127 decrease the frequency of the PLL2 synthesizer. The resolution of the RXOFST control word is in increments of 3.95 kHz, for a total RX offset adjustment range of ±248.9 kHz. The default value in WAKEUP mode is RXOFST[6:0]='000 0000'=0 kHz offset. Note that this register is "shared" with the BISTSIG[7:0] word. The lower seven bits (RXOFST[6:0]) may be written to at any time. However, the serial read back functionality is controlled by the most recent WRITE to the most significant data bit. If the most recent WRITE to D7 is a logic '0', the RXOFST[6:0] word is read back. If the most recent WRITE to D7 is a logic '1', the BISTSIG[7:0] word is read back.
BISTSIG[7:0]	8	These bits are the resulting 8-bit signature of the built-in self-test sequence applied to the Δ-Σ modulator digital circuitry. The self-test sequence is typically initiated by setting the BIST bit HIGH, and then reading this signature (**TBD**) clock cycles later for verification.

Table 5. Analog Test Bus Select Mapping

ATBSEL[3:0]	TESTP	TESTN
'0000'	RX IF Ground	RX IF Ground
'0001'	RX IRM Out+	RX IRM Out-
'0010'	RX BPF Out+	RX BPF Out-
'0011'	RX BPF OpAmp Clamp HI Level	RX BPF OpAmp Clamp LO Level
'0100'	RX BPF Common Mode Voltage	RX BPF Ground
'0101'	RX BPF BiQuad2 Out+	RX BPF BiQuad2 Out-
'0110'	LimRSSI BG Voltage Copy	RSSI Voltage
'0111'	Demod Input+	Demod Input-
'1000'	Demod Pulse Out+	Demod Pulse Out-
'1001'	Demod Data LPF Out+	Demod Data LPF Out-
'1010'	Demod DAC Output	Demod Ground
'1011'	PLL1 125uA RPOLY Bias Source	PLL1 25uA REXT Bias Sink
'1100'	Slicer Ref Voltage+	Slicer Ref Voltage-
'1101'	PLL1 Loop Filter Tap	PLL1 Ground
'1110'	PLL2 Power	PLL2 ChPump 5uA RPOLY Bias Sink
'1111'	PLL2 VCO Control	PLL2 Ground

Power-Up, DSLEEP and WAKEUP States

The RSTN line should be held LOW while V_{CC} is initially applied to the RFIC to force the device to transition to the WAKEUP mode. The RSTN line should be held in a LOW state until the V_{CC} supply and clock input signal are stable. Alternatively, a single active-LOW pulse may be applied to the RSTN line for a minimum of 1 µsec at any time after power-up to also enter the WAKEUP state. Such a pulse is also required to arouse the RFIC from the Deep Sleep (DSLEEP) mode. In DSLEEP mode, all functions of the chip are shut down and the current consumption is reduced to an absolute minimum. The chip is placed into DSLEEP mode by programming the DSLEEP bit HIGH. The Cordless Telephone unit (Base or Handset) is typically placed into DSLEEP mode at the factory to allow shipment with a fully charged battery pack already connected to the unit. Thus the active-low RSTN pulse provides a means for removing the unit from the DSLEEP mode when the end user operates the unit for the very first time. When the DSLEEP bit is set HIGH, the chip enters the DSLEEP mode after a 10 msec delay. This delay allows a sufficient period of time for the BBIC to shut itself down gracefully in the event it is also deriving its clock from the internal crystal oscillator of the RFIC.

In the Base unit, an external circuit block typically generates the RSTN pulse when the AC wall adapter is first plugged in and V_{CC} is provided to the RFIC. When a Handset unit is placed in DSLEEP Mode while V_{CC} is still applied (i.e. in the production line), an external RSTN signal is usually generated by placement of the Handset unit in the cradle.

In the event the BBIC derives its clock from the internal crystal oscillator of the RFIC, the length of the RSTN pulse must be increased to approximately 10 msec to allow the amplitude of oscillation of the built-in 13.824 MHz crystal oscillator to build to its full amplitude (see Figure 10).

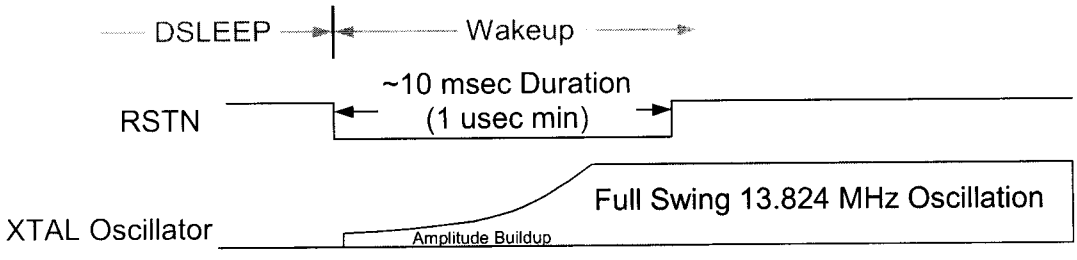


Figure 10. DSLEEP Mode to WAKEUP Mode Transition

When the RFIC transitions into the WAKEUP mode via the RSTN pulse, some circuitry is enabled to the ON state while other circuitry remains disabled. (This is only sensible, as it would not be desirable to wake the chip up with the transmitter enabled at full power at an unknown frequency.) The intent of the WAKEUP mode is to provide a known initial state from which the chip can be programmed to the desired frequency and mode of operation. The state of the various functional circuit blocks in both the DSLEEP and WAKEUP modes is depicted in Table 6 below. (Refer to Table 4 *Serial Control Bit Definition* for the state of the various serial control registers after WAKEUP). Note that although a default WAKEUP value for the FREQ[7:0] control word is provided, proper operation of the PLL synthesizer is not guaranteed until after a CAL command has been executed.

Table 6. DSLEEP and WAKEUP Modes

Pin/Bit	DSLEEP	WAKEUP
DSLEEP bit	High	Low
OSCCURR bit	X	High
OSCOFF bit	X	Low
RADIOEN bit	X	High
TXEN pin	X	Low
RXEN pin	X	Low
Circuit Block		
XTAL Oscillator	Off	On
Serial Logic Interface	Off	On
Synthesizer	Off	On
Rx/Tx Chain	Off	Off

WAKEUP is the RFIC state after RSTN is pulsed LOW.

Note: X implies don't care.

Managing STANDBY, IDLE, and ACTIVE Operational Modes

After the RFIC has been brought into the WAKEUP state, it is ready to be programmed. In normal usage there are three main operational modes of the chip: STANDBY mode, IDLE mode, and ACTIVE mode. The ACTIVE mode is used for normal transmit and receive functionality. The STANDBY and IDLE modes are both reduced-current modes that differ slightly in the amount of internal circuitry that is disabled. The use of either the STANDBY or IDLE mode is usually dictated by the crystal oscillator clock distribution scheme used in the system. There are three possible clock distribution schemes:

- The RFIC and BBIC each have their own separate internal crystal clock oscillators. A crystal blank is placed between the XIN and XOUT pins of the RFIC as shown in Figure 7.
- The RFIC derives its clock input signal from the crystal oscillator of the BBIC. The RFIC accepts the external clock signal on its XIN pin and buffers it for internal use.
- The BBIC derives its clock input signal from the crystal oscillator of the RFIC. Again, a crystal blank is placed between the XIN and XOUT pins of the RFIC as shown in Figure 7. The BBIC taps off the analog signal available at the XIN or XOUT pin and buffers it prior to use.

Further description of the operational modes and clock distribution schemes is provided below. The state of various circuit blocks as a function of operational mode (STANDBY, IDLE, or ACTIVE) is depicted in Table 7 below.

STANDBY Mode

In STANDBY mode, nearly all of the functions of the chip (including the internal crystal oscillator) are disabled in order to reduce current consumption to the absolute minimum possible level. The Serial Control Interface is the only circuit that remains active (to provide an exit from the STANDBY mode by programming the appropriate control register). As the Serial Control Interface is not typically clocked by the BBIC during STANDBY mode, the static current consumption of the RFIC is very low (< 1μA). Setting the RADIOEN bit LOW and the OSCOFF bit HIGH enters STANDBY mode. Entering the STANDBY mode does NOT cause loss of control register programming or CAL information; the prior state of the RFIC is recalled when the STANDBY mode is exited.

STANDBY mode is typically entered in a Handset unit when the link is not currently active, and relatively long periods of inactivity are expected. A typical Cordless Telephone software algorithm may briefly bring the Handset unit out of STANDBY mode to ACTIVE mode in order to scan the channels for an incoming call, and then return the unit to STANDBY mode if no activity is detected. STANDBY mode differs from DSLEEP mode in that the STANDBY mode may be exited by simply re-programming the RADIOEN and/or OSCOFF bits; DSLEEP mode may only be exited by application of an active low pulse on the RSTN pin. (However, it should be noted that exactly the same current consumption is realized in either STANDBY mode or DSLEEP mode, as the same internal circuitry is powered down.)

Use of the STANDBY mode is only possible when the BBIC does NOT derive its clock from the crystal oscillator of the RFIC, as the crystal oscillator is disabled in STANDBY mode.

IDLE Mode

IDLE mode is very similar to STANDBY mode with the exception that the internal crystal oscillator remains enabled. As a result, the current consumption is not as low as in STANDBY mode. Setting both the RADIOEN and OSCOFF bits LOW enters IDLE mode. Again, entering the IDLE mode does NOT cause loss of control register programming or CAL information; the prior state of the RFIC is recalled when the IDLE mode is exited.

IDLE mode is typically used when the 13.824 MHz crystal oscillator internal to the RFIC is the only oscillator in the system, and the clock required by the BBIC is derived by buffering the analog signal available at the XIN or XOUT pin(s).

Use of the IDLE mode may be appropriate even when the RFIC and the BBIC each have their own separate crystal clock oscillators. Although the crystal oscillator need not remain enabled in this configuration and use of the STANDBY mode would achieve a lower level of current consumption, it should be remembered that it might take a significant amount of time (several msec) for the crystal oscillator to turn back on and reach its full amplitude of oscillation due to the high-Q of the crystal blank. Thus use of the STANDBY mode may not be appropriate when rapid power-on times are required.

The OSCCURR bit may also be set HIGH or LOW as desired to increase the bias current to the crystal oscillator circuitry. A higher level of bias current may be necessary to support oscillation with some crystal blanks.

ACTIVE Mode(s)

In ACTIVE mode, all of the normal transmit and receive functions of the RFIC are available. Setting the RADIOEN bit HIGH enters ACTIVE mode. Operation within the ACTIVE mode is achieved by controlling the TXEN and RXEN pins as desired.

The internal crystal oscillator circuitry is continuously enabled in ACTIVE mode. Again, the OSCCURR bit may be set HIGH or LOW as desired to support a stronger mode of oscillation with some crystal blanks.

Table 7. STANDBY, IDLE and ACTIVE Modes

	XTAL Oscillator Configuration								
	RFIC generates System Clock			RFIC and BBIC have separate Clocks			BBIC generates System Clock		
Pin/Bit	**STANDBY**	**IDLE**	**ACTIVE**	**STANDBY**	**IDLE**	**ACTIVE**	**STANDBY**	**IDLE**	**ACTIVE**
DSLEEP bit	N/A	Low	Low	Low	Low	Low	Low	N/A	Low
OSCCURR bit	N/A	As Req	As Req	X	As Req	As Req	X	N/A	As Req
OSCOFF bit	N/A	Low	Low	High	H/L	High	High	N/A	Low
RADIOEN bit	N/A	Low	High	Low	Low	High	Low	N/A	High
TXEN pin	N/A	Low	Active	Low	Low	Active	Low	N/A	Active
RXEN pin	N/A	Low	Active	Low	Low	Active	Low	N/A	Active
Circuit Block									
XTAL Oscillator	N/A	On	On	Off	On	On	Off	N/A	On
Serial Logic Intfc	N/A	On	On	On	On	On	On	N/A	On
Synthesizer	N/A	Off	On	Off	Off	On	Off	N/A	On
Rx/Tx Chain	N/A	Off	Active	Off	Off	Active	Off	N/A	Active

Note: X implies don't care. N/A is a mode that is Not Applicable.

Operation of the RFIC within an ACTIVE mode is further determined by the state of the TXEN, RXEN and TC_CTRL pins as well as the PWRCTR[2:0] bits as shown in Table 8. The chip is placed into TX mode by setting the TXEN pin HIGH. The transmit output level is subsequently determined by the PWRCTR[2:0] bits. The chip is placed into RX mode by setting the RXEN pin HIGH. This enables the LNA, RX image-reject mixer, IF chain, and demodulator/slicer circuitry.

If neither the TXEN nor RXEN pins are set HIGH, the chip is considered to be in the TUNE mode. The TUNE mode is the transceiver at the onset of any Rx or Tx Slot. Quite often, a new channel is commanded and the gap time is used to allow the PLL synthesizer to settle to the new frequency. The TUNE mode is the default power-up state of the chip if the DSLEEP bit is not set.

Simultaneous transmit and receive (both TXEN and RXEN HIGH at the same time) is not considered to be a valid state.

Table 8. ACTIVE Mode Detail

	ACTIVE Modes				
Pin/Bit	**TUNE**	**RX_SLOW**	**RX_FAST**	**TX_HIGH Power**	**TX_LOW Power**
RADIOEN bit	High	High	High	High	High
TXEN pin	Low	Low	Low	High	High
RXEN pin	Low	High	High	Low	Low
TC_CTRL pin	X	Low	High	Low	Low
PWRCTR bits	X	X	X	'111'	'000'
Circuit Block					
Synthesizer	On	On	On	On	On
RX Chain	Off	On	On	Off	Off
Slicer	Off	Slow Track	Fast Track	Off	Off
TX Chain	Off	Off	Off	On (Full Power)	On (Low Power)

APPLICATION NOTES

Application Overview

The typical Application Circuit for the RF Module can be implemented on a 2-layer circuit board that is mounted on the main board. Upon request, DSPG can supply a reference design based on a Bill of Materials, shown below (includes a total of 42 components).

- 0402 capacitor and resistors: 30pcs
- 0402 inductors: 6pcs
- 10uF Tantalum: 2pcs
- L-C RF BPF: 1pc.
- RF SC-70 package PIN Diode: 1pc.
- 13.824 MHz Crystal: 1pc.
- RFIC: DH24RF17B

Application Schematic

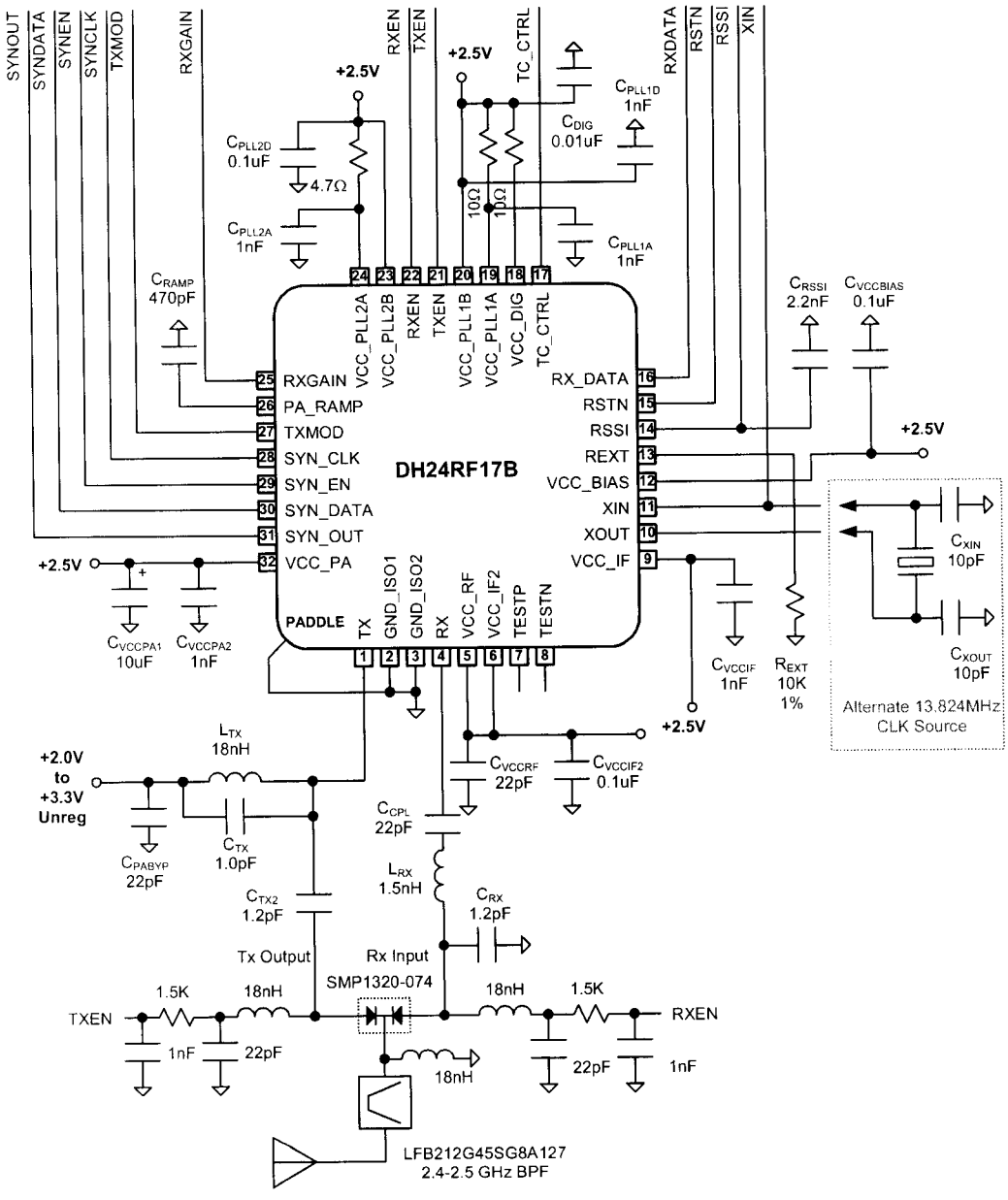


Figure 11. Application Schematic

RFIC/BBIC Interconnect Wiring

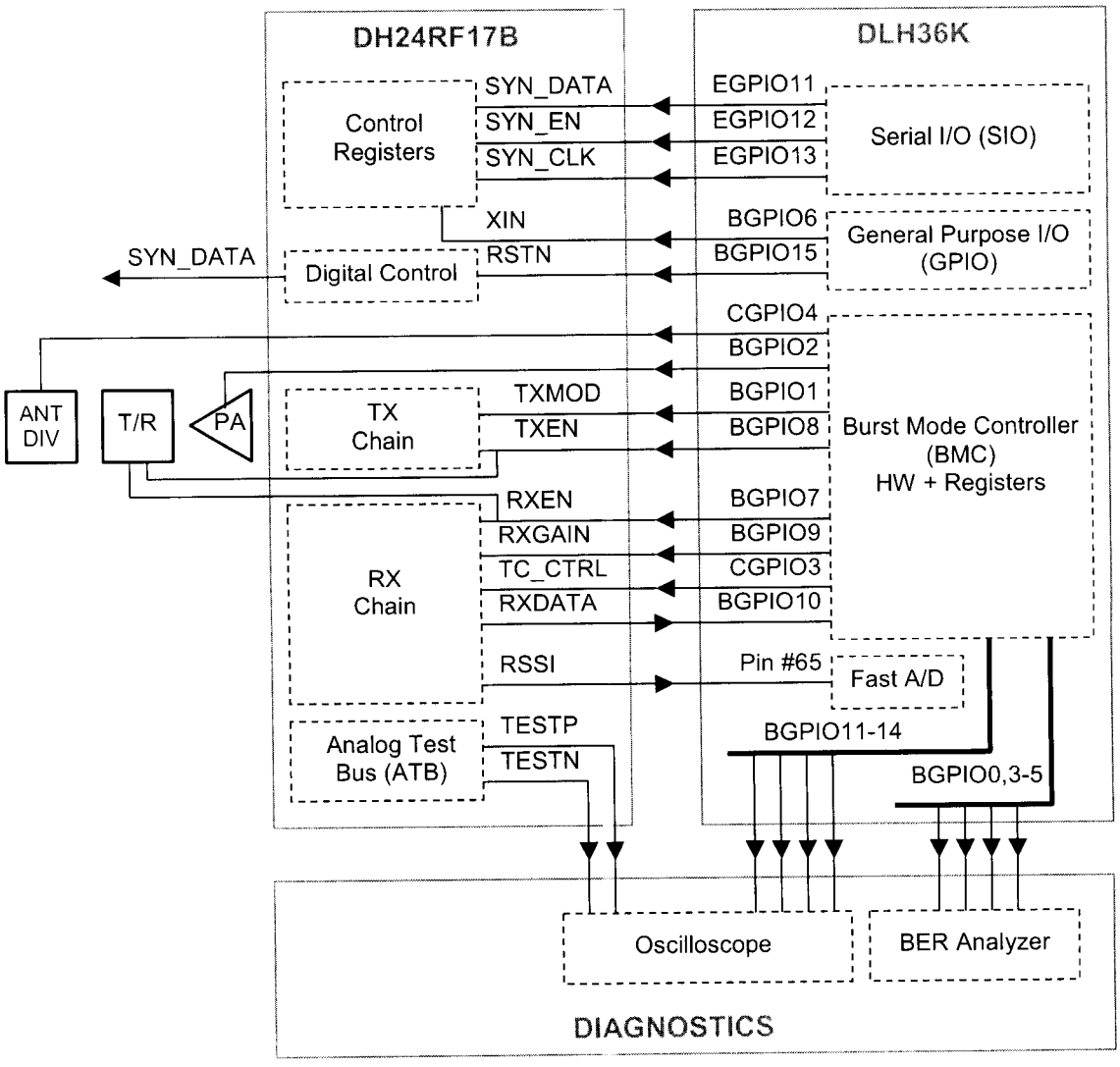


Figure 12. RFIC\BBIC Interconnection Diagram

Bit Error Rate (BER) Testing

The measured BER performance of an RF module based upon the Application Schematic of Figure 11 is shown in Figure 36. Note that the BER performance shown is obtained with approximately 3 dB of insertion loss (due to the T/R switch and preselector bandpass filter) prior to the RFIC. The Test Setup of Figure 13 was used to measure the BER performance.

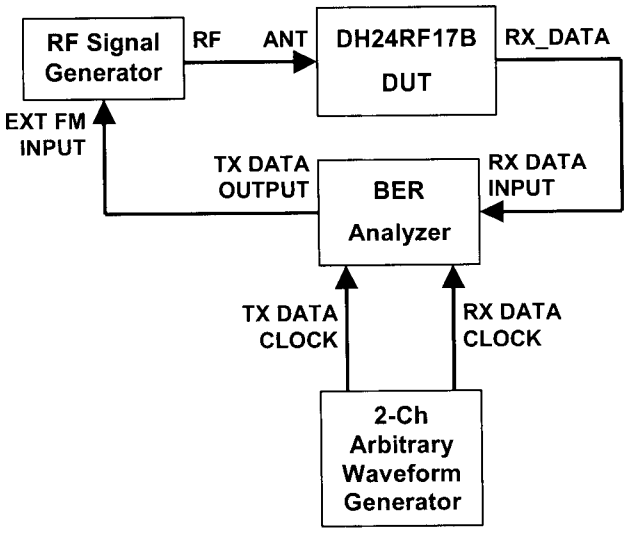


Figure 13. BER Test Setup

A 2-Channel Arbitrary Waveform Generator was used to create two 576 kbps clock signals. The first clock signal was used as the TX DATA CLOCK. Each negative edge transition of the TX DATA CLOCK signal causes the BER Analyzer to output another pseudo-random data bit on its TX DATA OUTPUT line. This is shown in Figure 14. This TX DATA OUTPUT signal is used to FSK-modulate an RF signal generator and applied to the antenna input of the DUT. The resulting demodulated and sliced data is available at the RX_DATA output of the DUT, shifted in time by the group delay of the RF module. Each positive transition of the RX DATA CLOCK signal clocks in another bit into the RX DATA INPUT of the BER Analyzer. The relative phase of the TX & RX DATA CLOCKS are manually adjusted to obtain the optimum BER. The optimum RX sampling point occurs at the center of the RX data eye pattern.

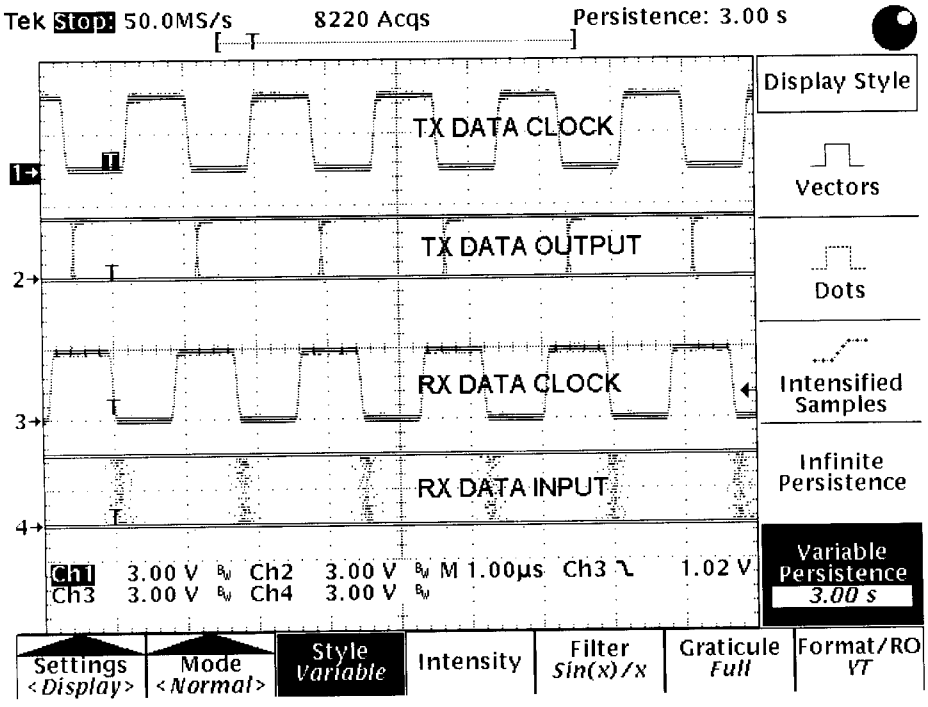


Figure 14. BER Clock & Data Signals

EDCT Time Division Duplex Protocol

The chip is intended for use in systems utilizing Time Division Duplexing (TDD), in which the transceiver alternately transmits and receives in a burst-like nature. Because the transmitter and receiver are never on at the same time, it is possible to use a single local oscillator (LO) for both transmit and receive modes. This is done by quickly shifting the LO frequency in the gap time between the transmit and receive bursts. Thus it is necessary to precisely control the timing of the serial interface (which programs the frequency of the chip) as well as the TX/RX mode signals (TXEN, RXEN, etc.).

The actual software protocol and TDD frame timing may vary from application to application. However, the RFIC has been optimized and extensively tested for use in a protocol with a 576 kbps data rate and a 10 msec EDCT TDD frame structure, consisting of four 1.25 msec Portable Part (PP) to Fixed Part (FP) Uplink slots, followed by four 1.25 msec FP-to-PP Downlink slots. The timing discussed in the following section is typical of this protocol. An overview of the timing of the frame structure is shown in Figure 15 below.

This EDCT protocol supports simultaneous operation of up to 4 handsets. Note that the uplink and downlink slots occur in pairs (i.e., slots a-A, slots b-B) spaced apart by 5 msec. The frequencies used by the 4 handsets in any given frame may be different (as shown by FREQ1-4), but will be the same in both the uplink and downlink slot of a particular frame. If a frequency hopping protocol is used, the frequencies will likely change in the subsequent frame (K+1) as shown by FREQ5-6, etc.

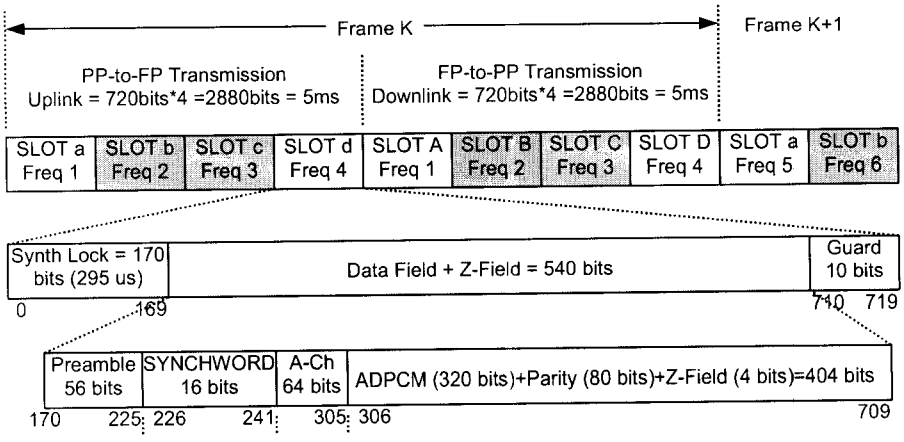


Figure 15. Frame Structure

The timing within a PP-to-FP uplink slot (RX slot as viewed by the FP) is shown in Figure 16. TXEN is set LOW simultaneously after the final data bit of a TX slot. The PLL synthesizer is reprogrammed at this time to shift to the receive LO frequency (e.g., F_{SLOT-D}). The desired receive frequency is programmed over the serial interface by sending the FREQ[7:0] word or just the word containing the OFFSET bit. Each serial control word consists of 4 bits of address header, followed by 8 bits of data and clock, followed by a Synthesizer Enable (EN) pulse. The serial interface is capable of operating at clock and data rates up to 7.5 MHz, so the length of time required to program 24 bits of information (the FREQ word and the OFFSET word) is relatively small (less than 5 µsec).

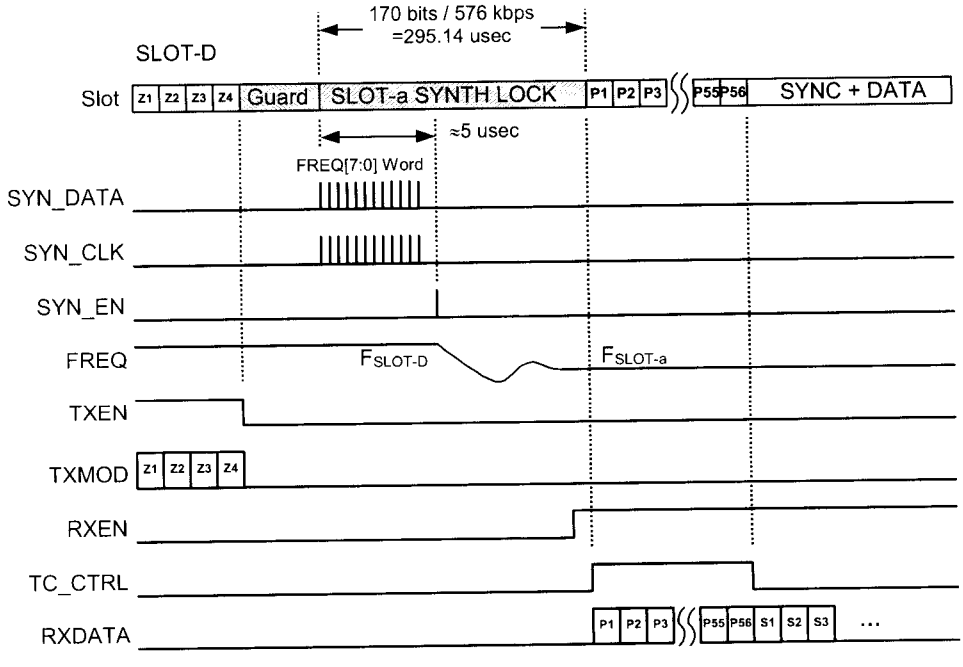


Figure 16. Serial Programming for a PP-to-FP Uplink (FP RX) Slot

RXEN is set HIGH at (or near) the beginning of the preamble of the received data. This allows the receiver chain sufficient time to turn on and settle any transients through the narrow bandwidth IF filters. TC_CTRL is asserted HIGH at the start of the preamble. The data slicer quickly acquires the appropriate slicing level during reception of the preamble. The TC_CTRL line is set back to a LOW state at the end of the preamble, thus allowing the slicing reference level to track slow variations in the received data for the remainder of the RX slot. The actual values of the fast and slow data slicer time constants are set by the FASTTC[1:0] and SLOWTC[1:0] words in the serial control stream. The RXDATA output is active regardless of the state of the TC_CTRL line, but is held at a logic LOW output level when RXEN is also set LOW. The relative timing of various signals during an RX sub-frame is shown in Figure 17.

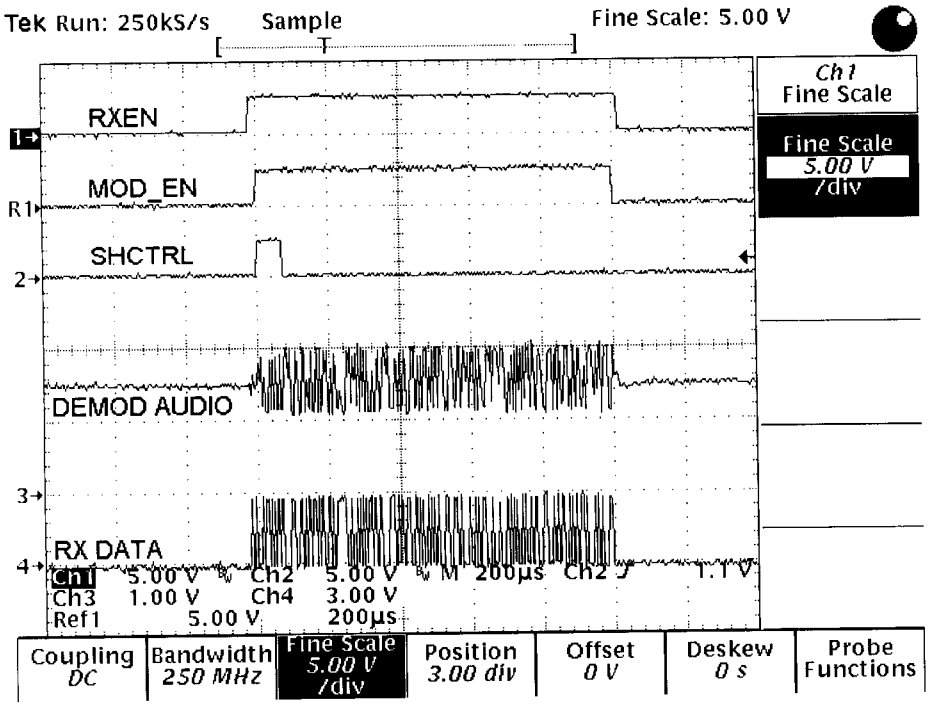


Figure 17. RX Sub-Frame Timing (NEEDS UPDATING!)

The timing within a FP-to-PP downlink slot (TX slot as viewed by the FP) is shown in Figure 18. After the FREQ[7:0] word has been programmed, the PLL2 synthesizer will begin to settle to its new frequency (e.g., F_{SLOT-A}). The amount of settling time required will be a function of the frequency step size and the PLL2 loop bandwidth. The loop filter integrated inside the RFIC is set to yield a nominal loop bandwidth of approximately 45 kHz. However, during a frequency hop to a new channel the loop bandwidth is briefly commanded to a wider bandwidth in order to meet the fast settling time requirements of the frequency hopping protocol. This combination is sufficient to tune anywhere within the 2.40-2.483 GHz ISM band in less than 220 µsec. In the frame structure shown in Figure 15, the synthesizer lock time between adjacent slots is only 170 bits. The recommended EDCT protocol uses the preamble bits (immediately after the synthesizer lock time) for the purpose of Antenna Diversity Selection. These preamble bits are important for proper operation of the system and are not available for "extra" synthesizer settling time. As a result, the upper bound on available synthesizer settling time is 295 µsec (170 bits at 576 kbps = 295.14 µsec).

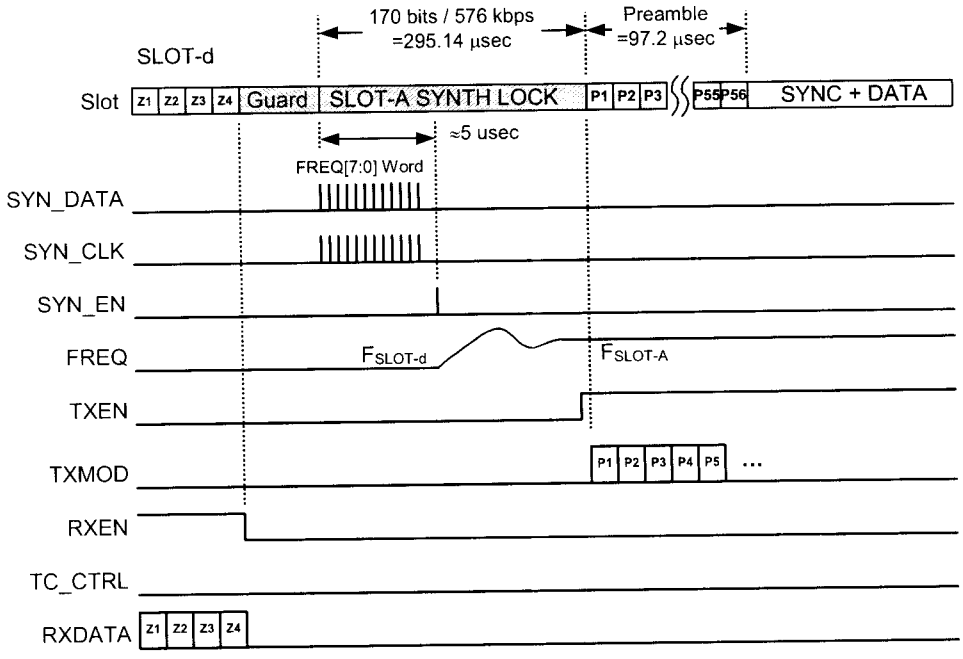


Figure 18. Serial Programming for a FP-to-PP Downlink (FP TX) Slot

All control lines should be held LOW during the synthesizer lock time, as it is not desirable to enable the transmitter while the synthesizer frequency is still settling to its final value. The TXEN line may be set HIGH (thus turning on the transmitter) shortly before the end of the settling process. This allows any small RX/TX switching transient to be absorbed into the final few µsec of the frequency settling process.

The TX modulation applied to the TXMOD pin should be held at a constant value during the non-TX portion of the frame. When tuning to a new channel, the synthesizer will settle to the commanded channel's center frequency plus the deviation indicated by the state of the TXMOD line. If the TXMOD pin is held at (for example) a logic LOW during the synthesizer settling time, the synthesizer will settle to ΔF_{MOD} kHz below the commanded channel's center frequency. Subsequently changing the TXMOD line to a logic HIGH will result in a $+2*\Delta F_{MOD}$ kHz increase in the output frequency (i.e., twice the peak deviation).

PCB Layout Notes

As one might expect when working with an RFIC at 2.4 GHZ, proper layout of the printed circuit board (PCB) is very important to obtaining good performance. It is absolutely essential that the PCB incorporate a solid ground plane underneath the entire RFIC and surrounding circuitry. Unused board areas on the component side should be filled with ground plane. Furthermore, ground plane areas on the component side should be connected to the ground plane on the bottom side with numerous through-hole vias. This is especially true in the area directly beneath the RFIC, as the majority of the RF grounds of the chip are obtained through the exposed metal paddle on the bottom side of the package. This is shown in Figure 19. Note that in order to guarantee a good electrical connection to the ground paddle, solder re-flow assembly techniques should be used. Excessive soldering temperatures should be avoided during the re-flow assembly process, as the thermal conductivity of the package is quite high (due to the short lead lengths) and damage to the internal bond wires may result. The recommended infra-red reflow profile is shown later in this data sheet.

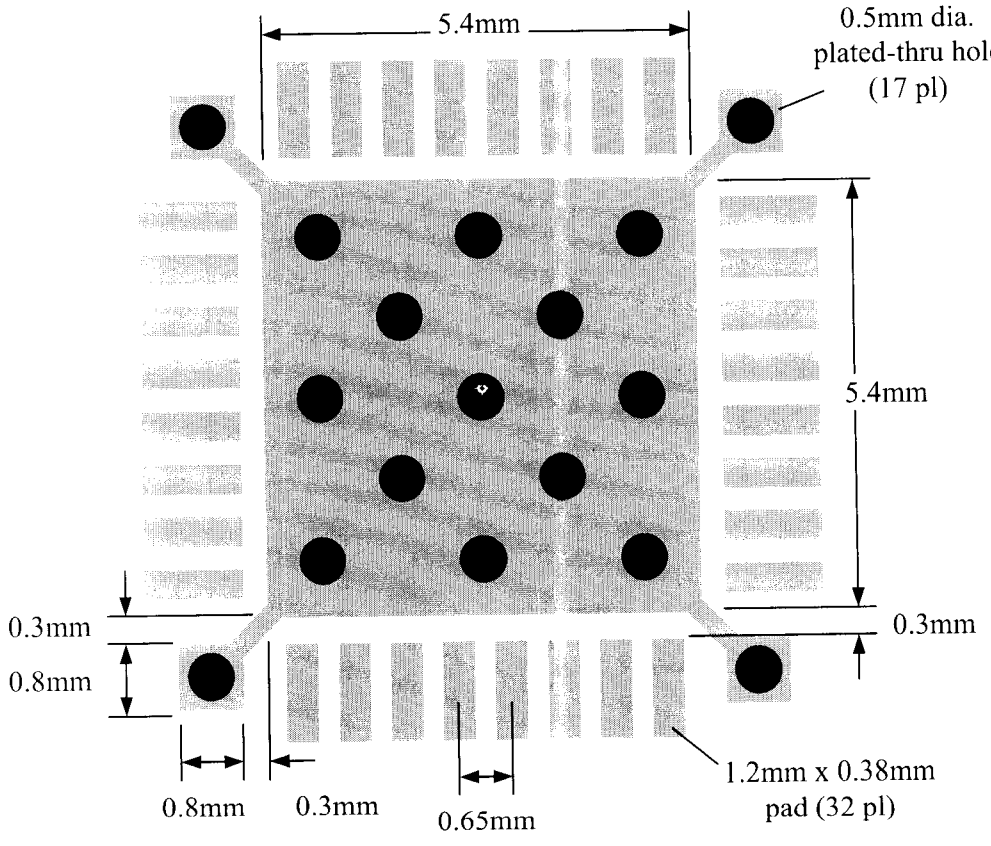


Figure 19. Recommended PCB Footprint

PRODUCTION TEST SCHEMATIC

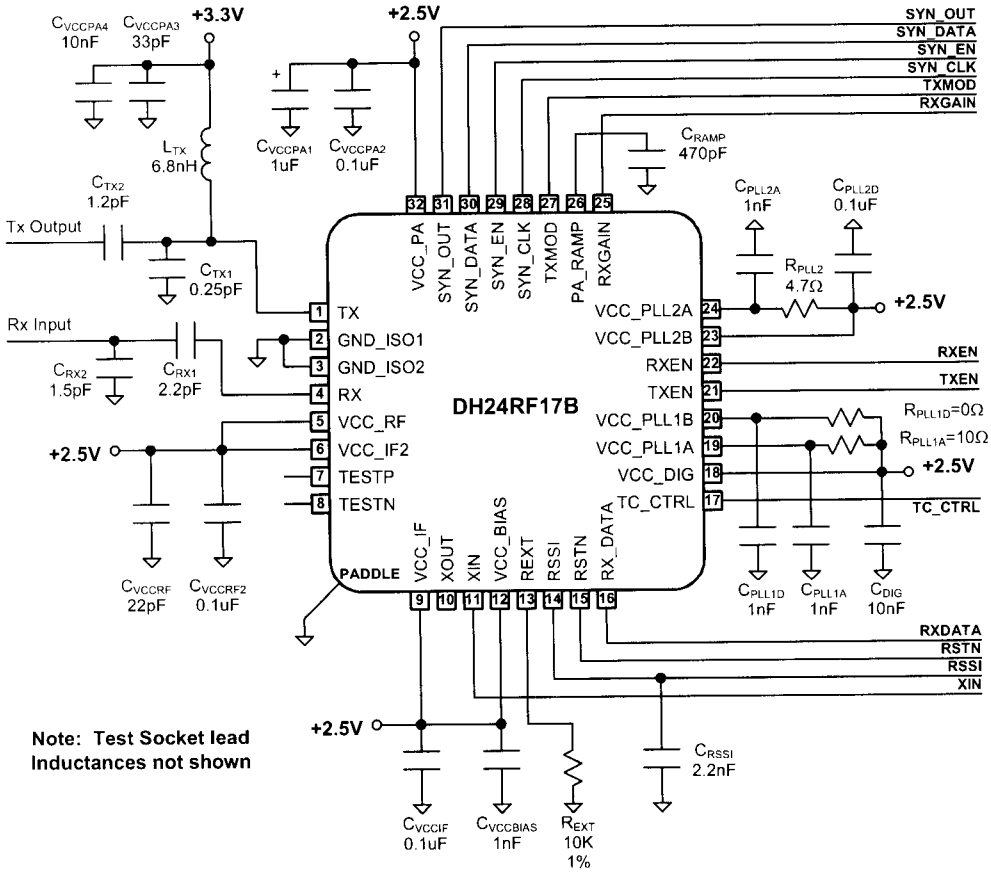


Figure 20. Production Test Schematic

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND: ..... –0.3 V, +3.5 V

Voltage on Digital Control Inputs: ..... –0.3 V, +3.5 V

Voltage on Analog Inputs: ..... –0.3 V, V_{CC} + 0.3 V

TX Output ..... –0.3 V, +4.6 V

RX Input Power: ..... +10 dBm

Thermal Impedance Θ_{JA} ..... 25.4 °C/W

Operating Ambient Temperature Range T_A: ..... 0°C to +70°C

Operating Junction Temperature T_J: ..... +125°C

Storage Temperature Range T_{STG}: ..... –40°C to +150°C

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.

DC CHARACTERISTICS

V_{CC} = +2.5V (unless specified otherwise), T_A = +25°C, no RF signals applied.
External reference signal (XIN) = 0.7 Vpp (unless noted otherwise) at 13.824MHz.
Production test schematic of Figure 20, unless noted otherwise.

Table 9. DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{CC}	All V_{CC} pins	2.25	2.5	2.75	V
Digital Input Voltage High (1)	V_{IH}	RXEN, TXEN, TC_CTRL, SYN_CLK, SYN_DATA, SYN_EN, TXMOD, RSTN	2.0			V
Digital Input Voltage Low (1)	V_{IL}	RXEN, TXEN, TC_CTRL, SYN_CLK, SYN_DATA, SYN_EN, TXMOD, RSTN			0.8	V
Digital Input Current High (1)	I_{IH}	RXEN, TXEN, TC_CTRL, SYN_CLK, SYN_DATA, SYN_EN, TXMOD, RSTN = V_{CC}			1	µA
Digital Input Current Low (1)	I_{IL}	RXEN, TXEN, TC_CTRL, SYN_CLK, SYN_DATA, SYN_EN, TXMOD, RSTN = 0V			1	µA
DSLEEP Mode Current (3)	$I_{dd\text{-}DSLEEP}$	DSLEEP bit = HIGH XIN = 0V		1	5	µA
STANDBY Mode Current (3)	$I_{dd\text{-}STDBY}$	DSLEEP, RADIOEN bits = LOW OSCOFF bit = HIGH XIN = 0V		1	5	µA
IDLE Mode Current (3)	$I_{dd\text{-}IDLE}$	DSLEEP, RADIOEN bits = LOW OSCOFF bit = LOW OSCCURR bit = HIGH (RESERVED) = HIGH		650	750	µA
TUNE Mode Current (3)	$I_{dd\text{-}TUNE}$	DSLEEP bit = LOW RADIOEN bit = HIGH OFFSET bit = LOW TXEN, RXEN = 0V	39	47	55	mA
RX Mode Current (3)	$I_{dd\text{-}RX}$	DSLEEP bit = LOW RADIOEN, OFFSET bits = HIGH TXEN = 0V, RXEN = V_{CC}	63	75	87	mA
TX Mode Current(s) (3) (All VCC pins but excluding the TX output pin 1)	$I_{CC\text{-}TX\text{-}HIGH}$	DSLEEP bit = LOW RADIOEN bit = HIGH PWRCTR = '111' TXEN = V_{CC}, RXEN = 0V	75 **TBD**	85 **TBD**	95 **TBD**	mA
	$I_{CC\text{-}TX\text{-}LOW}$	PWRCTR='000'	45	53	61 **TBD**	mA
TX Mode Current(s) (3) (TX output pin 1 only)	$I_{TX\text{-}HIGH}$	DSLEEP bit = LOW RADIOEN bit = HIGH PWRCTR = '111' TXEN = V_{CC}, RXEN = 0V	185 **TBD**	210 **TBD**	235 **TBD**	mA
	$I_{TX\text{-}LOW}$	PWRCTR='000'	5	7	8 **TBD**	mA
RSTN Pulse Width (1)	T_{RSTN}	Pulse width required to awaken from DSLEEP mode	1			µsec

Notes:

1. *Guaranteed by design and/or simulation but not tested.*
2. *Guaranteed by Engineering Qualification testing. Test data available upon request.*
3. *Guaranteed by 100% Production Test Screening.*

SYNTHESIZER AC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5 V, T_A = +25°C, no RF signals applied.
External reference signal (XIN) = 0.7 Vpp at 13.824MHz.
Device configured to TUNE mode, unless noted otherwise.
Production test schematic of Figure 20, unless noted otherwise.

Table 10. Synthesizer AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range (2) (3) (4)	F_{SYNTH}	117 Channels 2391.106 to 2494.563 MHz (OFFSET bit=LOW) 2389.106 to 2492.563 MHz (OFFSET bit=HIGH)	0		116	Ch
Channel Spacing	ΔF_{SYNTH}	Not programmable		891.871		kHz
Tuning Resolution	$F_{SYNTH-RES}$	Δ-Σ modulator tuning resolution		3.955		kHz
Synthesizer Loop BW	BW_{LOOP}			45		kHz
Synthesizer Settling Time (2)	t_{LOCK}	Worst-case frequency hop of Ch10 to Ch104, or Ch104 to Ch10. Measured to within ±10 ppm of final frequency.		180	220	µsec
Synthesizer Open-Loop Drift	$\Delta F_{OL-DRIFT}$	Max frequency drift in open-loop mode of operation, 1 msec frame		12		kHz
Residual FM (2)	ΔF_{RMS}	RMS, integrated over ±500 kHz bandwidth (500 Hz lower bound of integration)		7	15	kHz
Phase Noise (2)	$L\phi(f_M)$	ΔF = 10 kHz		-68	-63	dBc/Hz
		ΔF = 100 kHz		-82	-75	dBc/Hz
		ΔF = 1 MHz		-115	-89	dBc/Hz
		ΔF = 2 MHz		-120	-119	dBc/Hz
		ΔF >= 3 MHz		-130	-129	dBc/Hz
LO Leakage at TX Pin (2)	P_{LO_TX}	In TUNE mode		-50	-35	dBm
Crystal Oscillator Reference Frequency	F_{REF}			13.824		MHz
External Oscillator Input Level (3)	V_{REF}	External reference oscillator input level capacitively-coupled to XIN pin	1.0			Vpp
		External reference oscillator input level DC-coupled to XIN pin, centered at 1.2V	0.7	1.0		Vpp
Serial Bus Clock Frequency	F_{SER_CLK}			6.912		MHz
Power-On Time (3)	$t_{RSTN-CAL}$	Minimum time delay required from rising edge of RSTN pulse until a CAL command may be issued	350			µsec
	$t_{RADIOEN-LOCK}$	Minimum time delay required from setting RADIOEN=HIGH until RFIC reacquires lock at previously-commanded frequency	700			µsec
	$t_{STDBY-IDLE}$	Minimum time delay required from setting OSCOFF=LOW (while in STANDBY mode) until the crystal oscillator reaches full amplitude of oscillation (assumes crystal R_{SER} = **TBD** Ω)	5 **TBD**			msec

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Interface Timing Parameters (1)	t_{CLK}	Minimum SYN_CLK period (Maximum Serial Clock Rate)	125			nsec
	$t_{DATA-SU}$	Minimum DATA_VALID-to-CLK setup time	10			nsec
	$t_{DATA-HOLD}$	Minimum CLK-to-DATA_INVALID hold time	10			nsec
	t_{CLK-PW}	Minimum SYN_CLK pulse width	20			nsec
	t_{EN-PW}	Minimum SYN_EN pulse width	20			nsec
	t_{EN-DLY}	Minimum DATA-to-ENABLE delay time	20			nsec

Notes:

1. *Guaranteed by design and/or simulation but not tested.*
2. *Guaranteed by Engineering Qualification testing. Test data available upon request.*
3. *Guaranteed by 100% Production Test Screening.*
4. *Guaranteed over 0 to +70C temperature range by 100% Production Test Screening at +25C with additional margin.*

RECEIVER AC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5 V, T_A = +25°C, external reference signal (XIN) = 0.7 Vpp at 13.824MHz (±20ppm accuracy).
All specifications apply over an RX RF input signal frequency accuracy of ±20ppm.
Calibration (CAL) algorithm performed at given temperature prior to qualification test.
Device configured to RX mode, unless noted otherwise.
RF levels referenced to input of RFIC (not ANTENNA port of RF module).
Production test schematic of Figure 20, unless noted otherwise.

Table 11. Receiver AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Frequency Range	F_{RX}	117 Channels from 2391.106 MHz to 2494.563 MHz	0		116	Ch
RX Sensitivity (CW BER < 10^{-3}) (3)	P_{RX_HIGH}	RXGAIN = HIGH (HIGH_GAIN Mode)		-96	-92	dBm
(576 kbps GFSK BT=0.6 ΔF = ±190kHz)	P_{RX_LOW}	RXGAIN = LOW (LOW_GAIN Mode)		-84	-79	dBm
RX Strong Signal (CW BER < 10^{-7}) (2)	P_{RXSS_HIGH}	RXGAIN = HIGH (HIGH_GAIN Mode)	-43	-35		dBm
(576 kbps GFSK BT=0.6 ΔF = ±190kHz)	P_{RXSS_LOW}	RXGAIN = LOW (LOW_GAIN Mode)	-18	-10		dBm
Input Intercept Point, 3rd Order	$IIP3_{RX\_HIGH}$	RXGAIN = HIGH (HIGH_GAIN Mode)		-45		dBm
	$IIP3_{RX\_LOW}$	RXGAIN = LOW (LOW_GAIN Mode)		-23		dBm
LO Leakage at RX Pin (2)	P_{LO_RX}	RX mode		-50	-45	dBm
		TUNE mode		-50	-45	dBm
RXGAIN Step Size (3)	ΔG_{RXGAIN}	Difference between RX HIGH_GAIN and LOW_GAIN modes	16	22	28	dB
RXGAIN Step Settling Time (1)	t_{GAIN}			2	3	µsec
Image Rejection (3)	IR_{RX}		20	25		dB
RSSI Dynamic Range (2)	ΔP_{RSSI}	RXGAIN = LOW (LOW_GAIN Mode)	-83		-33	dBm
		RXGAIN = HIGH (HIGH_GAIN Mode)	-103		-53	dBm
RSSI Output Voltage Range (2)	ΔV_{RSSI}	RXGAIN = LOW (LOW_GAIN Mode) P_{RXIN} = –83 dBm to –33 dBm	0.2		2.0	V
		RXGAIN = HIGH (HIGH_GAIN Mode) P_{RXIN} = –103 dBm to –53 dBm	0.2		2.0	V
RSSI Slope (3) (must be monotonic)	$\Delta V/\Delta P_{RSSI}$	RXGAIN = LOW (LOW_GAIN Mode) P_{RXIN} = –83 dBm to –33 dBm	20	30	40	mV/dB
		RXGAIN = HIGH (HIGH_GAIN Mode) P_{RXIN} = –103 dBm to –53 dBm	20	30	40	mV/dB
RSSI Source Impedance	Z_{RSSI}	Internal series resistance to RSSI output		500		Ω
RSSI Settling Time (2)	Δt_{RSSI}	10% to 90% points, C_{RSSI} = 2.2 nF		5	10	µsec
RSSI Jamming (2) (HIGH_GAIN Mode)	P_{RSSI_JAM}	Equivalent On-Channel signal yields same RSSI value as -45dBm input at ±2MHz offset		-95		dBm
Demodulated Audio Output	V_{DMOD}	ΔF = ±190 kHz peak deviation, Output on TESTP pin (single-ended)		360		mVpp

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Slicer Polarity (1)	RX_DATA	$F_{RX} = F_C + \Delta F$ (INVDOUT = LOW)		HIGH		Logic
		$F_{RX} = F_C - \Delta F$ (INVDOUT = LOW)		LOW		Logic
Receive Processing Delay	ΔT_{RXMOD}	Fixed receive processing delay between application of modulating at air interface and resulting audio at TESTP & TESTN output pins (sum of IF BPF group delay and data lowpass filter delay)		2.4		µsec
RXDATA Output Rise/Fall Time (1)	Δt_{RXDATA_RISE}	10% to 90% points, C_{LOAD}=10 pF			50	nsec
RXDATA Pulsewidth Jitter	$\Delta T_{RXDATA-SS}$	"Locked" jitter RF input FSK-modulated with '11110000' data stream TC_CTRL = LOW (SLOW) SLOWTC[1:0] = '10' (820 µsec)		±0.3		µsec
	$\Delta T_{RXDATA-ACQ}$	"Acquisition" jitter RF Input coded with 50bits ('10101'...) followed by 16bit Sync Word TC_CTRL = HIGH (FAST) FASTTC[1:0] = '10' (25 µsec)		±0.3		µsec
RXDATA Duty Cycle (3) (4) (End of HOLD frame)		Input Data Pattern = '101010', TC_CTR =1 msec FAST, 4 msec SLOW FASTTC[1:0] = '10' (25 µsec) SLOWTC[1:0] = '11' (HOLD)	40	50	60	%
Co-Channel Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	C/I_{CO-CH}	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		10		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		10		dB
±1-Ch Offset Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	C/I_{1-CH}	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		-5		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		-5		dB
±2-Ch Offset Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	C/I_{2-CH}	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		-35		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		-35		dB
+3 Ch Offset Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	C/I_{3-CH}	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		-40		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		-40		dB
Image Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	C/I_{IMAGE}	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		-15		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		-15		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Image ±1-Ch Offset Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	$C/I_{IMG-1CH}$	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		-30		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		-30		dB
Image -2-Ch Offset Selectivity (BER < 10^{-3}) (Interferer modulated with 576 kbps GFSK BT=0.6 ΔF = ±190kHz uncorrelated)	$C/I_{IMG-2CH}$	RXGAIN = LOW (LOW_GAIN Mode) Desired Reference Signal = -78 dBm		-40		dB
		RXGAIN = HIGH (HIGH_GAIN Mode) Desired Reference Signal = -87 dBm		-40		dB

Notes:

1. *Guaranteed by design and/or simulation but not tested.*
2. *Guaranteed by Engineering Qualification testing. Test data available upon request.*
3. *Guaranteed by 100% Production Test Screening.*
4. *Guaranteed over 0 to +70C temperature range by 100% Production Test Screening at +25C with additional margin.*

TRANSMITTER AC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5 V, T_A = +25°C, external reference signal (XIN) = 0.7 Vpp at 13.824MHz.
Device configured to TX mode, unless noted otherwise.
RF levels referenced to output of RFIC (not ANTENNA port of RF module).
Production test schematic of Figure 20, unless noted otherwise.

Table 12. Transmitter AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency Range (3)	F_{TX}	117 Channels from 2391.106 MHz to 2494.563 MHz	0		116	Ch
P.A. RF Output Level (3)	P_{RF_OUT}	Maximum Power Mode (PWRCTR bits = '111')	+18.5	+20		dBm
		Minimum Power Mode (PWRCTR bits = '000')	-13	-8	-3	dBm
P.A. RF Output Steps	ΔP_{RF_OUT}	Intermediate Power Modes (PWRCTR bits = '001' to '110')		4		dB
P.A. RF Output Level (2) Variation vs. Temperature	ΔP_{RF_TEMP}	Intermediate Power Modes (PWRCTR bits = '000' to '110')		3	5	dB
P.A. RF Output Level Variation vs. Frequency	ΔP_{RF_FREQ}	Any Power Mode (PWRCTR bits = '000' to '111')		3		dB
P.A. Harmonic Output Level	$N*F_O$	N=2 and 3		-30		dBc
P.A. Output Impedance	Z_{OUT_TX}	Unmatched, measured at TX output (pin 1), PWRCTR bits = '000'		4+j30		Ω
Transmit Modulation Data Rate	F_{DATA}			576		kbps
Transmit Modulation Data Polarity	ΔF_{DATA}	TXMOD = HIGH (INVDIN = LOW)		$F_{TX} = F_C+\Delta F_{MOD}$		MHz
		TXMOD = LOW (INVDIN = LOW)		$F_{TX} = F_C-\Delta F_{MOD}$		MHz
Transmit FM Deviation (3)	ΔF_{MOD}	Measured with '00001111' pattern	±181	±190	±209	kHz
Transmit FM Deviation Overshoot/Undershoot		Frequency transition peaks relative to steady-state deviation		±10		%
Transmit Modulation Shaping		Gaussian filter response Bandwidth-Time product		0.6		B*T
Transmit Modulation Processing Delay (1)	ΔT_{TXMOD}	Fixed modulation processing delay between application of data at TXMOD pin and resulting modulation at air interface		2.0		µsec
P.A. RF Output (2) Rise Time	t_{RISE}	Referenced from rising edge of TXEN	1.5	5	10	µsec
P.A. RF Output (2) Fall Time	t_{FALL}	Referenced from falling edge of TXEN	1.5	5	10	µsec
TDD Spectral Mask (2)		Any Power Mode (PWRCTR bits = '000' to '111') Measured at a ±3 MHz frequency offset, RBW=100 kHz, VBW=100 kHz		-30	-20	dBm
Spurious Signals (2) (5)	P_{SPUR}	Any Power Mode (PWRCTR bits = '000' to '111') Measured in a 1 MHz bandwidth, in any FCC restricted band		-50	-41	dBm

Notes:

1. *Guaranteed by design and/or simulation but not tested.*
2. *Guaranteed by Engineering Qualification testing. Test data available upon request.*
3. *Guaranteed by 100% Production Test Screening.*
4. *Guaranteed over 0 to +70C temperature range by 100% Production Test Screening at +25C with additional margin.*
5. *Measured with bandpass filter in TX path as shown in Application Schematic of Figure 11.*

TYPICAL OPERATING CHARACTERISTICS

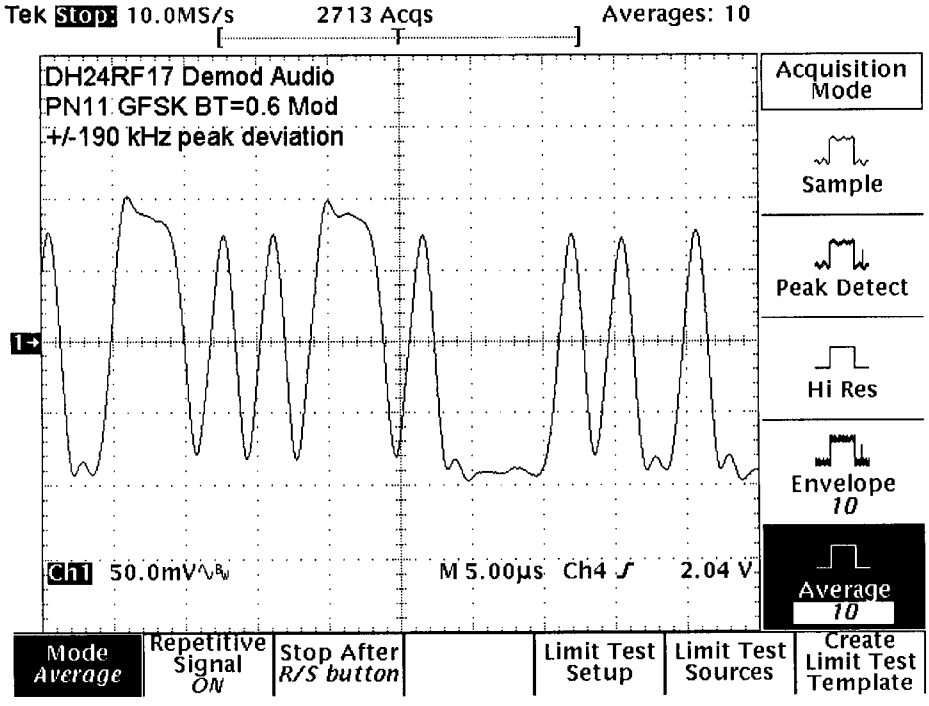


Figure 21. Demod Audio

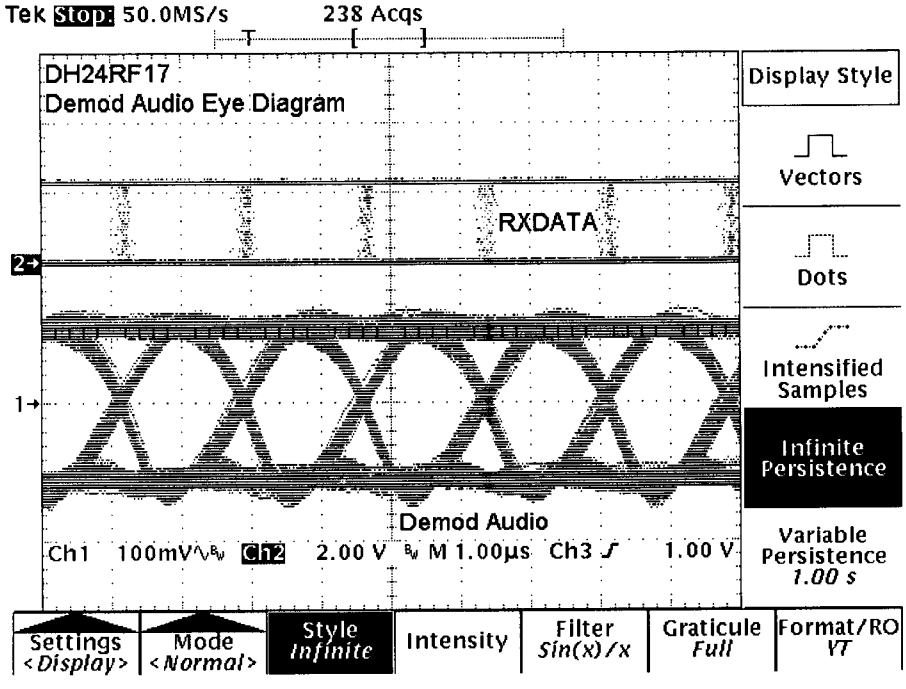


Figure 22. Demod Audio & RX Data Eye Pattern

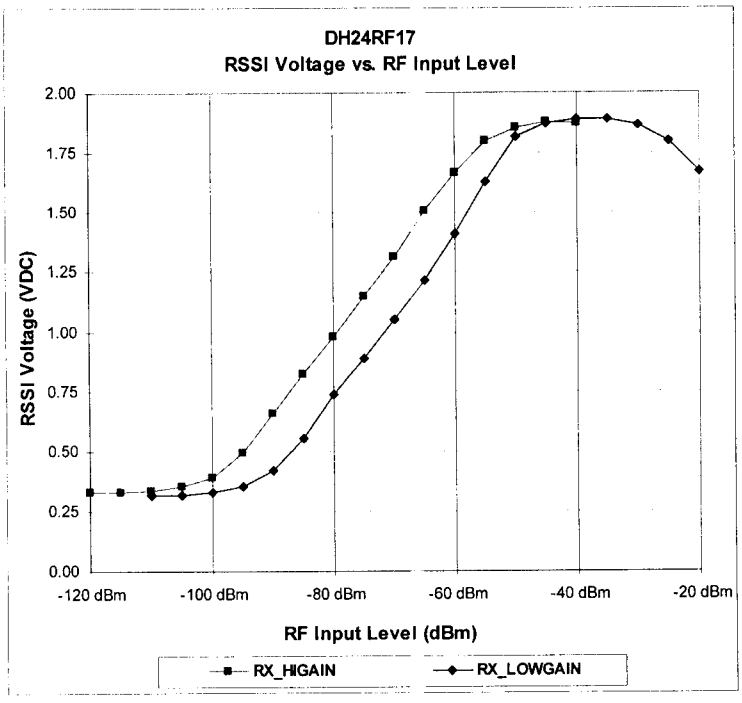


Figure 23. RSSI Voltage

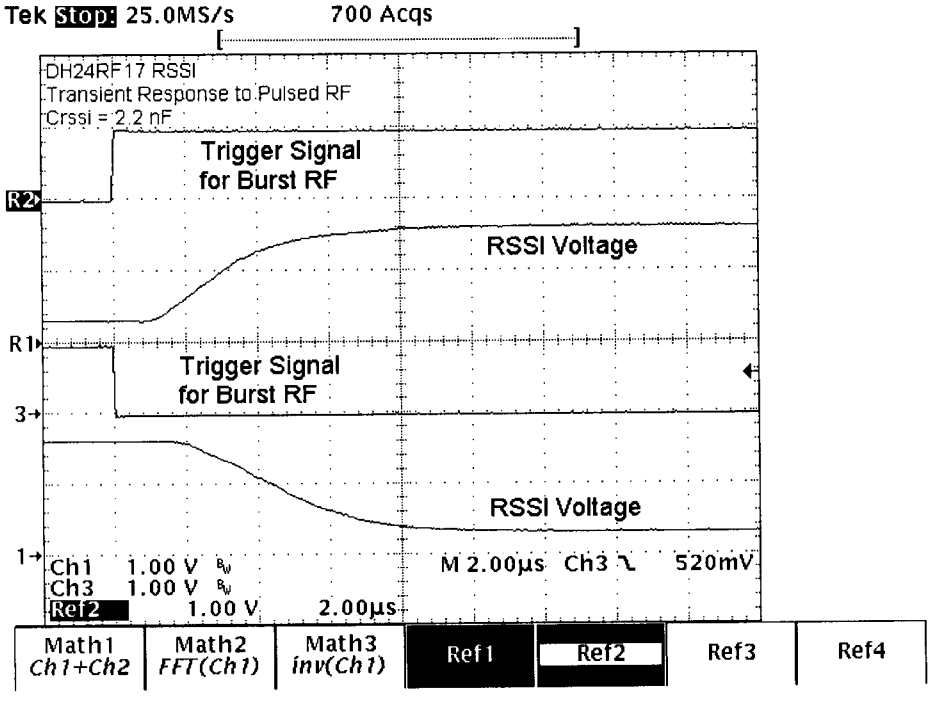
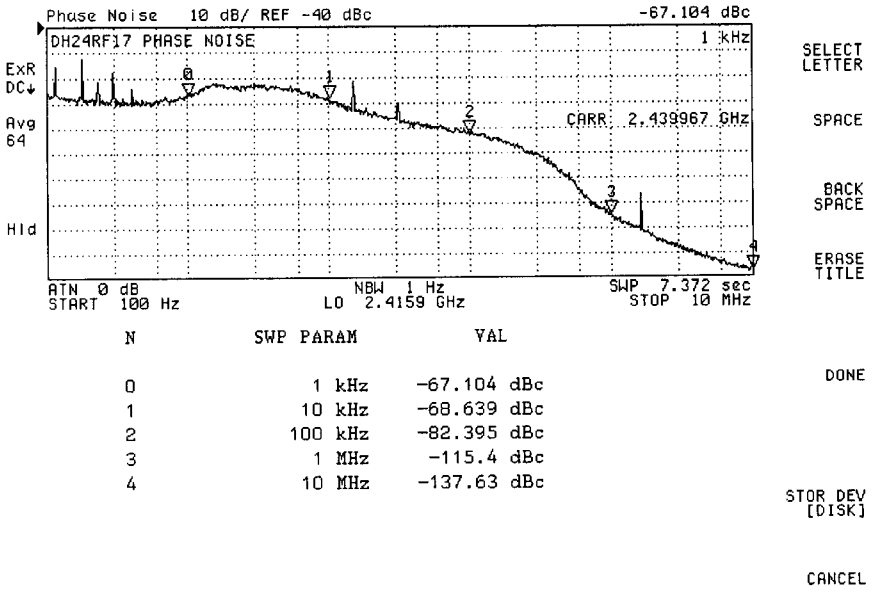


Figure 24. RSSI Transient Response Time (C_{RSSI}=2.2 nF)



N	SWP PARAM	VAL
0	1 kHz	-67.104 dBc
1	10 kHz	-68.639 dBc
2	100 kHz	-82.395 dBc
3	1 MHz	-115.4 dBc
4	10 MHz	-137.63 dBc

Figure 25. Phase Noise, Closed Loop

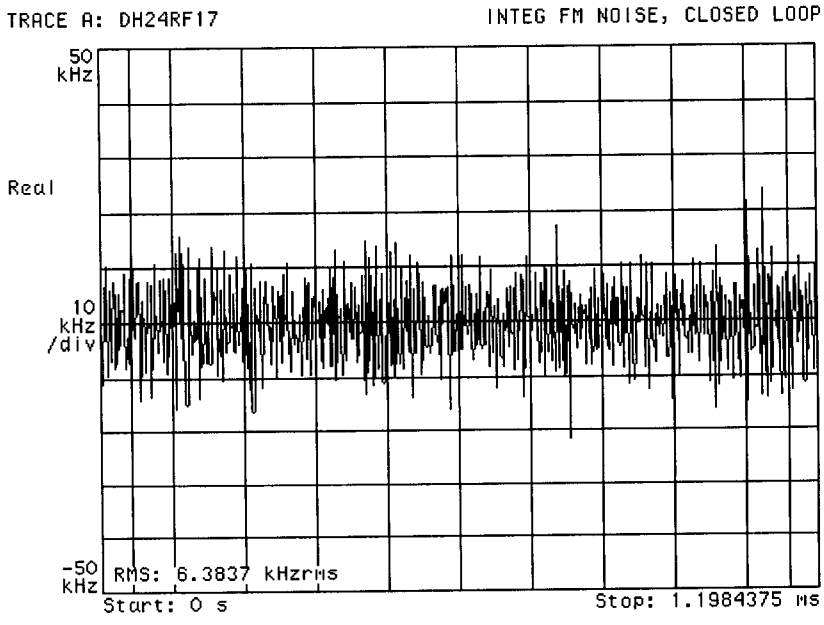


Figure 26. Integrated FM Noise

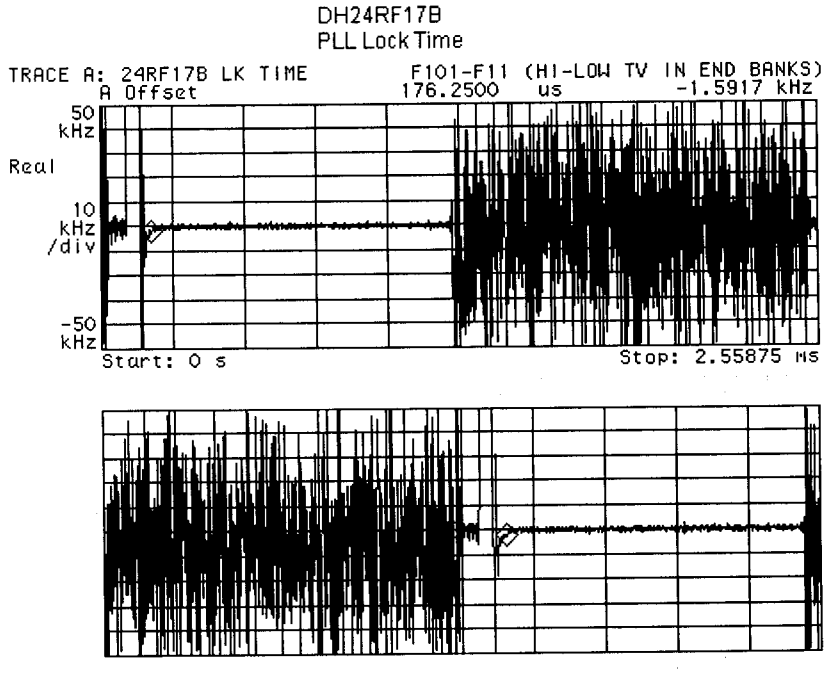


Figure 27. PLL Synthesizer Settling Time

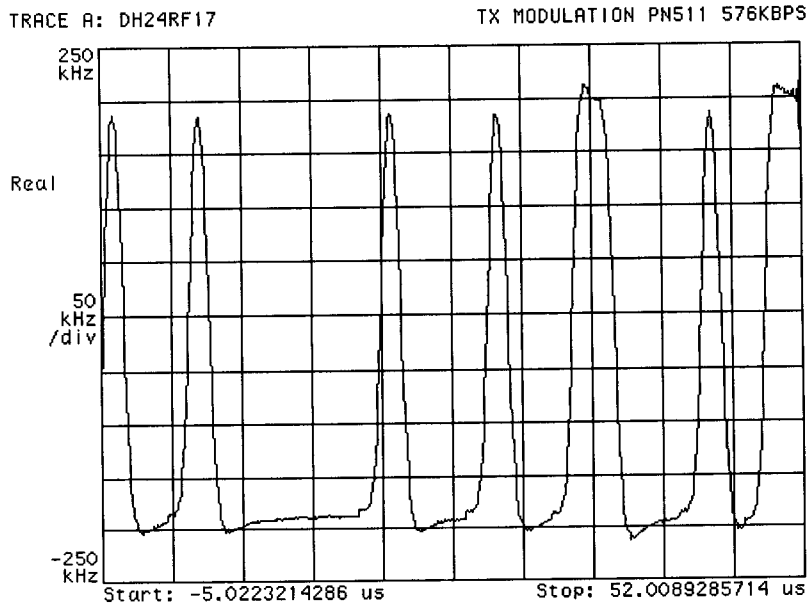


Figure 28. Transmit Modulation

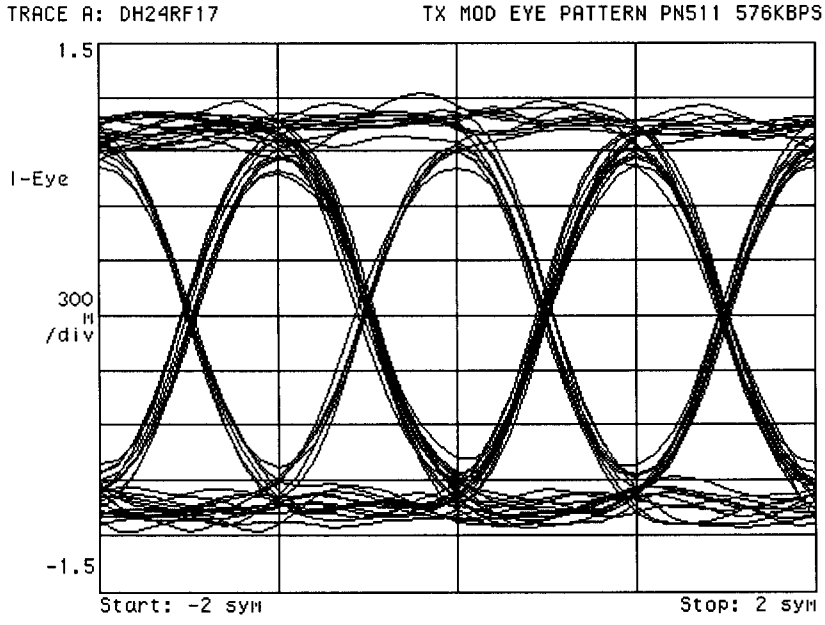


Figure 29. TX Data Eye Pattern

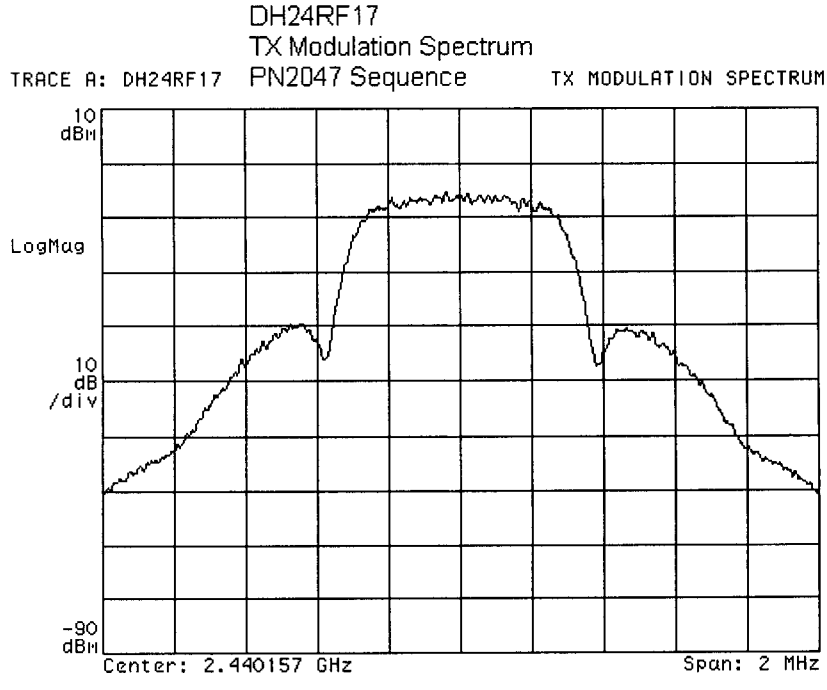


Figure 30. TX Modulation Spectrum

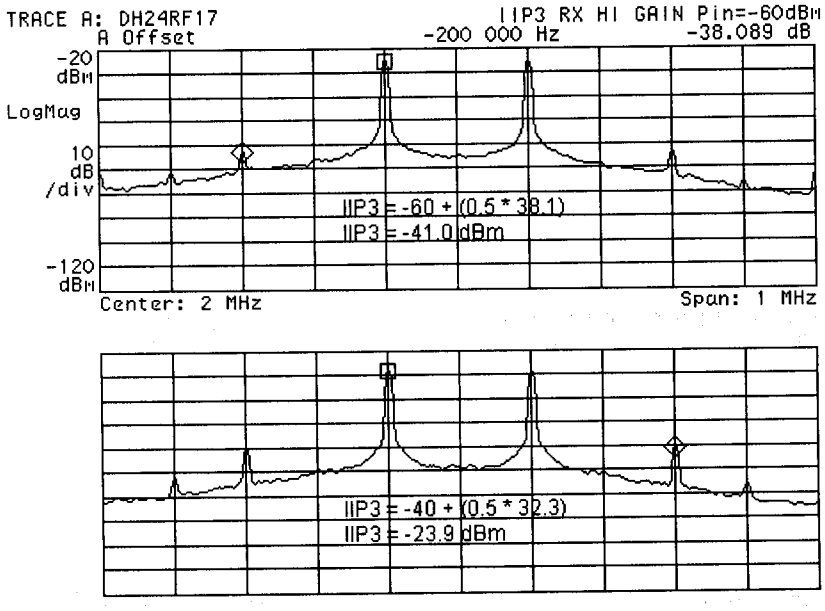


Figure 31. LNA/Mixer IIP3

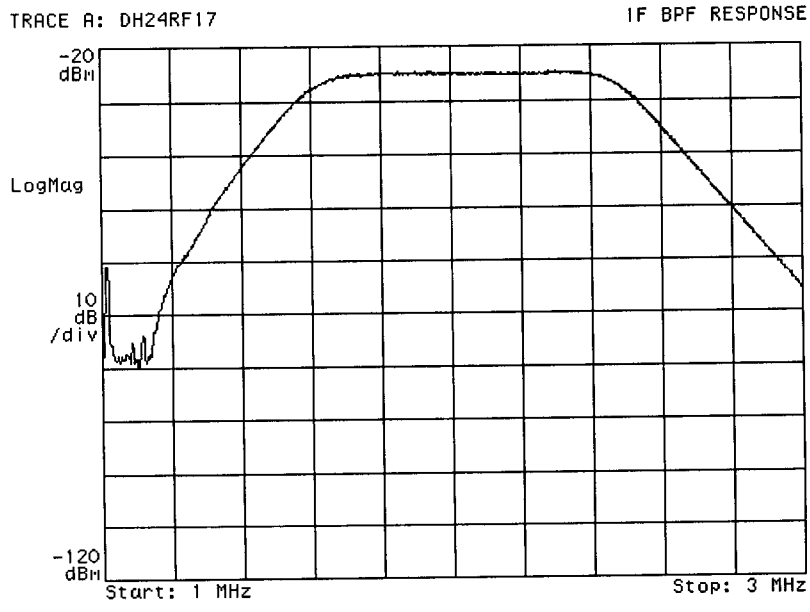


Figure 32. IF BPF Frequency Response

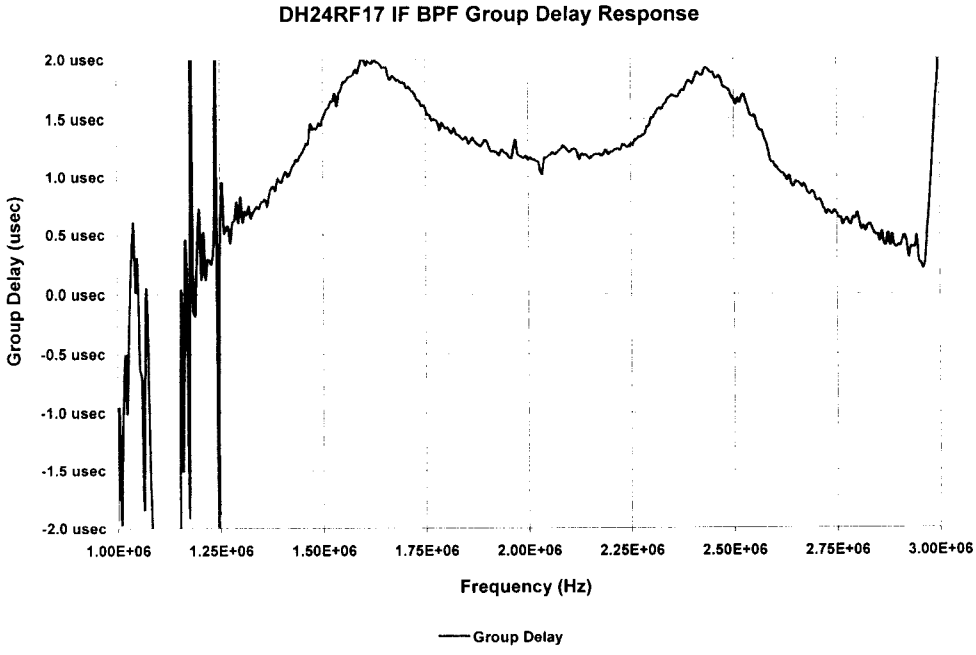


Figure 33. IF BPF Group Delay

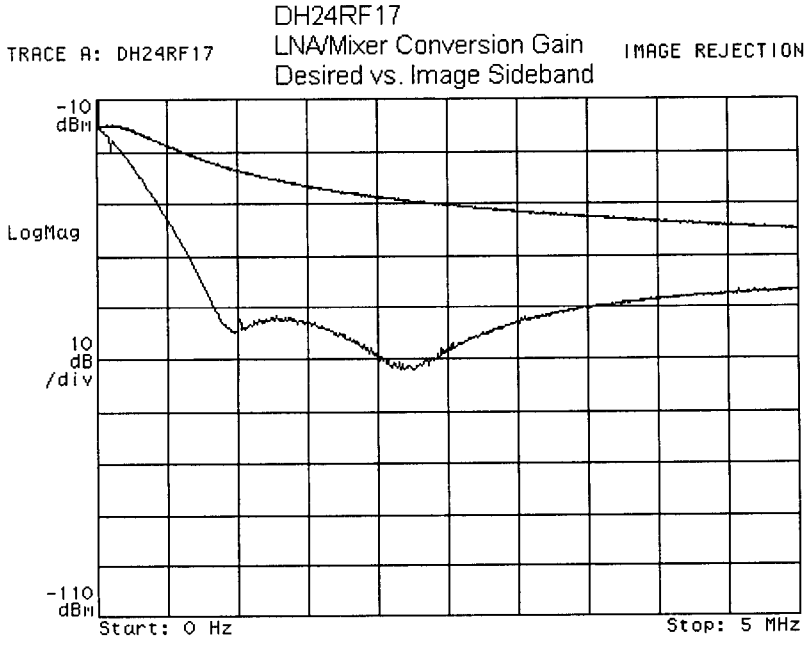


Figure 34. Mixer Image Rejection

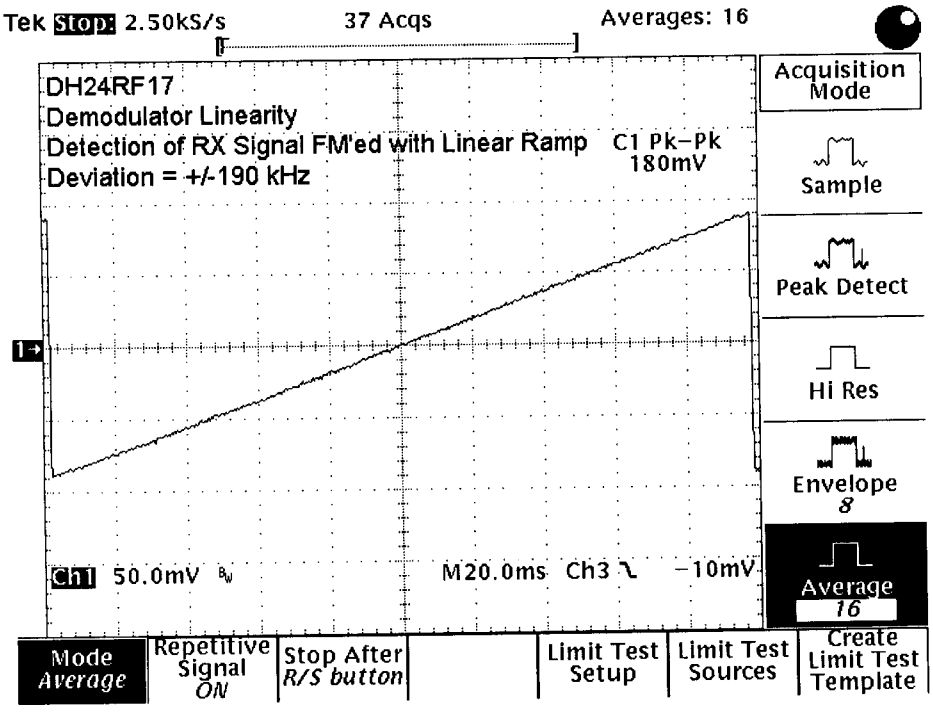


Figure 35. FM Discriminator Linearity

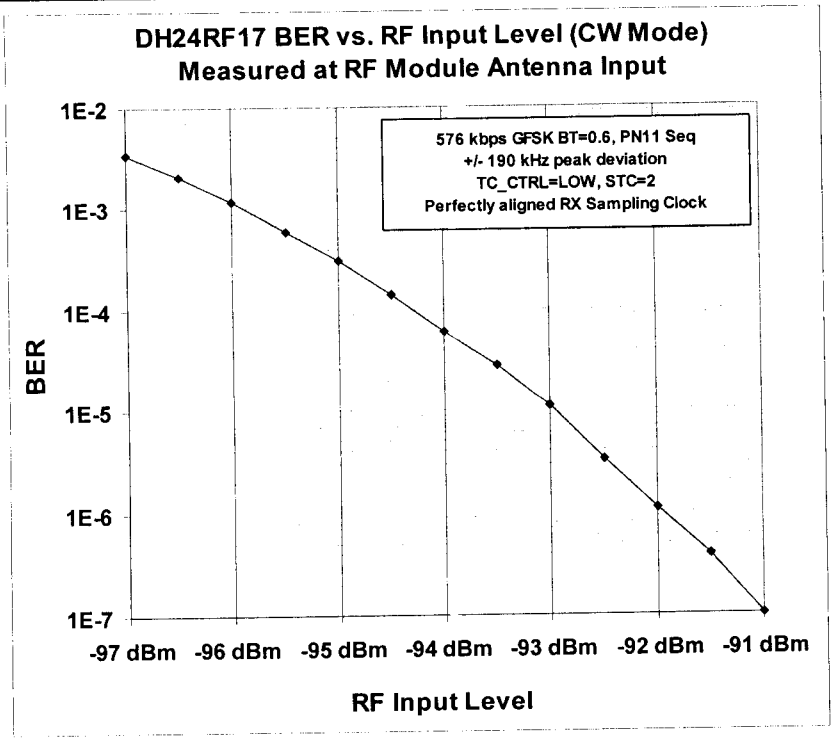


Figure 36. BER vs. RF Level (CW Mode)

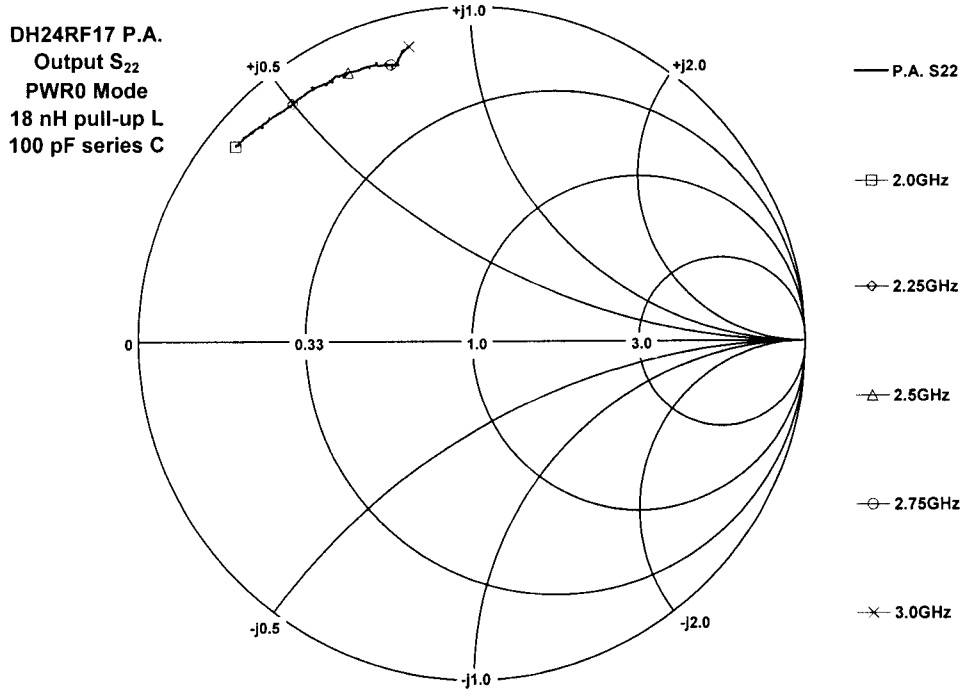


Figure 37. P.A. Output Impedance

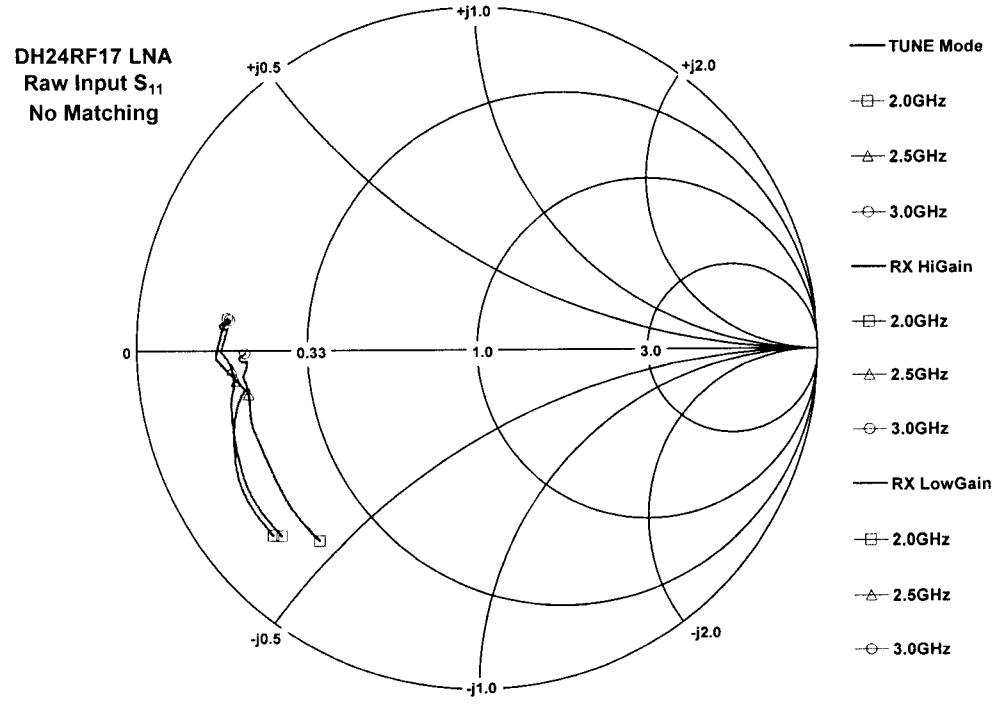
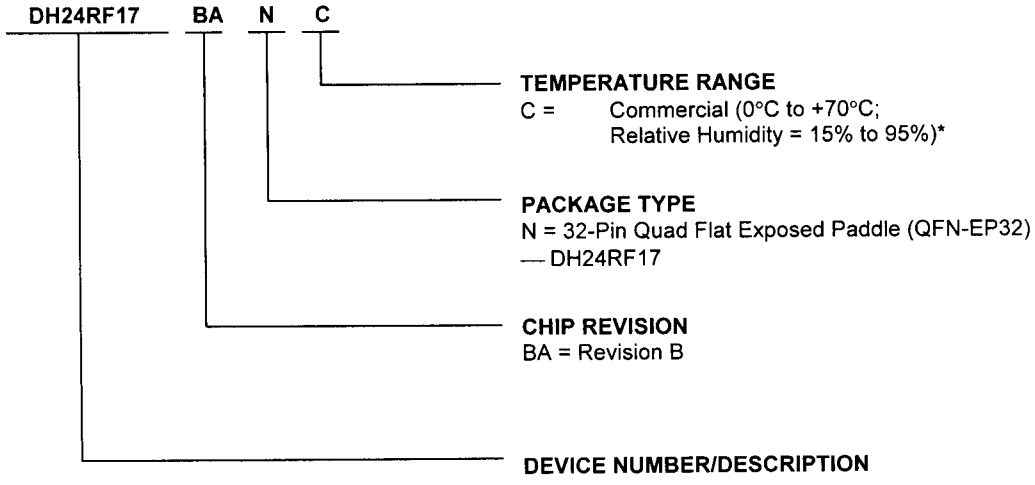


Figure 38. LNA Input Impedance

ORDERING INFORMATION

Standard Products

DSPG standard products are available in several packages and operating ranges. The ordering number (valid combination) is formed by a combination of the elements below:



Valid Combinations	
DH24RF17	BANC

Valid Combinations

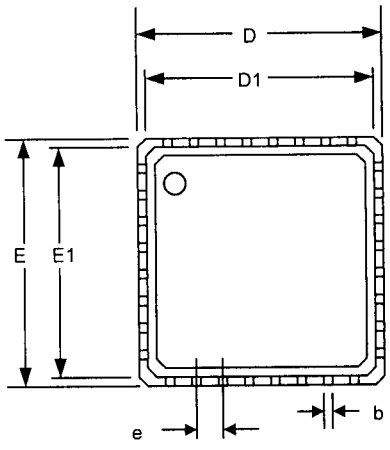
Valid combinations list configurations planned to be supported in volume for this device. Consult the local DSPG sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on DSPG's standard commercial grade products.

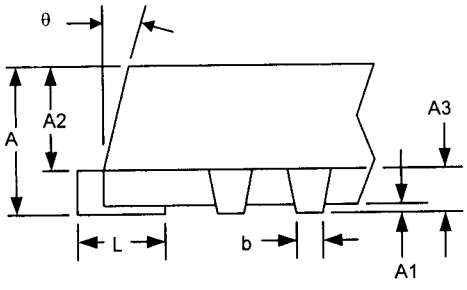
Note:

**Functionality of the device from 0° C to +70° C is guaranteed by production testing.*

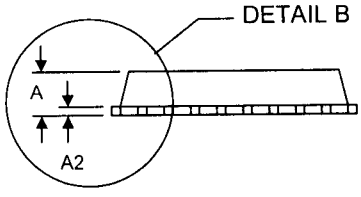
PACKAGE OUTLINE DRAWING

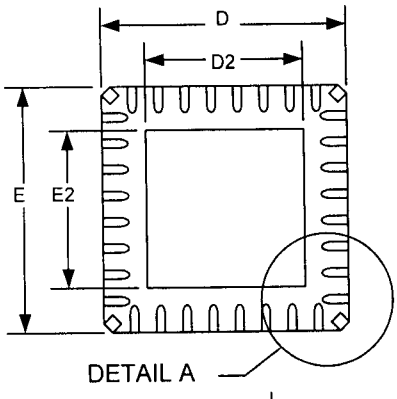
32-Pin QFN-EP (7X7)

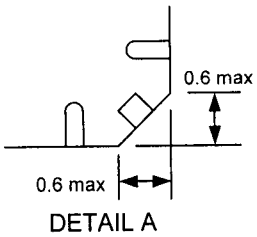




DETAIL B







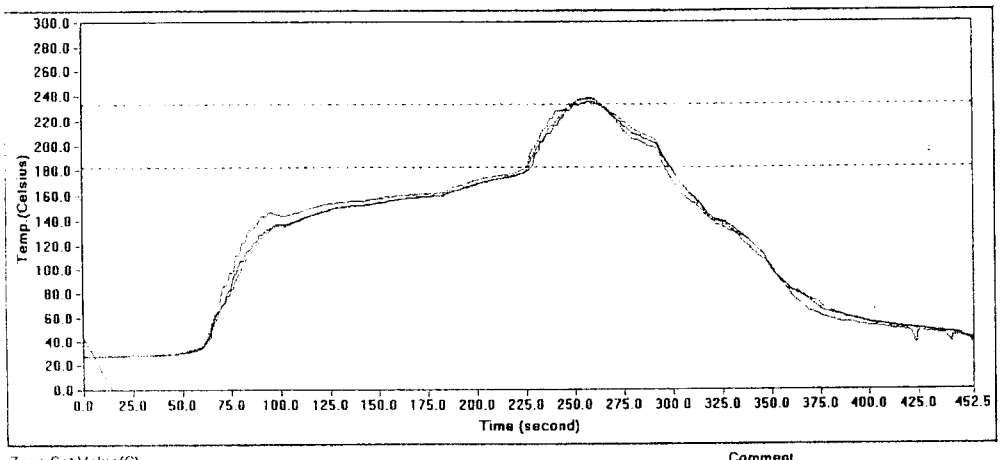
DETAIL A

SYMBOL	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.00	0.65	1.00	0.000	0.026	0.039
A3	0.20 REF			0.008 REF		
b	0.23	0.30	0.38	0.009	0.012	0.015
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
D2	5.05	5.20	5.35	0.199	0.205	0.211
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
E2	5.05	5.20	5.40	0.199	0.205	0.213
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	—	12°	0°	—	12°

Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

RECOMMENDED INFRA-RED REFLOW PROFILE

THERMOTRACKER report



Report Date(dd/mm/yy): 07/06/2001

Company: SPIL

Product: QFN64

Line Speed: 0.59 M/Min

Down Load Information
Scan Rate(mm:ss): 00:00.5
Date(dd/mm/yy): 07/06/2001
Time(hh:mm:ss): 09:57:00

Data File: r292.pdf

Zone Set Value(C)

Zone Number	1	2	3	4	5	6	7	8	9	10
SV(Up)	200	170	170	185	318	0	0	0	0	0
SV(Down)	200	170	170	185	318	0	0	0	0	0

Comment
SLOPE 1.69

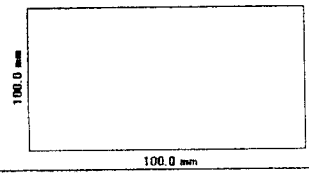
Sensor Description and Max/Threshold Information

Sensor Name	Max. Temp.(C)	At Time(Sec)	Time Above 234 Deg. C(Sec)	Time Above 183 Deg. C(Sec)
1:	237.7	257.5	15.0	73.0
2:	235.3	258.0	8.0	70.5
3:	44.1	0.0	0.0	0.0
4:	238.7	258.0	14.0	71.0

Sensor Location X mm , Ymm

1: ------ , ------
2: ------ , ------
3: ------ , ------
4: ------ , ------

PCB Move Direction



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