Reference oscillator and modulator

The PLL reference oscillator runs at one 32nd (9.750 MHz) of the final output frequency. IC2 pins 15 and 16 are the base and emitter of the internal transistor, configured with C1, C2 to form a Colpitts oscillator. The crystal XT1 has a series circuit including varicap diode D1, to provide the necessary pulling (+/- 1.5 KHz) for direct FSK (frequency shift keyed) operation. The crystal requires 10pF of load capacitance to oscillate at its nominal frequency. C14 and C17, in series with the oscillator feedback circuit and transistor, provide the necessary 10pF load.

R17 provides an RF decoupling function to the varicap and feeds the modulation waveform from the data shaping RC network R1, C20. This shaping is required to reduce the emissions (from the data high frequency content) in adjacent channels to below regulatory levels. The output from the reference oscillator is internally fed to IC2 phase detector.

Phase Sensitive Detector (PSD)

The phase locked loop requires a post phase detector filter to define the loop bandwidth. Since we use a frequency shifted reference oscillator to achieve our modulation, the loop bandwidth is set to handle the highest frequencies required in the transmitted data together with a speedy lock up time. Since the incidental phase noise outside the loop bandwidth is quite high on this simple PLL, the loop filter is not allowed to be too wide and a compromise value of around 50kHz is selected. The loop filter components R5, C10 and C11 determine the loop bandwidth.

Voltage Controlled Oscillator (VCO)

IC2 includes a VCO. All components, including the tuning varicap diode are on chip, with the exception of the tank circuit inductor. This inductor is formed by L3 and L5 in series. Two components are used to obtain a finer selection resolution than would be offered by the preferred values of a single component. R3 provides the DC feed to the VCO transistors on chip.

RF2514 output amplifier

The on chip output stage offers an open collector on IC2 pin 3 fed to a resonant circuit at 312 MHz, formed by L1, C3 and C4. The impedance transformer formed by the tapped capacitor configuration offers a match to 50 ohms. DC is fed through L1 from Vbatt and decoupled by C6. A 3 element low pass filter network matched to 50 ohms is formed by L4, C4 and C5. In this case C4 value is a composite of the value required for the output tank circuit and the low pass filter input component. R21 (270R) provides a resistive termination to the RF amplifier to improve stability.

A bias feed is required to the output transistor base on pin 5 of IC2 and this is fed via R2, decoupled by C16, from the 1.8v regulator RG1.