Design

312MHz Amie Circuit Description

A. Circuit configuration

A.1 A 5th overtone Hartley crystal oscillator (TR1) running at 104.000 MHz is modulated using narrow band direct frequency shift keying. Deviation at 312.000MHz is ±1.5 kHz.

A.2 The common emitter tripler stage (TR2) feeds a tuned loop antenna, via a pi section matching circuit and harmonic filter.

A.3 A custom integrated circuit (IC1) generates a digital identity code with a sequence held on chip in EEPROM. The IC has an integral clock running at 6KHz. The coding word is generated using pulse position modulation. Each bit is 1mS wide, with a pulse width of either 0.666mS (Data 0) or 0.333mS (Data 1).

IC1 also controls transmission time (1 second), voltage regulator (TR3) and provides a low battery voltage comparator. During normal use the LED remains on for 5 seconds. If the battery voltage is sensed low during a transmission, the LED will flash for 5 seconds.

A.4 The product uses a 2 cell lithium battery, nominally 6.0v. Both RF stages are powered from a 3.75v regulated rail.

B. Oscillator stage

B.1 The oscillator (TR1) is a Hartley design using a 5th overtone crystal at 104.000 MHz. DC conditions are set by R6, R15 and R16. C2 decouples R6 at signal frequencies. The oscillator is fed from a regulated DC supply of 4.2v provided by TR3.

B.2 Tank circuit resonance at 104MHz is set by L2 / L4 tuned by C10 (fixed) and D1 (varicap diode) in series with C3. C7 provides decoupling at the DC feed to the tank circuit. The tuning point of this circuit is modulated by varying the bias applied to D1. Data from the custom IC is band limited by R1, C1 and fed to D1 by R2. R2 provides a high impedance at 104MHz.

B.3 The series mode crystal provides selective decoupling of the emitter impedance. L3 tunes out crystal parallel capacitance to improve deviation performance. C9 provides a DC block and the correct load condition for the crystal to operate on the desired frequency.

B.4 The required levels at TP1 to set the two frequencies, 104.000MHz +500Hz and 104.000MHz -500Hz, are programmed into the custom IC at the production test stage.

C. Frequency multiplier stage and antenna

C.1 The output from the Hartley oscillator is coupled via C4 to the base of the multiplier (TR2) via a resistive shunt. This resistor (R3, 100Ω) provides a controlled load for the oscillator, preventing moding and spurious operation. C5 provides a DC block. The multiplier is fed from a regulated DC supply of 4.2v provided by TR3. This provides consistent power output and range performance throughout the battery life.

C.2 A fixed bias is provided on the multiplier stage by R17, R4 and R5. With no drive, the quiescent current to the multiplier is approximately 1mA and with drive this rises to 3mA. Total current consumption of the oscillator and multiplier together is typically 8mA.

C.3 The multiplier collector load inductor L5 (33nH) resonates at 312MHz with C11 (5p6) and TR2 collector capacitance and strays. The pi circuit (resultant collector capacitance, L1 100nH and C8 27pF) then matches the high collector impedance to near 50Ω at point TP26.

C.4 The antenna loop is parallel resonant with the 2.6pF trimmer VC1 in series with C8 27pF. This capacitive tap transformer matches the low impedance feed at the capacitor junction to the high dynamic impedance of the parallel resonant loop.

TP5 at the bottom of the antenna loop provides a test point for alignment purposes during production testing.