BlueCore® CSR8615 QFN

CSR8615 Mono ROM Solution

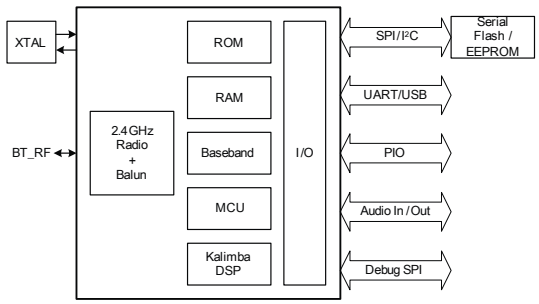
1-mic CVC Audio Enhancement

Fully Qualified Single-chip Bluetooth® v4.0 System

Engineering Sample

CSR8615A04

Issue 2



Features

- Bluetooth® v4.0 specification compliant
- 80MHz RISC MCU and 80MIPS Kalimba DSP
- High-performance mono codec with 1 microphone input
- Internal ROM, serial flash memory and EEPROM interfaces
- Radio includes integrated balun with RF performance of 8dBm transmit power and -89dBm receiver sensitivity
- AVRCP v1.4
- 5-band fully configurable EQ
- Wideband speech supported by HFP v1.6 and mSBC codec
- CSR's latest CVC technology for narrowband and wideband voice connections including wind noise reduction
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Secure simple pairing, CSR's proximity pairing and CSR's proximity connections
- Audio interfaces: Line-in and PCM
- Serial interfaces: USB 2.0, UART, I²C and SPI
- SBC, MP3 and AAC decoder support
- Wired audio support
- Integrated dual switch-mode regulators, linear regulators and battery charger
- External crystal load capacitors not required for typical crystals
- 3 LED outputs (RGB)
- 68-lead QFN 8 x 8 x 0.9mm 0.4mm pitch
- Green (RoHS compliant and no antimony or halogenated flame retardants)

General Description

CSR's BlueCore® CSR8615 QFN is a single-chip CSR8615 mono ROM solution for rapid evaluation and development of Bluetooth audio applications.

BlueCore® CSR8615 QFN consumer audio platform for wired and wireless applications using the QFN package integrates an ultra-low power DSP and application processor with embedded flash memory, a high-performance mono codec, a power management subsystem and LED drivers.

The CSR configuration tools and the development kit provide a flexible and powerful development platform to design advanced and high-quality audio products using BlueCore® CSR8615 QFN single-chip Bluetooth audio solution.

Applications

- Bluetooth mono speakers
- Speakerphones
- 1-mic CVC headset or headphones
- Handsfree car kits

The enhanced Kalimba DSP coprocessor with 80MIPS supports enhanced audio and DSP applications.

The integrated audio codec supports stereo line input with 1-mic CVC input and mono output, as well as a variety of audio standards.

See *CSR Glossary* at www.csrsupport.com.

Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSR8615 Mono ROM Solution	QFN-68-lead (Pb free)	8 x 8 x 0.9mm 0.4mm pitch	Tape and reel	CSR8615A04-IQQF-R

Note:

Until CSR8615A04 reaches **Production** status, engineering samples order number applies. This is ES-CSR8615A04-IQQF, with no minimum order quantity.

CSR8615 QFN is a ROM-based device where the product code has the form CSR8615Axx. Axx is the specific ROM-variant, A04 is the ROM-variant for CSR8615 Mono ROM Solution.

At **Production** status minimum order quantity is 2kpcs taped and reeled.

Your attention is drawn to Cambridge Silicon Radio Limited's ("Seller"'s) standard terms of supply which govern the supply of **Prototype Products** or **Engineering Samples** and which state in clause 5:

5.1 "Prototype Products" or "Engineering Samples" means any products that have not passed all the stages of full production acceptance as determined solely by the Seller. The Seller will usually identify which of the Goods ordered are considered Prototype Products designating them "ES" on the Quotation and any Order for Prototype Products shall be subject to the special terms contained in this clause 5.

5.2 The Seller has used reasonable efforts to design and build the Prototype Products in accordance with the relevant specification, but because the testing carried out by the Seller in respect of the Prototype Products is incomplete, the Seller does not give or enter into any warranties, conditions or other terms in relation to quality or fitness for purpose of the Prototype Products and/or that the Prototype Products are free from bugs, errors or omissions.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

Contacts

General information	www.csr.com
Information on this product	sales@csr.com
Customer support for this product	www.csrsupport.com
Details of compliance and standards	product.compliance@csr.com
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CSR8615 Mono ROM Solution Development Kit Ordering Information

Description	Order Number
CSR8615 Mono ROM Solution Audio Development Kit	DK-8615-10161-1A

Device Details

Bluetooth low energy

- Dual-mode Bluetooth low energy radio
- Support for Bluetooth basic rate / EDR and low energy connections
- 3 Bluetooth low energy connections at the same time as basic rate A2DP

Bluetooth Radio

- On-chip balun (50Ω impedance)
- No production trimming of external components
- Bluetooth v4.0 specification compliant

Bluetooth Transmitter

- 8dBm (typ) RF transmit power with level control
- Class 1, Class 2 and Class 3 support, no external PA or TX/RX switch required

Bluetooth Receiver

- -91dBm (typ) π/4 DQPSK receiver sensitivity and -81dBm (typ) 8DPSK receiver sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available to application
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Bluetooth Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 32MHz

Kalimba DSP

- Enhanced Kalimba DSP coprocessor, 80MIPS, 24-bit fixed point core
- 2 single-cycle MACs; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 6K x 32-bit program RAM including 1K instruction cache for executing out of internal ROM
- 16K x 24-bit + 16K x 24-bit 2-bank data RAM

Audio Interfaces

- Stereo line input audio ADC with 1-mic CVC
- Mono audio DAC
- Supported sample rates of 8, 11.025, 16, 22.05, 32, 44.1, 48 and 96kHz (DAC only)

Auxiliary Features

- Crystal oscillator with built-in digital trimming

Package Option

- 68-lead QFN 8 x 8 x 0.9mm 0.4mm pitch

Physical Interfaces

- UART interface for debug
- USB 2.0 (full-speed) interface, including charger enumeration
- 1-bit SPI flash memory interface
- SPI interface for debug and programming
- I²C interface for EEPROM
- Up to 20 general purpose PIOs with 3 extra open-drain PIOs available when LED not used
- PCM and I²S (only in HCI mode) interfaces
- 3 LED drivers (includes RGB) with PWM flasher independent of MCU

Integrated Power Control and Regulation

- Automatic power switching to charger when present
- 2 high-efficiency switch-mode regulators with 1.8V and 1.35V outputs direct from battery supply
- 3.3V linear regulator for USB supply
- Low-voltage linear regulator for internal digital circuits
- Low-voltage linear regulator for internal analogue circuits
- Power-on-reset detects low supply voltage
- Power management includes digital shutdown and wake-up commands for ultra-low power modes

Battery Charger

- Lithium ion / Lithium polymer battery charger
- Instant-on function automatically selects the power supply between battery and USB, which enables operation even if the battery is fully discharged
- Fast charging support up to 200mA with no external components. Higher charge currents using external pass device.
- Supports USB charger detection
- Support for thermistor protection of battery pack
- Support to enable end product design to PSE law:
  - Design to JIS-C 8712/8714 (batteries)
  - Testing based on IEEE 1725

Baseband and Software

- Internal ROM
- Memory protection unit supporting accelerated VM
- 56KB internal RAM, enables full-speed data transfer, and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping

CSR8615 Mono ROM Solution Details

Bluetooth Profiles

- Bluetooth v4.0 specification support
- A2DP v1.2
- AVRCP v1.4
- DI v1.3

Music Enhancements

- Configurable 5-band EQ for music playback (rock, pop, classical, jazz, dance etc)
- SBC, MP3, AAC and Faststream decoder
- Volume Boost

Additional Functionality

- Support for multi-language programmable audio prompts
- CSR's proximity pairing and CSR's proximity connection
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Talk-time extension

CSR8600 ROM Series Configuration Tool

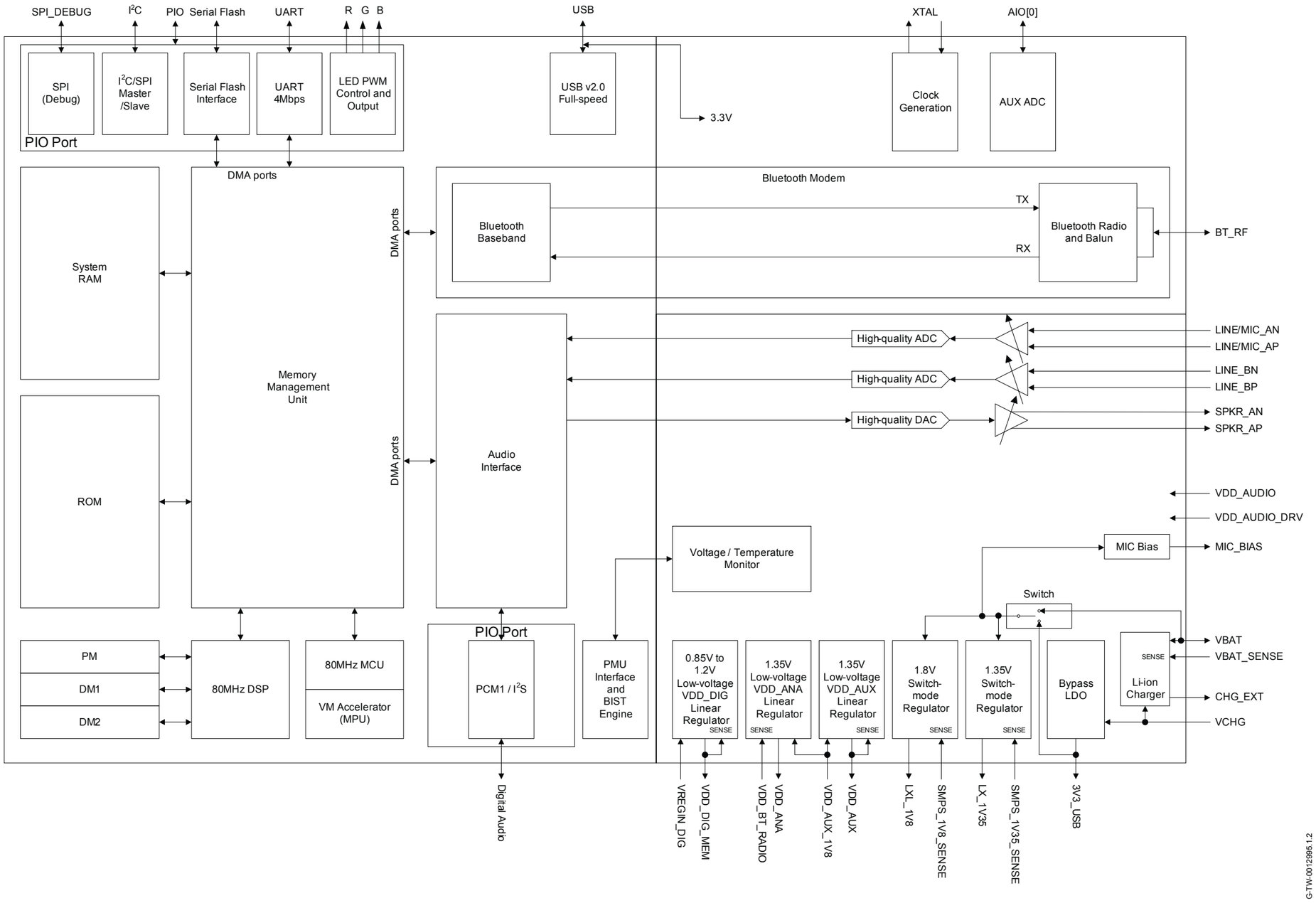
Configures the CSR8615 mono ROM solution software features:

- Bluetooth v4.0 specification features
- Reconnection policies, e.g. reconnect on power-on
- Audio features, including default volumes
- Button events: configuring button presses and durations for certain events, e.g. double press on PIO for last number redial
- LED indications for states, e.g. device connected, and events, e.g. power on
- Indication tones for events and ringtones
- Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
- Advanced Multipoint settings

CSR8615 Mono ROM Solution Development Kit

- CSR8615 mono ROM solution demonstrator board (DB-8615-10162-1A)
- Interface adapters and cables are available
- Works in conjunction with the CSR8600 ROM Series Configuration Tool and other supporting utilities

Functional Block Diagram



Document History

Revision	Date	Change Reason
1	26 JUL 13	Original publication of this document.
2	20 AUG 13	Updates include: ■ Engineering Sample release added. ■ AVRCP v1.4 added. ■ HFP and HSP profiles added. ■ PCM interface for HCI only. ■ Minor editorial updates.

Status Information

The status of this Data Sheet is **Engineering Sample**. CSR Product Data Sheets progress according to the following format:

- **Advance Information:**
  - Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
- **Engineering Sample:**
  - Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
  - All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.
- **Pre-production Information:**
  - Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
  - All electrical specifications may be changed by CSR without notice.
- **Production Information:**
  - Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.
  - Production Data Sheets supersede all previous document versions.

Device Implementation

Important Note:

As the feature-set of the CSR8615 QFN is firmware build-specific, see the relevant software release note for the exact implementation of features on the CSR8615 QFN.

Life Support Policy and Use in Safety-critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

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CSR8615 QFN devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). CSR8615 QFN devices are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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Refer to www.csrsupport.com for compliance and conformance to standards information.

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1 Package Information

1.1 Pinout Diagram

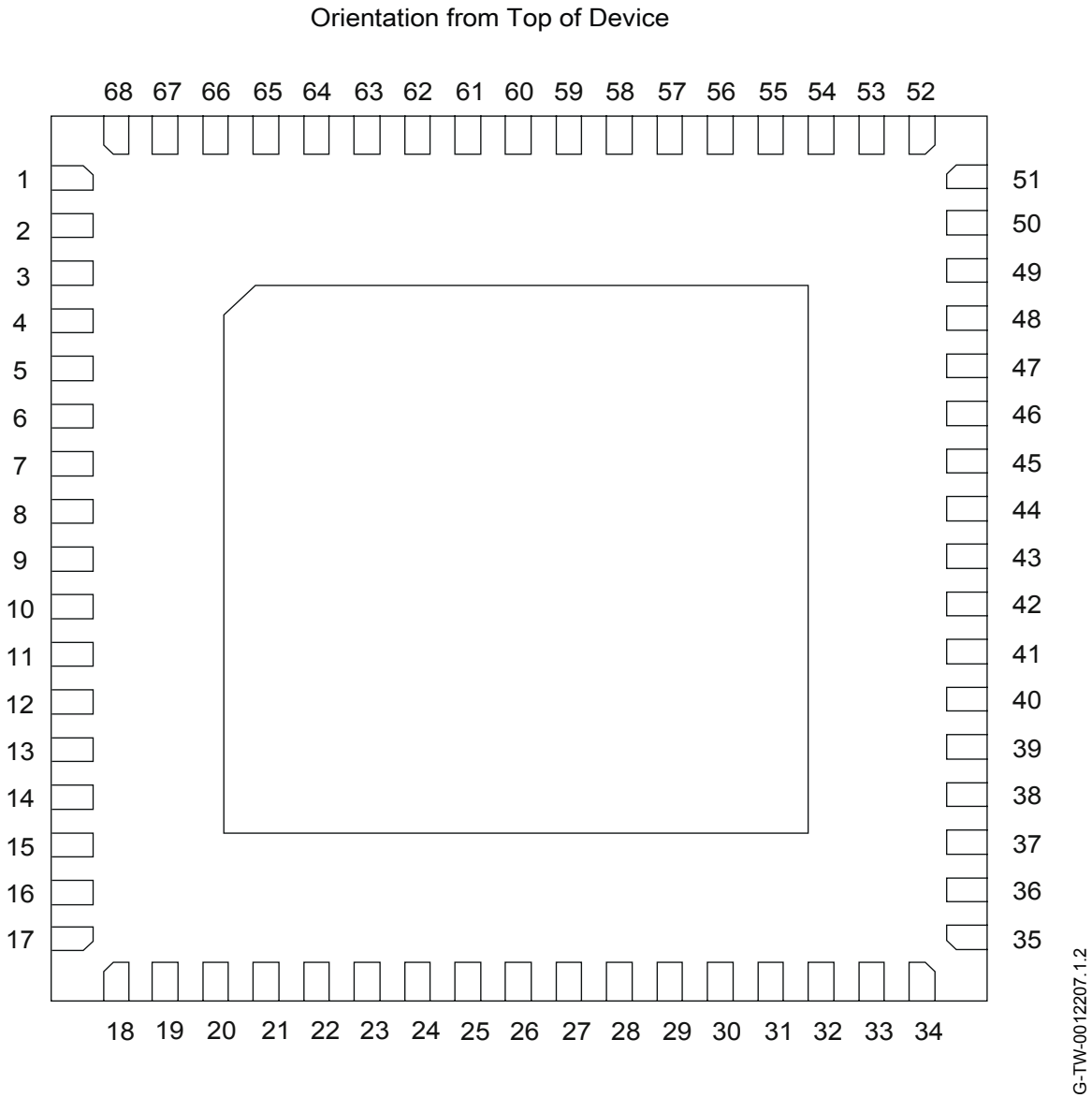


Figure 1.1: Device Pinout

1.2 Device Terminal Functions

Radio	Lead	Pad Type	Supply Domain	Description
BT_RF	12	RF	VDD_BT_RADIO	Bluetooth 50Ω transmitter output / receiver input

Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	19	Analogue	VDD_AUX	For crystal or external clock input
XTAL_OUT	18			Drive for crystal

USB	Lead	Pad Type	Supply Domain	Description
USB_DP	56	Bidirectional	VDD_USB	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	55			USB data minus

SPI/PCM Interface	Lead	Pad Type	Supply Domain	Description
SPI_PCM#_SEL	29	Input with weak pull-down	VDD_PADS_1	SPI/PCM select input: ■ 0 = PCM/PIO interface ■ 1 = SPI

Note:

SPI and PCM1 interfaces are mapped as alternative functions on the PIO port.

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[21]	64	Bidirectional with weak pull-down	VDD_PADS_2	Programmable input / output line 21.
PIO[18]	65	Bidirectional with weak pull-down	VDD_PADS_2	Programmable input / output line 18.
PIO[17]	32	Bidirectional with strong pull-down	VDD_PADS_1	Programmable input / output line 17. Alternative function: ■ UART_CTS: UART clear to send, active low
PIO[16]	27	Bidirectional with strong pull-up	VDD_PADS_1	Programmable input / output line 16. Alternative function: ■ UART_RTS: UART request to send, active low
PIO[15]	21	Bidirectional with strong pull-up	VDD_PADS_1	Programmable input / output line 15. Alternative function: ■ UART_TX: UART data output

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[14]	23	Bidirectional with strong pull-up	VDD_PADS_1	Programmable input / output line 14. Alternative function: ■ UART_RX: UART data input
PIO[13]	31	Bidirectional with strong pull-down	VDD_PADS_1	Programmable input / output line 13. Alternative function: ■ QSPI_IO[1]: SPI flash data bit 1
PIO[12]	22	Bidirectional with strong pull-up	VDD_PADS_1	Programmable input / output line 12. Alternative function: ■ QSPI_FLASH_CS#: SPI flash chip select ■ I2C_WP: I²C bus memory write protect line
PIO[11]	26	Bidirectional with strong pull-down	VDD_PADS_1	Programmable input / output line 11. Alternative function: ■ QSPI_IO[0]: SPI flash data bit 0 ■ I2C_SDA: I²C serial data line
PIO[10]	25	Bidirectional with strong pull-down	VDD_PADS_1	Programmable input / output line 10. Alternative function: ■ QSPI_FLASH_CLK: SPI flash clock ■ I2C_SCL: I²C serial clock line
PIO[9]	58	Bidirectional with strong pull-down	VDD_PADS_2	Programmable input / output line 9. Alternative function: ■ UART_CTS: UART clear to send, active low
PIO[8]	61	Bidirectional with strong pull-up	VDD_PADS_2	Programmable input / output line 8. Alternative function: ■ UART_RTS: UART request to send, active low
PIO[7]	57	Bidirectional with strong pull-down	VDD_PADS_2	Programmable input / output line 7.
PIO[6]	62	Bidirectional with strong pull-down	VDD_PADS_2	Programmable input / output line 6.
PIO[5]	34	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 5. Alternative function: ■ SPI_CLK: SPI clock ■ PCM1_CLK: PCM1 synchronous data clock

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[4]	24	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 4. Alternative function: ■ SPI_CS#: chip select for SPI, active low ■ PCM1_SYNC: PCM1 synchronous data sync
PIO[3]	28	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 3. Alternative function: ■ SPI_MISO: SPI data output ■ PCM1_OUT: PCM1 synchronous data output
PIO[2]	30	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 2. Alternative function: ■ SPI_MOSI: SPI data input ■ PCM1_IN: PCM1 synchronous data input
PIO[1]	60	Bidirectional with strong pull-up	VDD_PADS_2	Programmable input / output line 1. Alternative function: ■ UART_TX: UART data output
PIO[0]	59	Bidirectional with strong pull-up	VDD_PADS_2	Programmable input / output line 0. Alternative function: ■ UART_RX: UART data input
AIO[0]	20	Bidirectional	VDD_AUX	Analogue programmable input / output line 0.

Test and Debug	Lead	Pad Type	Supply Domain	Description
RST#	35	Input with strong pull-up	VDD_PADS_1	Reset if low. Pull low for minimum 5ms to cause a reset.

Codec	Lead	Pad Type	Supply Domain	Description
MIC_BIAS	2	Analogue in	VDD_AUDIO	Microphone bias
AU_REF	1			Decoupling of audio reference (for high-quality audio)
SPKR_AN	9	Analogue out	VDD_AUDIO_DRV	Speaker output negative, left
SPKR_AP	10			Speaker output positive, left
LINE/MIC_AN	67	Analogue in	VDD_AUDIO	Line or microphone input negative, channel A
LINE/MIC_AP	68			Line or microphone input positive, channel A
LINE_BN	4	Analogue in	VDD_AUDIO	Line input negative, channel B
LINE_BP	5			Line input positive, channel B

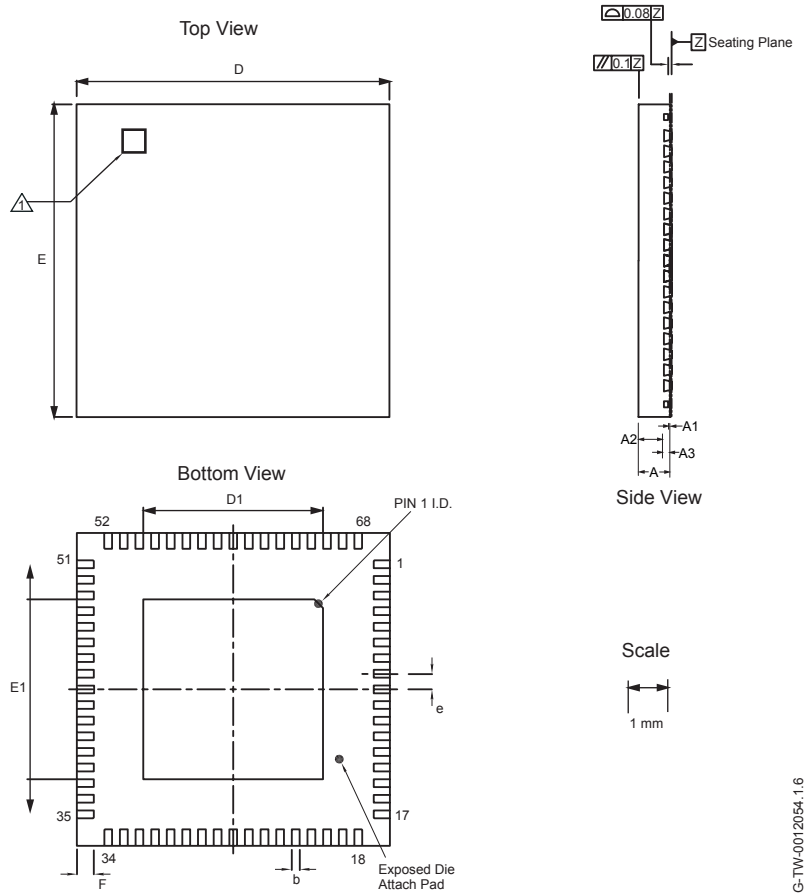
LED Drivers	Lead	Pad Type	Supply Domain	Description
LED[2]	66	Bidirectional	VDD_PADS_2	LED driver. Alternative function: programmable output PIO[31] **Note:** As output is open-drain, an external pull-up is required when PIO[31] is configured as a programmable output.
LED[1]	36	Bidirectional	VDD_PADS_1	LED driver. Alternative function: programmable output PIO[30]. **Note:** As output is open-drain, an external pull-up is required when PIO[30] is configured as a programmable output.
LED[0]	37	Bidirectional	VDD_PADS_1	LED driver. Alternative function: programmable output PIO[29]. **Note:** As output is open-drain, an external pull-up is required when PIO[29] is configured as a programmable output.

Power Supplies and Control	Lead	Description
CHG_EXT	43	External battery charger control. External battery charger transistor base control when using external charger boost. Otherwise leave unconnected.
LX_1V35	50	1.35V switch-mode power regulator inductor connection.
LX_1V8	47	1.8V switch-mode power regulator inductor connection.
SMPS_1V35_SENSE	52	1.35V switch-mode power regulator sense input.
SMPS_1V8_SENSE	53	1.8V switch-mode power regulator sense input.
SMP_BYP	49	Alternative supply via bypass regulator for 1.8V and 1.35V switchmode power supply regulator inputs. Must be connected to the same potential as VOUT_3V3.
SMP_VBAT	48	1.8V and 1.35V switch-mode power supply regulator inputs. Must be at the same potential as VBAT.
VSS_SMPS_1V35	51	1.35V switch-mode regulator ground.
VSS_SMPS_1V8	46	1.8V switch-mode regulator ground.
VBAT	45	Battery positive terminal.
VBAT_SENSE	44	Battery charger sense input. Connect directly to the battery positive pin.
VCHG	42	Charger input. Typically connected to VBUS (USB supply) as Section 12 shows.
VDD_ANA	17	Analogue LDO linear regulator output (1.35V). Connect to 1.35V supply, see Section 12 for connections.
VDD_AUDIO	3	Positive supply for audio. Connect to 1.35V supply, see Section 12 for connections.
VDD_AUDIO_DRV	8	Positive supply for audio output amplifiers. Connect to 1.8V supply, see Section 12 for connections.
VDD_AUX	14	Auxiliary supply. Connect to 1.35V supply, see Section 12 for connections.
VDD_AUX_1V8	15, 16	Auxiliary LDO regulator input. Connect to 1.8V supply, see Section 12 for connections.
VDD_BT_LO	13	Bluetooth radio local oscillator supply (1.35V). Connect to 1.35V supply, see Section 12 for connections.
VDD_BT_RADIO	11	Bluetooth radio supply. Connect to 1.35V supply, see Section 12 for connections.

Power Supplies and Control	Lead	Description
VDD_DIG_MEM	38	Digital LDO regulator output, see Section 12 for connections.
VDD_PADS_1	33	Positive supply input for input/output ports.
VDD_PADS_2	63	Positive supply input for input/output ports.
VDD_USB	54	Positive supply for USB port.
VOUT_3V3	41	3.3V bypass linear regulator output. Connect external minimum 2.2µF ceramic decoupling capacitor.
VREGENABLE	40	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
VREGIN_DIG	39	Digital LDO regulator input, see Section 12 for connections. Typically connected to a 1.35V supply.
VSS	Exposed pad	Ground connections.

Unconnected Terminals	Lead	Description
NC	6, 7	Leave unconnected

1.3 Package Dimensions



Description	Min	Typ	Max	Description	Min	Typ	Max
A	0.80	0.85	0.90	E	7.90	8.00	8.10
A1	0.00	0.035	0.05	e	-	0.40	-
A2	-	0.65	0.67	D1	4.50	4.60	4.70
A3	-	0.203	-	E1	4.50	4.60	4.70
b	0.15	0.20	0.25	F	0.35	0.40	0.45
D	7.90	8.00	8.10	-			

Notes	1. Top side polarity mark. The dimensions of the square polarity mark are 0.75 x 0.75mm. Coplanarity applies to leads, corner leads and die attach pad.		
Description	QFN		
Size	8 x 8 x 0.9mm	**JEDEC**	MO-220
Pitch	0.4mm pitch	**Units**	mm

1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8 x 0.9mm QFN 68-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.5 Typical Solder Reflow Profile

For information, see *Typical Solder Reflow Profile for Lead-free Devices Information Note*.

2 Bluetooth Modem

2.1 RF Ports

2.1.1 BT_RF

CSR8615 QFN contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power into a 50Ω load.

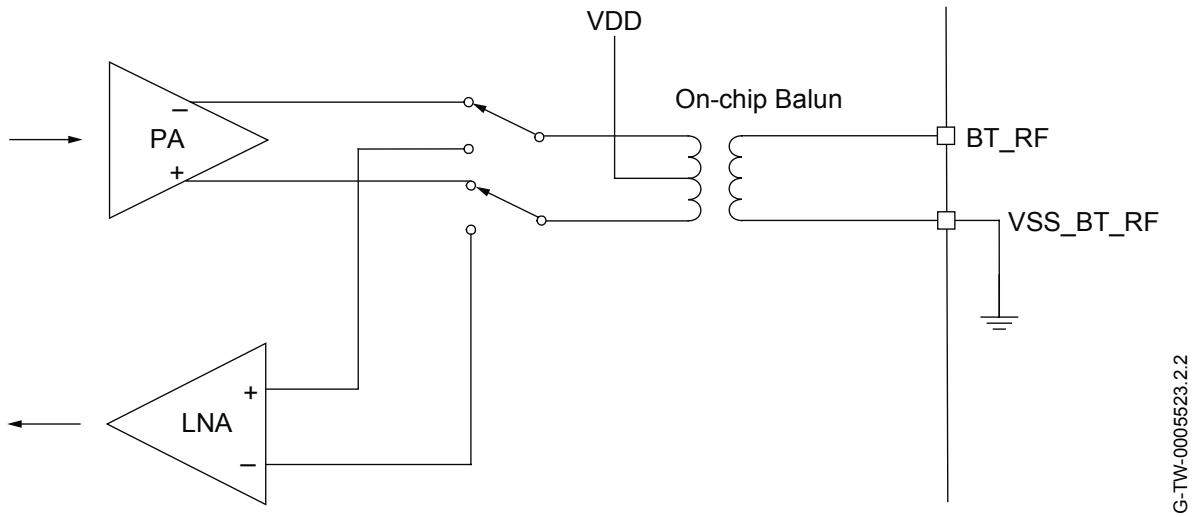


Figure 2.1: Simplified Circuit BT_RF

2.2 RF Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. A digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise enables CSR8615 QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the CSR8615 QFN has a maximum output power that enables it to operate as a Class 1, Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.0 specification.

2.5 Baseband

2.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

2.5.2 Physical Layer Hardware Engine

Dedicated logic performs:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of the Bluetooth v4.0 specification including AFH and eSCO.

3 Clock Generation

CSR8615 QFN accepts a reference clock input from either a crystal or an external clock source, e.g. a TCXO.

The external reference clock is required in active and deep sleep modes and must be present when CSR8615 QFN is enabled.

3.1 Crystal

CSR8615 QFN contains a crystal driver circuit that acts as a transconductance amplifier that drives an external crystal connected between XTAL_IN and XTAL_OUT. The crystal driver circuit forms a Pierce oscillator with the external crystal. External capacitors are not required for standard crystals that require a load capacitance of around 9pF. CSR recommends this option.

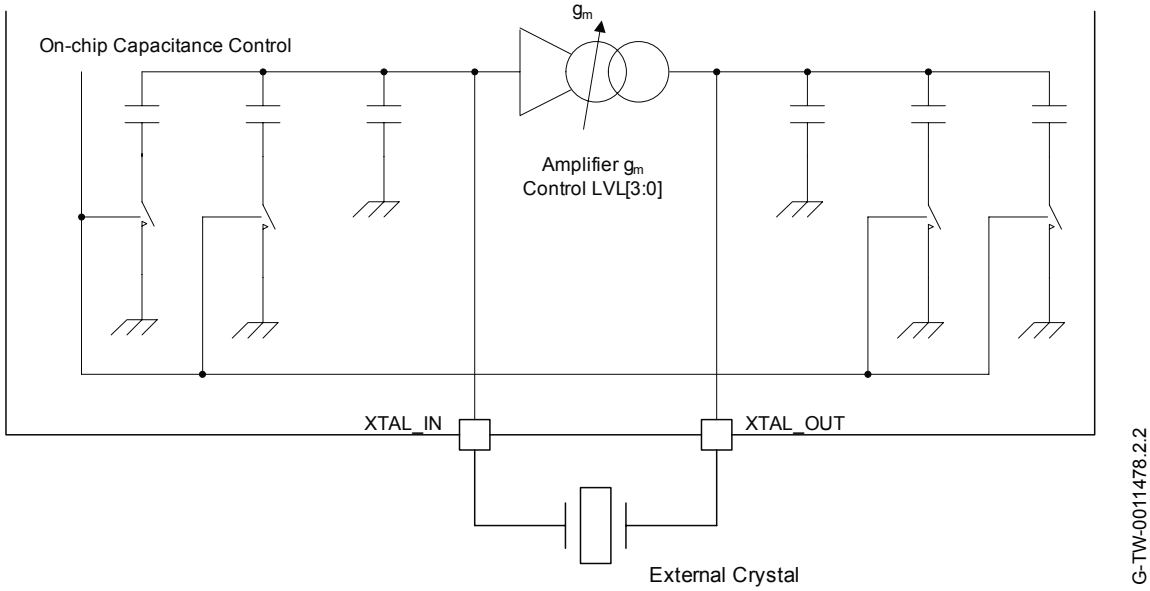


Figure 3.1: Crystal Oscillator Overview

The on-chip capacitance is adjusted using PSKEY_XTAL_OSC_CONFIG, see Table 3.1. The default values suit a typical crystal requiring a 9pF load capacitance. In deep sleep mode, the crystal oscillation is maintained, but at a lower drive strength to reduce power consumption. The drive strength and load capacitance are configured with a PS Key.

	Normal Mode PSKEY_XTAL_OSC_CONFIG [3:2]				Low Power Mode PSKEY_XTAL_OSC_CONFIG [1:0]			
Value	00	01	10	11	00	01	10	11
XTAL_IN (Typical)	15.6 pF	10.8 pF	6.0 pF	1.1 pF	15.6 pF	10.8 pF	6.0 pF	1.1 pF
XTAL_OUT (Typical)	20.8 pF	16.0 pF	11.2 pF	6.4 pF	16.0 pF	11.2 pF	6.4 pF	1.5 pF

Table 3.1: Typical On-chip Capacitance Values

The drive strength is configured with PSKEY_XTAL_LVL. The default level for this PS Key is sufficient for typical crystals. The level control is set in the range 0 to 15, where 15 is the maximum drive level.

Increasing the crystal amplifier drive level increases the transconductance of the crystal amplifier, which creates an increase in the oscillator margin (ratio of oscillator amplifiers is equivalent to the negative resistance of the crystal ESR).

Note:

Excessive amplifier transconductance can lead to an increase in the oscillator phase noise if the oscillator amplifier is excessively overdriven. Set the transconductance to the minimum level to give the desired oscillation ratio. Higher values can increase power consumption. Also, insufficient drive strength can prevent the the crystal from starting to oscillate.

3.1.1 Negative Resistance Model

The crystal and its load capacitor can be modelled as a frequency dependant resistive element. Consider the driver amplifier as a circuit that provides negative resistance. For oscillation, the value of the negative resistance should be greater than that of the crystal circuit equivalence resistance. Equation 3.1 shows how to calculate the equivalent negative resistance.

$$R_{neg} = -\frac{g_m C_{in} C_{out}}{2\pi f^2 (C_{out} C_{in} + (C_0 + C_{int})(C_{out} + C_{in}))^2}$$

Equation 3.1: Negative Resistance

Where:

- g_m = Transconductance of the crystal oscillator amplifier
- C_o = Static capacitance of the crystal, which is sometimes referred to as the shunt or case capacitance
- C_{int} = On-chip parasitic capacitance between input and output of XTAL amplifier.
- C_{in} = Internal capacitance on XTAL_IN, see Table 3.1
- C_{out} = Internal capacitance on XTAL_OUT, see Table 3.1

Parameter	Min	Typ	Max	Unit
Transconductance	2	-	-	mS
C_{int}	-	1.5	-	pF

Table 3.2: Transconductance and On-chip Parasitic Capacitance

3.1.2 Crystal Specification

Table 3.3 shows the specification for an external crystal.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	32	MHz
Initial Frequency error from nominal frequency which can be compensated for	-	-	±285	ppm
Frequency Stability	-	-	±20	ppm
Crystal ESR	-	-	60	Ω

Table 3.3: Crystal Specification

3.1.3 Crystal Calibration

The actual crystal frequency depends on the capacitance of XTAL_IN and XTAL_OUT on the PCB and the CSR8615 QFN, as well as the capacitance of the crystal.

The Bluetooth specification requires ±20ppm clock accuracy. The actual frequency at which a crystal oscillates contains two error terms, which are typically mentioned in the crystal device datasheets:

- Initial Frequency Error: The difference between the desired frequency and the actual oscillating frequency caused by the crystal itself and its PCB connections. It is also called as Calibration Tolerance or Frequency Tolerance.
- Frequency Stability: The total of how far the crystal can move off frequency with temperature, aging or other effects. It is also called as Temperature Stability, Frequency Stability or Aging.

CSR8615 QFN has the capability to compensate for Initial Frequency errors by a simple per-device basis on the production line, with the trim value stored in the non-volatile memory (PS Key). However, it is not possible to compensate for frequency stability, therefore a crystal must be chosen with a Frequency Stability that is better than ±20 ppm clock accuracy.

Some crystal datasheets combine both these terms into one tolerance value. This causes a problem because only the initial frequency error can be compensated for and CSR8615 QFN cannot compensate for the temperature or aging performance. If frequency stability is not explicity stated, CSR cannot guarantee remaining within the Bluetooth's ±20ppm frequency accuracy specification.

Crystal calibration uses a single measurement of RF output frequency and can be performed quickly as part of the product final test. Typically, a TXSTART radio command is sent and then a measurement of the output RF frequency is read . From this, the calibration factor to correct actual offset from the desired frequency can be calculated. This offset value is stored in PSKEY_ANA_FTRIM_OFFSET. CSR8615 QFN then compensates for the initial frequency offset of the crystal.

The value in PSKEY_ANA_FTRIM_OFFSET is a 16-bit 2's complement signed integer which specifies the fractional part of the ratio between the true crystal frequency, f_{actual}, and the value set in PSKEY_ANA_FREQ, $f_{nominal}$. Equation 3.2 shows the value of PSKEY_ANA_FTRIM_OFFSET in parts per 2^{20} rounded to the nearest integer.

For more information on TXSTART radio test see *BlueTest User Guide*.

$$\text{PSKEY\_ANA\_FTRIM\_OFFSET} = \left(\frac{f_{actual}}{f_{nominal}} - 1\right) \times 2^{20}$$

Equation 3.2: Crystal Calibration Using PSKEY_ANA_FTRIM_OFFSET

3.2 Non-crystal Oscillator

Apply the external reference clock to the CSR8615 QFN XTAL_IN input. Connect XTAL_OUT to ground.

The external clock is either a low-level sinusoid, or a digital-level square wave. The clock must meet the specification in Table 3.4. The external reference clock is required in active and deep sleep modes, it must be present when CSR8615 QFN is enabled.

		Min	Typ	Max	Unit
Frequency[a]		19.2	26	40	MHz
Duty cycle		40:60	50:50	60:40	-
Edge jitter (at zero crossing)		-	-	10	ps rms[b]
Signal level	AC coupled sinusoid amplitude	0.2	0.4	VDD_AUX[c]	V
	DC coupled digital extremes	0	-	VDD_AUX[c]	V
	DC coupled digital digital amplitude	0.4	-	1.2	V pk-pk
XTAL_IN input impedance		30	-	-	kΩ
XTAL_IN input capacitance		-	-	1	pF

Table 3.4: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] 100Hz to 1MHz

[c] VDD_AUX is 1.35V nominal

3.2.1 XTAL_IN Impedance in Non-crystal Mode

The impedance of XTAL_IN does not change significantly between operating modes. When transitioning from deep sleep to active states, the capacitive load can change. For this reason, CSR recommends using a buffered clock input.

4 Bluetooth Stack Microcontroller

The CSR8615 QFN uses a 16-bit RISC 80MHz MCU for low power consumption and efficient use of memory. It contains a single-cycle multiplier and a memory protection unit for the VM accelerator, see Section 4.1.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

4.1 VM Accelerator

CSR8615 QFN contains a VM accelerator alongside the MCU. This hardware accelerator improves the performance of VM applications.

5 Kalimba DSP

The Kalimba DSP is an open platform DSP enabling signal processing functions to be performed on over-air data or codec data to enhance audio applications. Figure 5.1 shows the Kalimba DSP interfaces to other functional blocks within CSR8615 QFN.

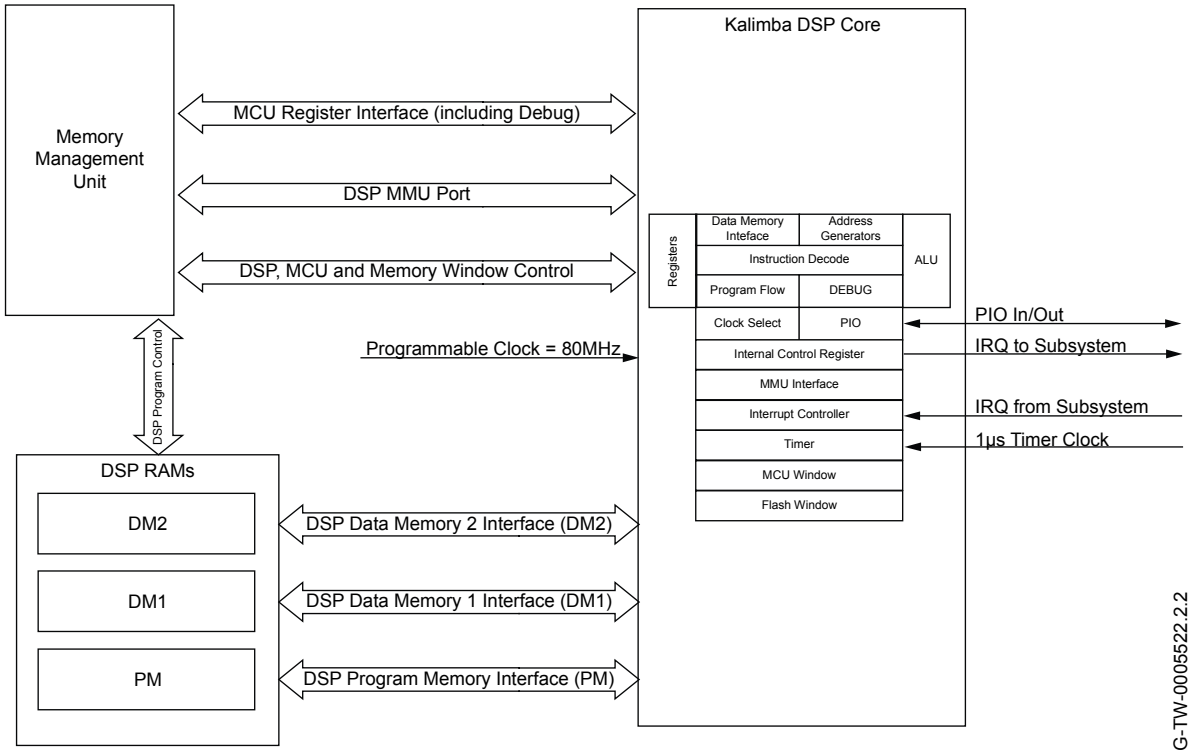


Figure 5.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 80MIPS performance, 24-bit fixed point DSP core
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulate includes 2 rMAC registers and new instructions for improved performance over previous architecture
- 32-bit instruction word
- Separate program memory and dual data memory, enabling an ALU operation and up to 2 memory accesses in a single cycle
- Zero overhead looping, including a very low-power 32-instruction cache
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 56-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

For more information see *Kalimba Architecture 3 DSP User Guide*.

6 Memory Interface and Management

6.1 Memory Management Unit

The MMU provides dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers. The use of DMA ports also helps with efficient transfer of data to other peripherals.

6.2 System RAM

56KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

6.3 Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 16K x 24-bit for data memory 1 (DM1)
- 16K x 24-bit for data memory 2 (DM2)
- 6K x 32-bit for program memory (PM)

6.4 Internal ROM

Internal ROM is provided for system firmware implementation.

6.5 Serial Flash Interface

CSR8615 QFN supports external serial flash ICs. This enables additional data storage areas for device-specific data. CSR8615 QFN supports serial single I/O devices with a 1-bit I/O flash-memory interface.

Figure 6.1 shows a typical connection between CSR8615 QFN and a serial flash IC.

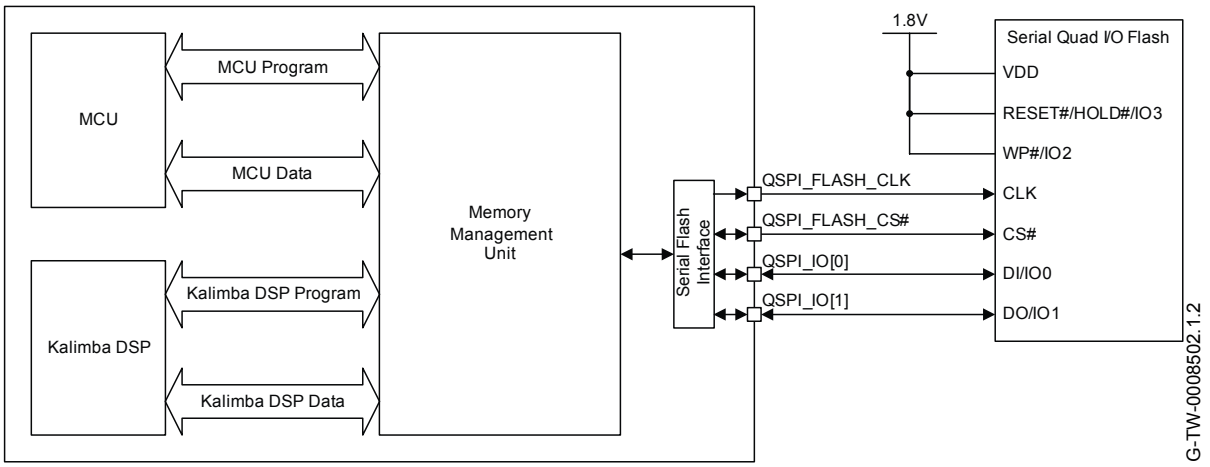


Figure 6.1: Serial Flash Interface

CSR8615 QFN supports Winbond, Microchip/SST, Macronix (and compatible) selected serial flash devices for PS Key and voice prompt storage up to 16Mb, see firmware release note for up-to-date device support.

7 Serial Interfaces

7.1 USB Interface

CSR8615 QFN has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on CSR8615 QFN acts as a USB peripheral, responding to requests from a master host controller.

CSR8615 QFN contains internal USB termination resistors and requires no external resistor matching.

CSR8615 QFN supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, supports USB standard charger detection and fully supports the *USB Battery Charging Specification*, available from http://www.usb.org. For more information on how to integrate the USB interface on CSR8615 QFN see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

7.2 UART Interface

CSR8615 QFN has one optional standard UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug. The UART interface is multiplexed with PIOs and other functions, and hardware flow control is optional. PS Keys configure this multiplexing, see Table 7.1.

PS Key	PIO Location Option
PSKEY_UART_RX_PIO	PIO[0] (default) or PIO[14]
PSKEY_UART_TX_PIO	PIO[1] (default) or PIO[15]
PSKEY_UART_RTS_PIO	PIO[8] (default) or PIO[16]
PSKEY_UART_CTS_PIO	PIO[9] (default) or PIO[17]

Table 7.1: PS Keys for UART/PIO Multiplexing

Figure 7.1 shows the 4 signals that implement the UART function.

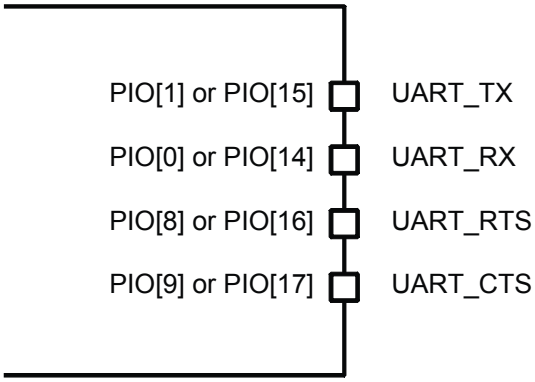


Figure 7.1: Universal Asynchronous Receiver

When CSR8615 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using CSR8615 QFN firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 7.2 shows the possible UART settings.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 7.2: Possible UART Settings

Table 7.3 lists common baud rates and their associated values for the PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range is set in the PS Key according to the formula in Equation 7.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 7.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 7.3: Standard Baud Rates

7.3 Programming and Debug Interface

CSR8615 QFN provides a debug SPI interface for programming, configuring (PS Keys) and debugging the CSR8615 QFN. Access to this interface is required in production. Ensure the 4 SPI signals and the SPI_PCM# line are brought out to either test points or a header. To use the SPI interface, the SPI_PCM# line requires the option of being pulled high externally.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

7.3.1 Multi-slave Operation

Avoid connecting CSR8615 QFN in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSR8615 QFN is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, CSR8615 QFN outputs 0 if the processor is running or 1 if it is stopped.

7.4 I²C EEPROM Interface

CSR8615 QFN supports optional I²C EEPROM for storage of PS Keys and voice prompt data if SPI flash is not used. Figure 7.2 shows an example I²C EEPROM connection where:

- PIO[10] is the I²C EEPROM SCL line
- PIO[11] is the I²C EEPROM SDA line
- PIO[12] is the I²C EEPROM WP line

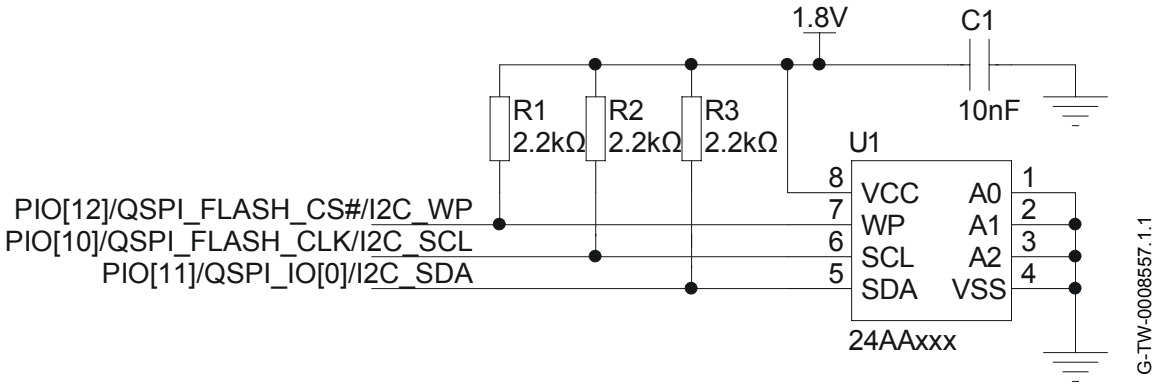


Figure 7.2: Example I²C EEPROM Connection

Note:

The I²C EEPROM requires external pull-up resistors, see Figure 7.2. Ensure that external pull-up resistors are suitably sized for the I²C interface speed and PCB track capacitance.

To minimise boot time, CSR recommends using 400kHz capable I²C EEPROMs and I2C_CONFIG and ANA_FREQ should be the first 2 keys in the EEPROM PS-store image.

EEPROMs must be suitable for operation at 1.8V.

8 Interfaces

8.1 Programmable I/O Ports, PIO

CSR8615 QFN provides 20 lines of programmable bidirectional I/O, PIO[21,18:0]. Some of the PIOs on the CSR8615 QFN have alternative functions, see Table 8.1.

PIO	Function				
	Debug SPI (See Section 7.3)	SPI Flash (See Section 6.5)	UART (See Section 7.2)	PCM (See Section 9.3)	EEPROM (See Section 7.4)
PIO[0]	-	-	UART_RX (default)	-	-
PIO[1]	-	-	UART_TX (default)	-	-
PIO[2]	SPI_MOSI	-	-	PCM1_IN	-
PIO[3]	SPI_MISO	-	-	PCM1_OUT	-
PIO[4]	SPI_CS#	-	-	PCM1_SYNC	-
PIO[5]	SPI_CLK	-	-	PCM1_CLK	-
PIO[8]	-	-	UART_RTS (default)	-	-
PIO[9]	-	-	UART_CTS (default)	-	-
PIO[10]	-	QSPI_FLASH_CLK	-	-	I2C_SCL
PIO[11]	-	QSPI_IO[0]	-	-	I2C_SDA
PIO[12]	-	QSPI_FLASH_CS#	-	-	I2C_WP
PIO[13]	-	QSPI_IO[1]	-	-	-
PIO[14]	-	-	UART_RX	-	-
PIO[15]	-	-	UART_TX	-	-
PIO[16]	-	-	UART_RTS	-	-
PIO[17]	-	-	UART_CTS	-	-

Table 8.1: Alternative PIO Functions

Note:

See the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

8.2 Analogue I/O Ports, AIO

CSR8615 QFN has 1 general-purpose analogue interface pin, AIO[0]. Typically, this connects to a thermistor for battery pack temperature measurements during charge control. See Section 12 for typical connections.

8.3 LED Drivers

CSR8615 QFN includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

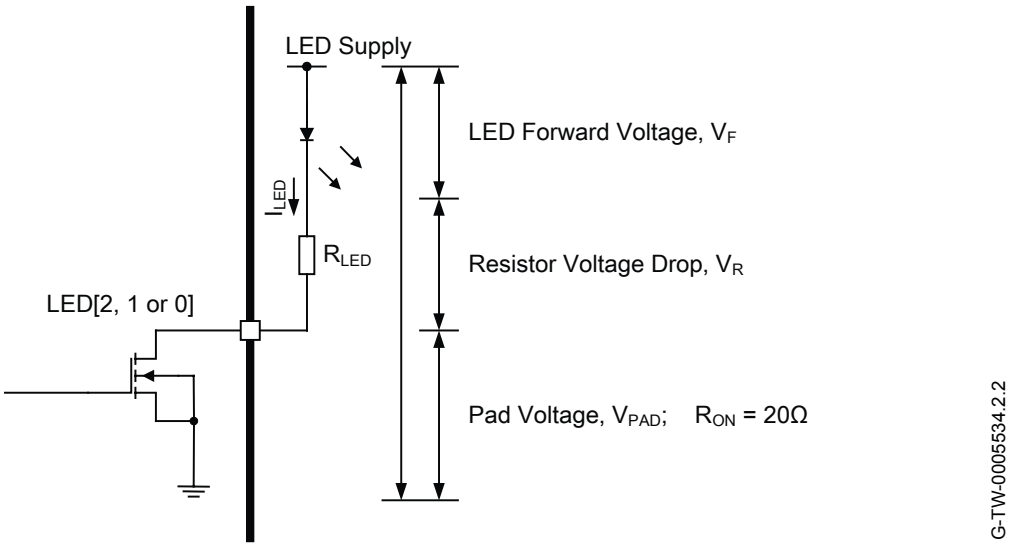


Figure 8.1: LED Equivalent Circuit

From Figure 8.1 it is possible to derive Equation 8.1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 8.1: LED Current

For the LED pads to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, V_R, keeps V_{PAD} below 0.5V. Equation 8.2 also applies.

$$VDD = V_F + V_R + V_{PAD}$$

Equation 8.2: LED PAD Voltage

Note:

The supply domain in Section 1.2 for LED[2:0] must remain powered for LED functions to operate.

The LED current adds to the overall current. Conservative LED selection extends battery life.

9 Audio Interface

The audio interface circuit consists of:

- Stereo line input with 1-mic CVC input and mono output audio codec
- Dual analogue audio inputs
- Mono analogue audio output
- Configurable PCM (PCM1) and I²S interfaces, for configuration information contact CSR

Figure 9.1 shows the functional blocks of the interface. The codec supports mono playback and stereo line input recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC contains 2 independent high-quality channels and the DAC a single high-quality channel of the codec. Any of the ADC channels or the DAC channel runs at its own independent sample rate.

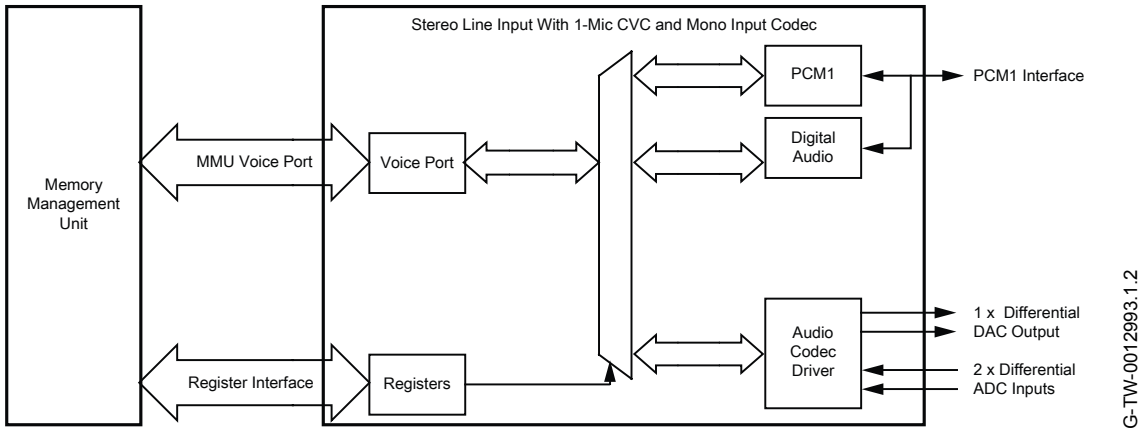


Figure 9.1: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM1 codec interface described in Section 9.3. Table 9.1 lists the alternative functions.

Important Note:

The term *PCM* in Section 9.3 and its subsections refers to the PCM1 interface.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 9.1: Alternative Functions of the Digital Audio Bus Interface on the PCM1 Interface

9.1 Audio Input and Output

The audio input circuitry consists of 2 independent 16-bit high-quality ADC channels:

- Programmable as either stereo line or 1-mic CVC input
- 1 input programmable as either microphone or line input, the other as line input only
- Each channel is independently configurable to be either single-ended or fully differential
- Each channel has an analogue and digital programmable gain stage, this also aids optimisation of different microphones

The audio output circuitry consists of a single differential class A-B output stage.

Note:

CSR8615 QFN is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

9.2 Audio Codec Interface

The main features of the interface are:

- Stereo line analogue input for voice band and audio band
- Single mono microphone analogue input for voice band and audio band
- Mono analogue output for voice band and audio band
- Support for I²S stereo digital audio bus standard
- Support for PCM interface including PCM master codecs that require an external system clock

Important Note:

To avoid any confusion regarding stereo operation this data sheet with respect to audio input, software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

9.2.1 Audio Codec Block Diagram

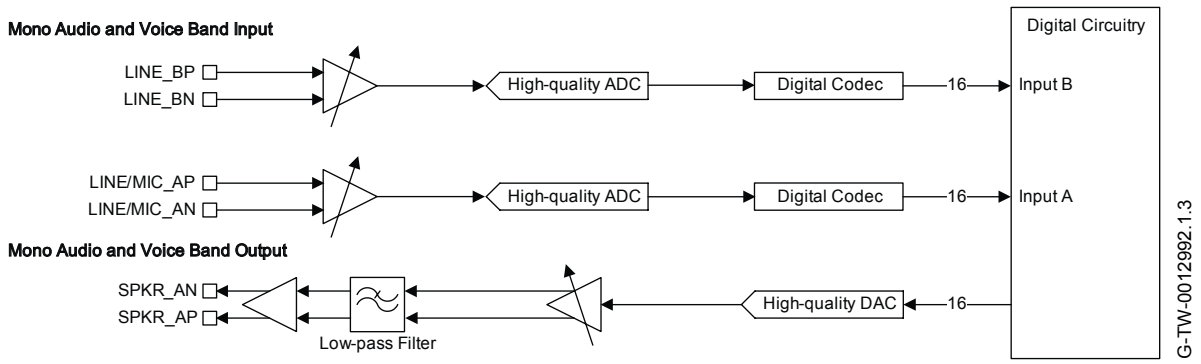


Figure 9.2: Audio Codec Input and Output Stages

The CSR8615 QFN audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO for the audio circuits and VDD_AUDIO_DRV for the audio driver circuits.

9.2.2 ADC

Figure 9.2 shows the CSR8615 QFN consists of 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage, see Section 9.2.4.

9.2.3 ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40kHz:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz

9.2.4 ADC Audio Input Gain

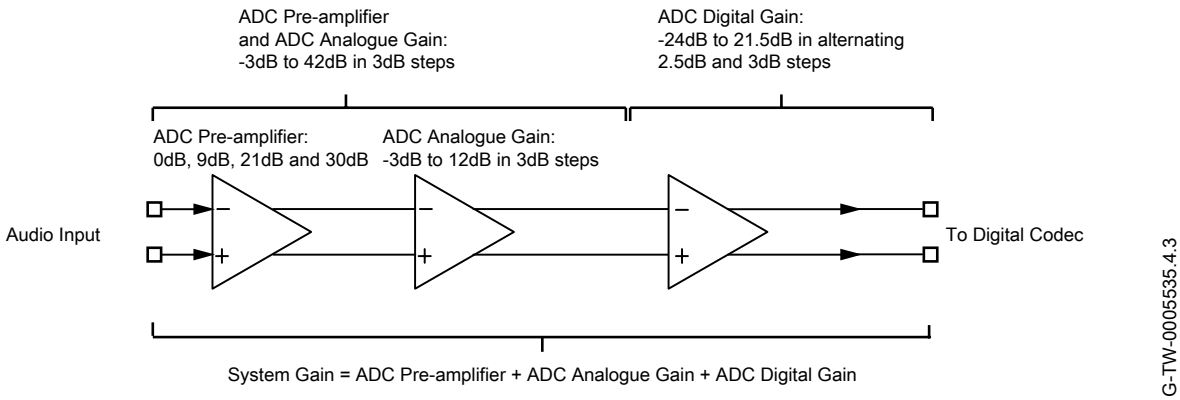


Figure 9.3: Audio Input Gain

9.2.5 ADC Pre-amplifier and ADC Analogue Gain

CSR8615 QFN has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0dB, 9dB, 21dB and 30dB
- The ADC analogue amplifier gain is -3dB to 12dB in 3dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3dB to 42dB in 3dB steps, see Figure 9.3
- At mid to high gain levels it acts as a microphone pre-amplifier, see Section 9.2.13
- At low gain levels it acts as an audio line level amplifier

9.2.6 ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see Table 9.2. There is also a *fine gain interface* with a 9-bit gain setting allowing gain changes in 1/32 steps, for more information contact CSR.

The firmware controls the audio input gain.

Digital Gain Selection Value	ADC Digital Gain Setting (dB)	Digital Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 9.2: ADC Audio Input Gain Rate

9.2.7 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A *long* IIR filter suitable for music (>44.1kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8kHz / 16kHz / voice)

For more information contact CSR.

9.2.8 DAC

The DAC consists of:

- 1 fourth-order Sigma-Delta converter, see Figure 9.2
- 2 gain stages, 1 of which is an analogue gain stage and the other is a digital gain stage

9.2.9 DAC Sample Rate Selection

Each DAC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 32kHz
- 40kHz
- 44.1kHz
- 48kHz
- 96kHz

9.2.10 DAC Digital Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB, see Table 9.3. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact CSR.

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 9.3: DAC Digital Gain Rate Selection

9.2.11 DAC Analogue Gain

Table 9.4 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

Table 9.4: DAC Analogue Gain Rate Selection

9.2.12 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default *long* FIR filter for best performance at ≥ 44.1kHz.
- A *short* FIR to reduce latency.
- A *narrow* FIR (a very sharp roll-off at Nyquist) for G.722 compliance. Best for 8kHz / 16kHz.

9.2.13 Microphone Input

CSR8615 QFN contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones. Figure 9.4 shows a biasing circuit for microphones with a sensitivity between about -40 to -60dB (0dB = 1V/Pa).

Where:

- The microphone bias generator derives its power from VBAT or 3V3_USB and requires no capacitor on its output.
- The microphone bias generator maintains regulation within the limits 70µA to 2.8mA, supporting a 2mA source typically required by 2 electret condensor microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
- Biasing resistors R1 is 2.2kΩ.
- The input impedance at LINE/MIC_AN and LINE/MIC_AP is typically 6kΩ.
- C1 and C2 are 100/150nF if bass roll-off is required to limit wind noise on the microphone.
- R1 sets the microphone load impedance and are normally around 2.2kΩ.

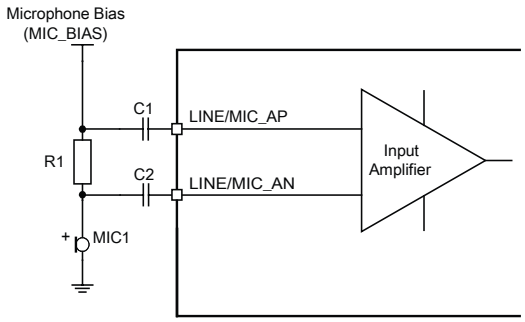


Figure 9.4: Microphone Biasing

The microphone bias characteristics include:

- Power supply:
  - CSR8615 QFN microphone supply is VBAT or 3V3_USB
  - Minimum input voltage = Output voltage + drop-out voltage
  - Maximum input voltage is 4.3V
- Drop-out voltage:
  - 300mV maximum
- Output voltage:
  - 1.8V or 2.6V
  - Tolerance 90% to 110%
- Output current:
  - 70µA to 2.8mA
- No load capacitor required

9.2.14 Line Input

Figure 9.5 and Figure 9.6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

In line input mode, the input impedance of the pins to ground varies from 6kΩ to 34kΩ depending on input gain setting.

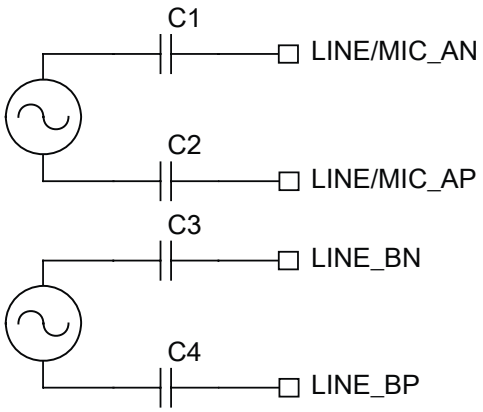


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Figure 9.5: Differential Input

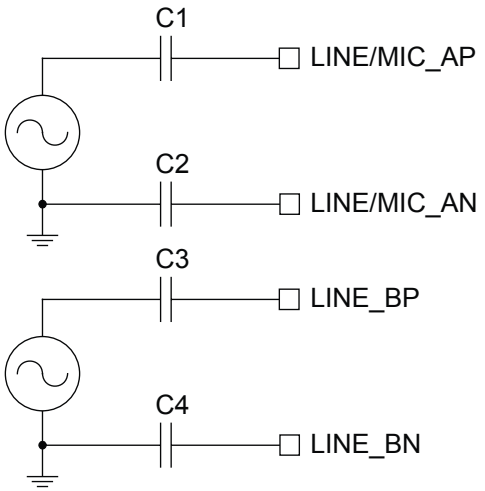

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Figure 9.6: Single-ended Input

9.2.15 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 9.7 shows that the output is available as a differential signal between SPKR_AN and SPKR_AP.

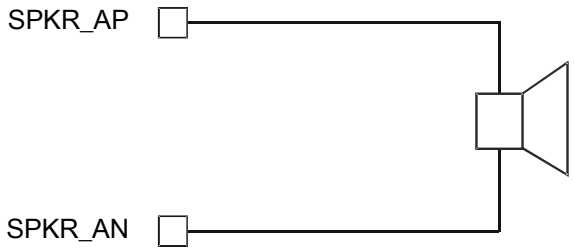

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Figure 9.7: Speaker Output

9.2.16 Side Tone

In some applications it is necessary to implement side tone. This side tone function involves feeding a properly gained microphone signal in to the DAC stream, e.g. earpiece. The side tone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface, see Figure 9.8.

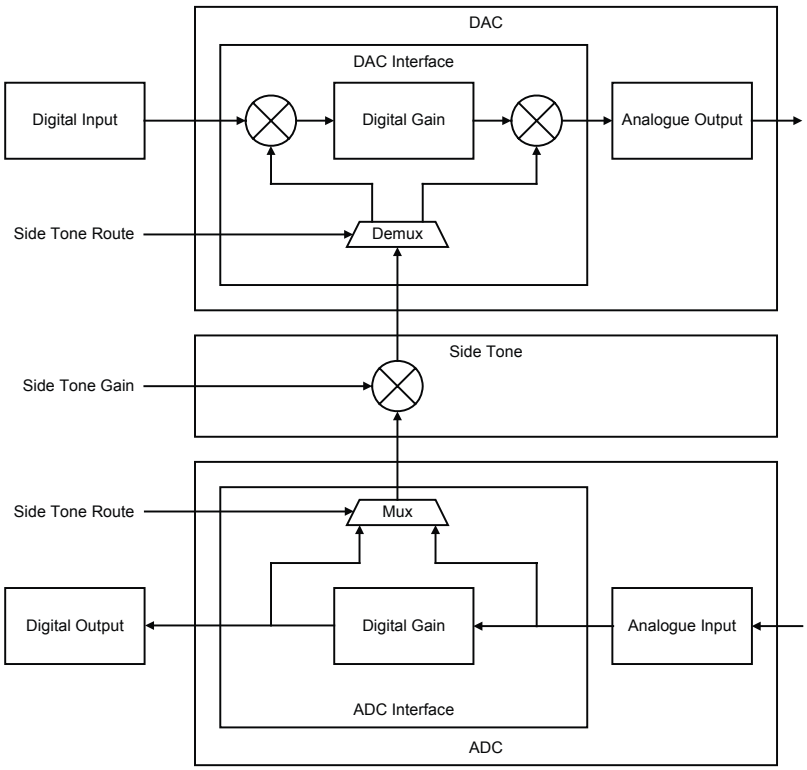

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Figure 9.8: Side Tone

The ADC provides simple gain to the side tone data. The gain values range from -32.6dB to 12.0dB in alternating steps of 2.5dB and 3.5dB, see Table 9.5.

Value	Side Tone Gain	Value	Side Tone Gain
0	-32.6dB	8	-8.5dB
1	-30.1dB	9	-6.0dB
2	-26.6dB	10	-2.5dB
3	-24.1dB	11	0dB
4	-20.6dB	12	3.5dB
5	-18.1dB	13	6.0dB
6	-14.5dB	14	9.5dB
7	-12.0dB	15	12.0dB

Table 9.5: Side Tone Gain

Note:

The values of side tone are shown for information only. During standard operation, the application software controls the side tone gain.

The following PS Keys configure the side tone hardware:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

9.2.17 Integrated Digital IIR Filter

CSR8615 QFN has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2-stage, second order IIR and is for functions such as custom wind noise reduction. The filter also has optional DC blocking.

The filter has 10 configuration words:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format `NN.NNNNNNNNNN`.

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

```
01.1111111111 = most positive number, close to 2
01.0000000000 = 1
00.0000000000 = 0
11.0000000000 = -1
10.0000000000 = -2, most negative number
```

Equation 9.1 shows the equation for the IIR filter. Equation 9.2 shows the equation for when the DC blocking is enabled.

The filter is configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps. This requires firmware support. The configuration function takes 10 variables in the following order:

```
0 : Gain
1 : b01
2 : b02
3 : a01
4 : a02
5 : b11
6 : b12
7 : a11
8 : a12
9 : DC Block (1 = enable, 0 = disable)
```

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01}\, z^{-1} + b_{02}\, z^{-2})}{(1 + a_{01}\, z^{-1} + a_{02}\, z^{-2})} \times \frac{(1 + b_{11}\, z^{-1} + b_{12}\, z^{-2})}{(1 + a_{11}\, z^{-1} + a_{12}\, z^{-2})}$$

Equation 9.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 9.2: IIR Filter Plus DC Blocking Transfer Function, $H_{DC}(z)$

9.3 PCM1 Interface

Important Note:

The PCM1 interface is provided as a test interface and is only accessible when running the CSR8615 QFN in HCI-only mode.

Section 9 describes the various digital audio interfaces multiplexed on the the PCM1 interface. The PCM1 interface also shares the same physical set of pins with the SPI interface, see Section 7.3 and Section 8.1. Either interface is selected using SPI_PCM#:

- SPI_PCM# = 1 selects SPI
- SPI_PCM# = 0 selects PCM

Important Note:

The term *PCM* refers to PCM1.

The audio PCM interface on the CSR8615 QFN supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the CSR8615 QFN for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
  - GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PSKEY_PCM_CONFIG32.

9.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSR8615 QFN generates PCM_CLK and PCM_SYNC.

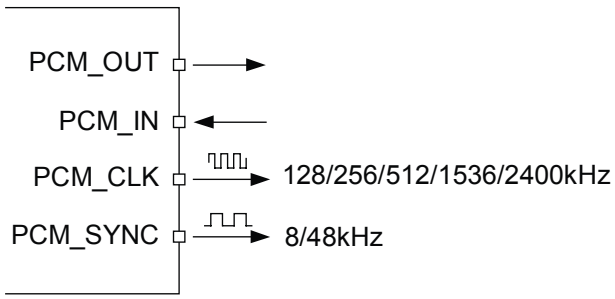

Figure 9.9: PCM Interface Master

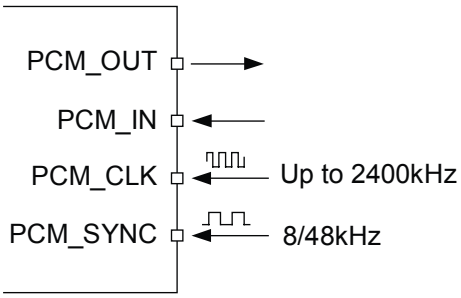

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Figure 9.10: PCM Interface Slave

9.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When CSR8615 QFN is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When CSR8615 QFN is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

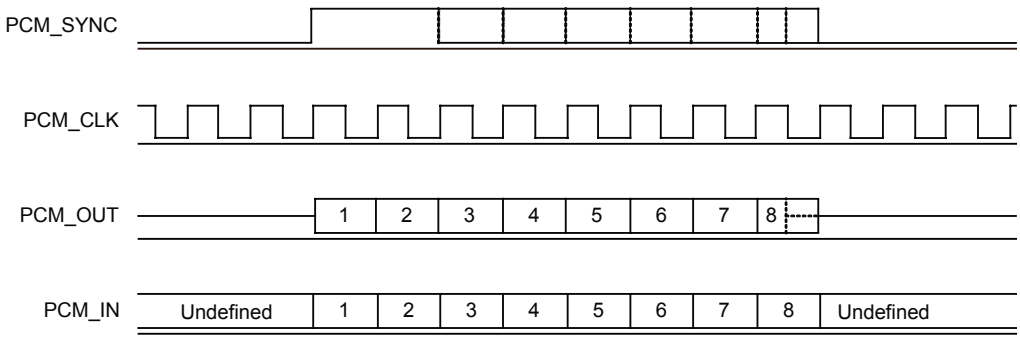

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Figure 9.11: Long Frame Sync (Shown with 8-bit Companded Sample)

CSR8615 QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always 1 clock cycle long.

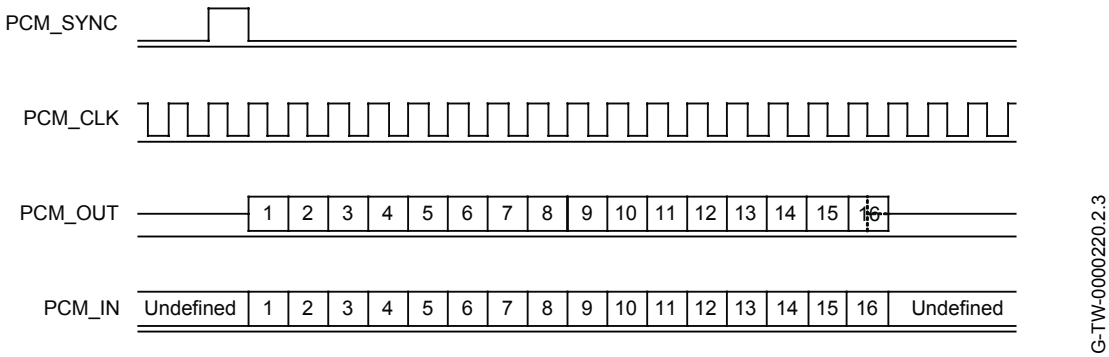


Figure 9.12: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, CSR8615 QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.3.4 Multi-slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any of the first 4 slots.

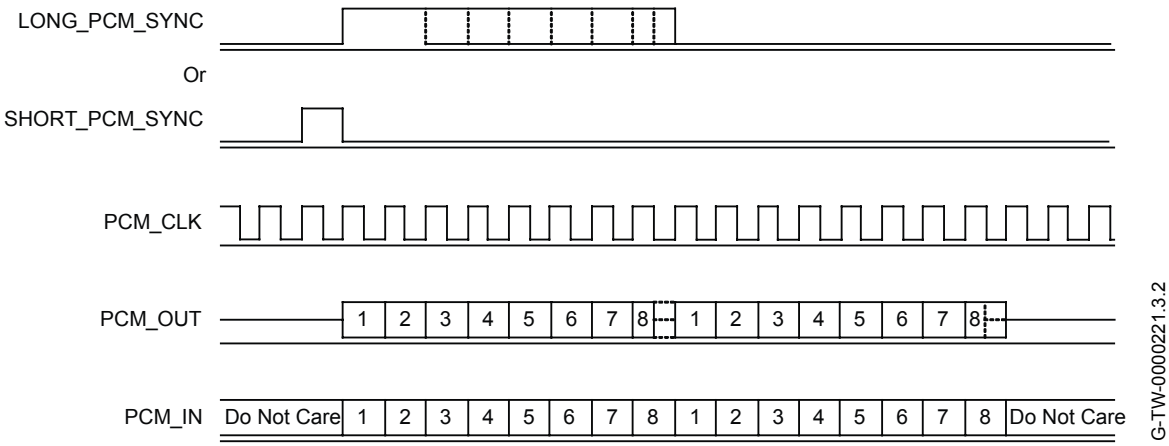


Figure 9.13: Multi-slot Operation with 2 Slots and 8-bit Companded Samples

9.3.5 GCI Interface

CSR8615 QFN is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels are accessed when this mode is configured.

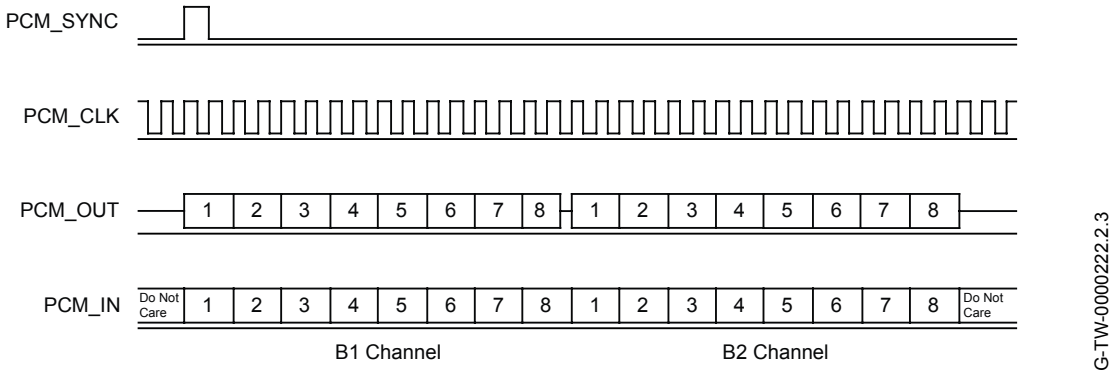


Figure 9.14: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

9.3.6 Slots and Sample Formats

CSR8615 QFN receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

CSR8615 QFN supports:

- 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats.
- A sample rate of 8ksps.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

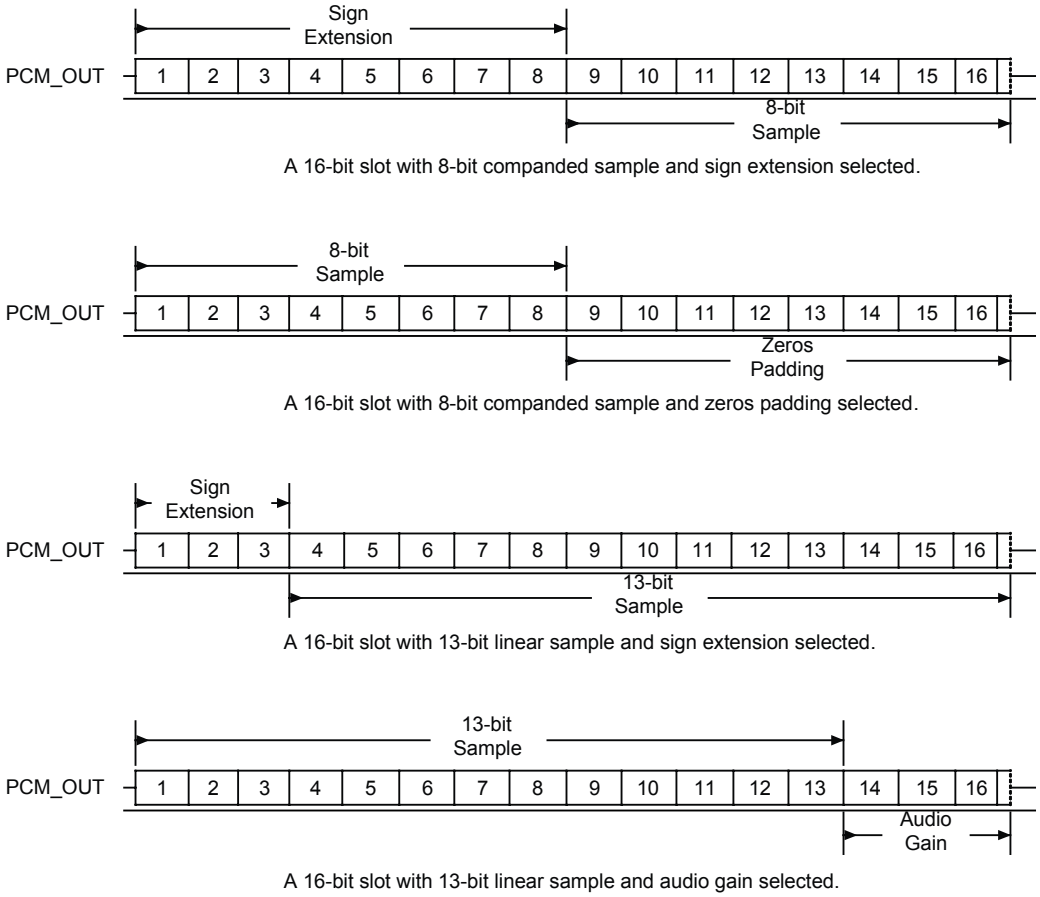


Figure 9.15: 16-bit Slot Length and Sample Formats

9.3.7 Additional Features

CSR8615 QFN has a mute facility that forces PCM_OUT to be 0. In master mode, CSR8615 QFN is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

9.3.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		20	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		0	-	-	ns

Table 9.6: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

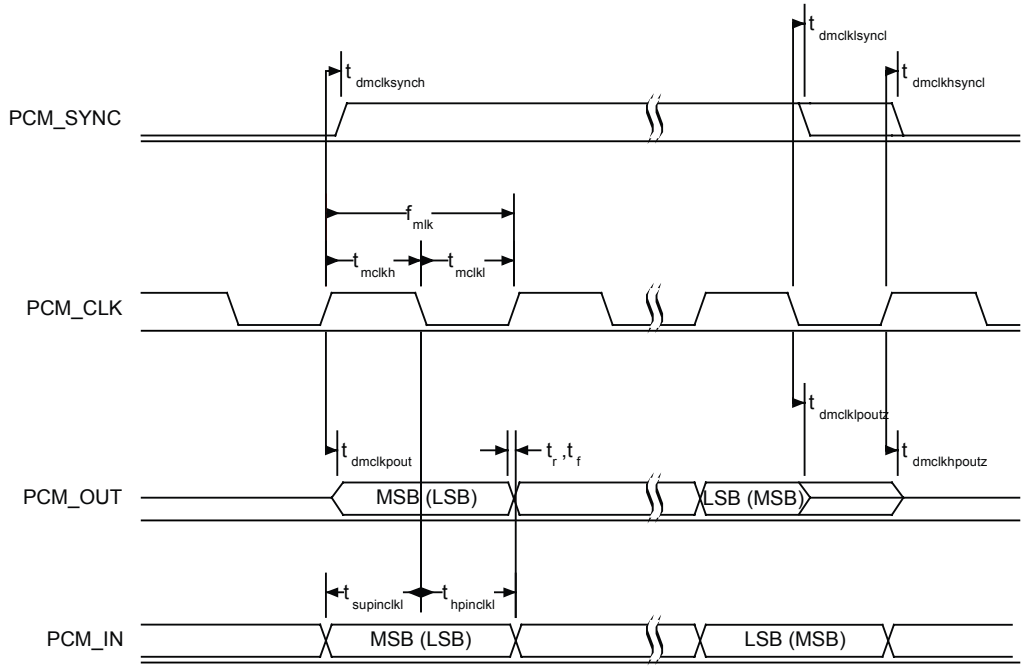


Figure 9.16: PCM Master Timing Long Frame Sync

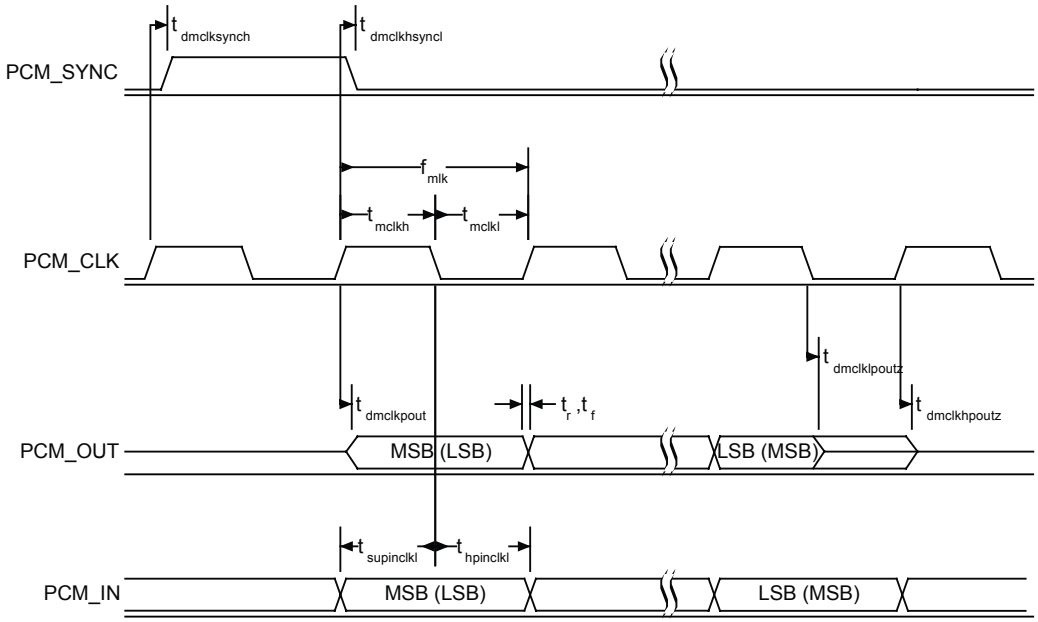


Figure 9.17: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	(a)	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	(b)	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	2	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	15	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	15	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	2	-	-	ns

Table 9.7: PCM Slave Timing

(a) Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

(b) Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

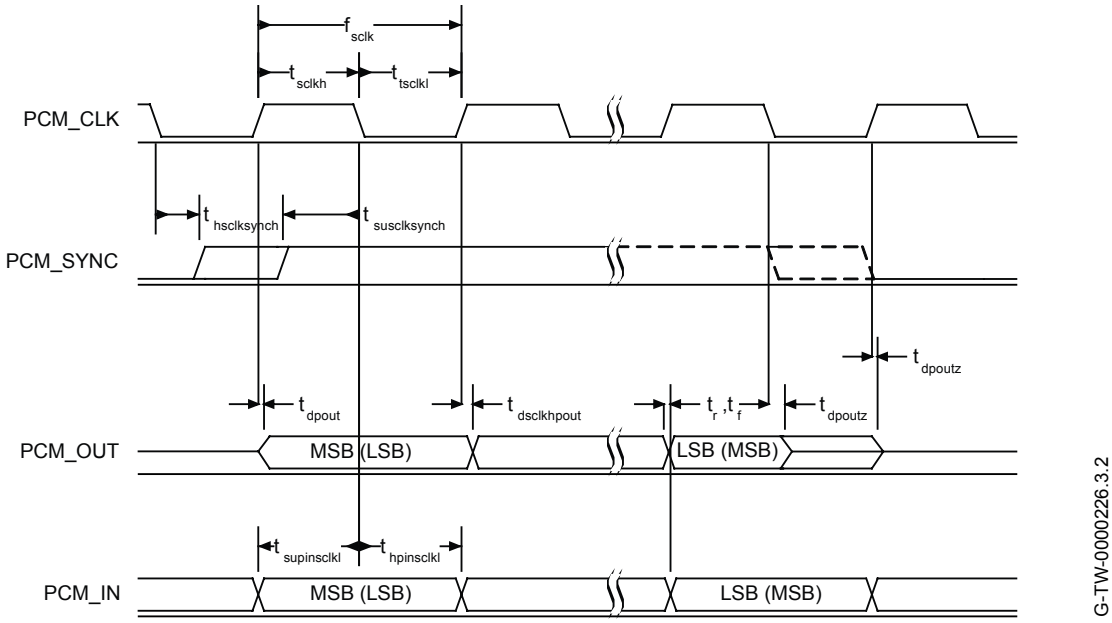


Figure 9.18: PCM Slave Timing Long Frame Sync

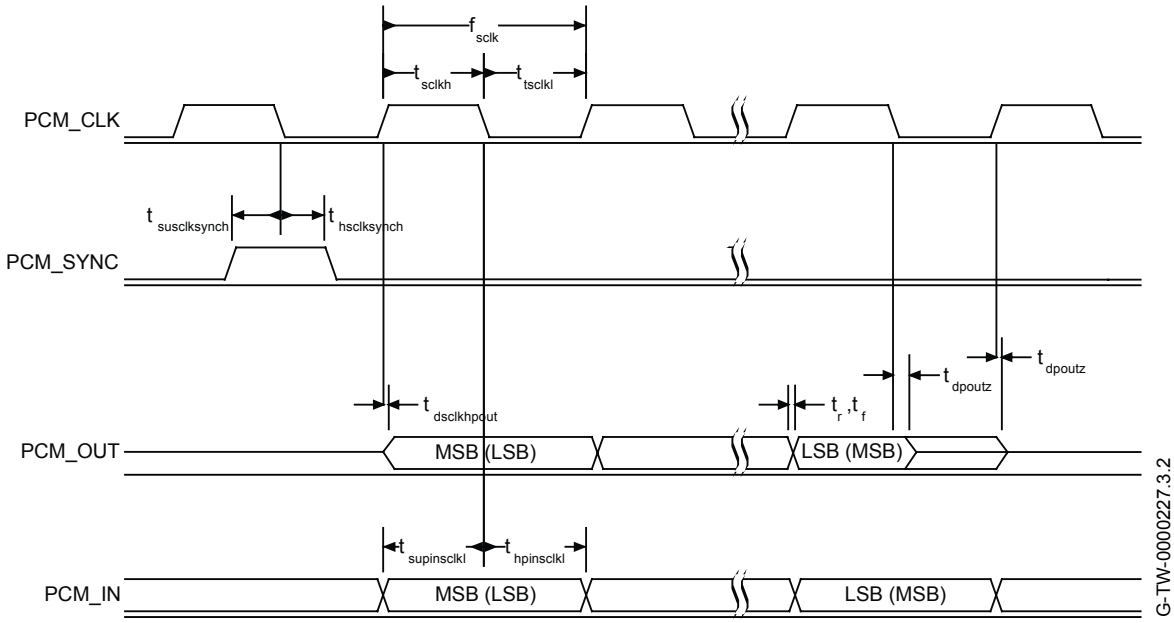


Figure 9.19: PCM Slave Timing Short Frame Sync

9.3.9 PCM_CLK and PCM_SYNC Generation

CSR8615 QFN has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from CSR8615 QFN internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock, which enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

PSKEY_PCM_USE_LOW_JITTER_MODE sets the low jitter mode when the sync rate is 8kHz and the PCM clock is set either by PSKEY_PCM_CLOCK_RATE or through the audio API, see *BlueCore Audio API Specification*.

9.3.10 PCM Configuration

Configure the PCM by using the PS Key PSKEY_PCM_CONFIG32 or through the audio API, see *BlueCore Audio API Specification*. The default for PSKEY_PCM_CONFIG32 is `0x00800000`, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

9.4 Digital Audio Interface (I²S)

Important Note:

The I²S interface is provided as a test interface and is only accessible when running the CSR8615 QFN in HCI-only mode.

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 9.8 lists these alternative functions. Figure 9.20 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 9.8: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see *BlueCore Audio API Specification* and the PS Key file.

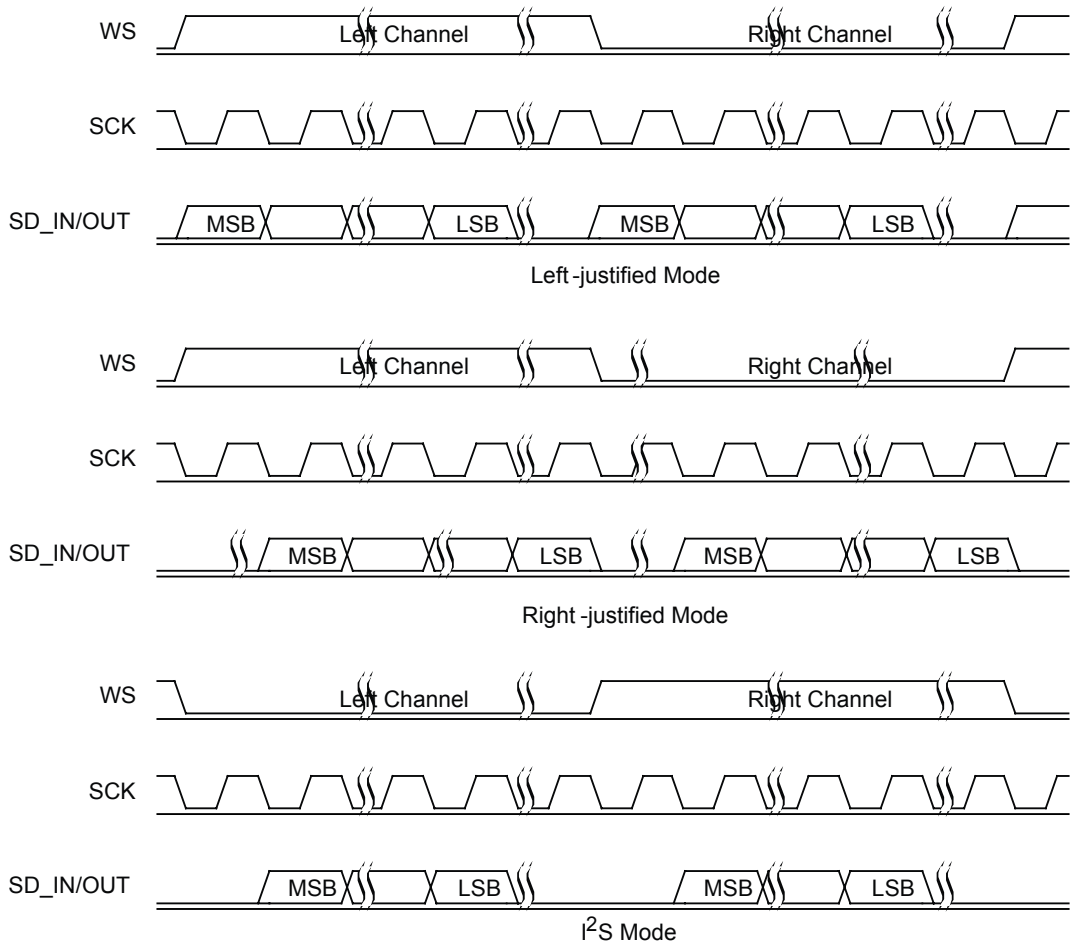


Figure 9.20: Digital Audio Interface Modes

The internal representation of audio samples within CSR8615 QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns

Table 9.9: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	-	-	ns
t_{sh}	SCK high to WS invalid hold time	2.5	-	-	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	-	-	ns

Table 9.10: I²S Slave Mode Timing

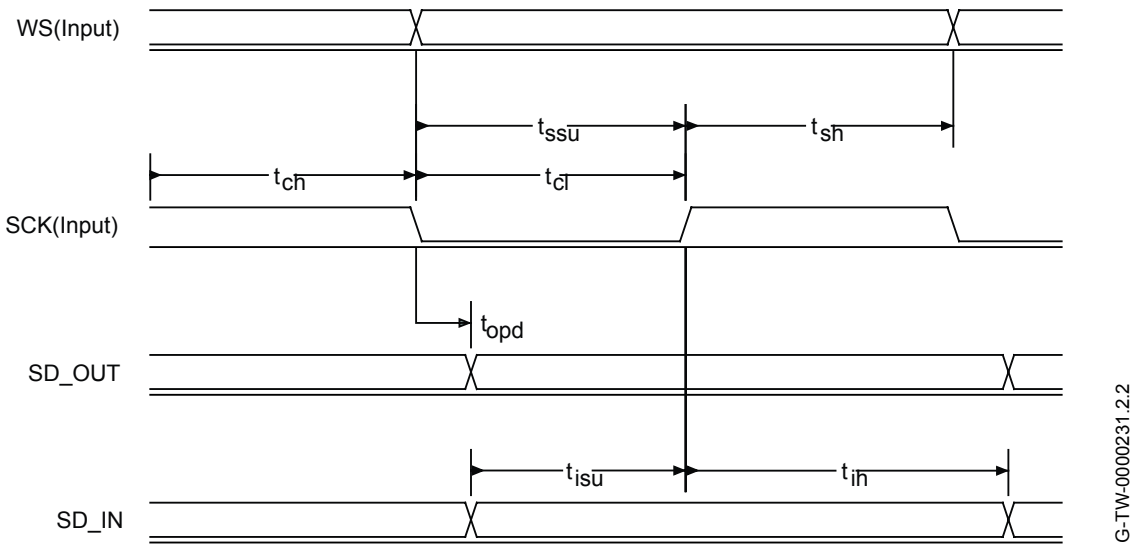


Figure 9.21: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz

Table 9.11: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	-	-	39.27	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	-	-	ns

Table 9.12: I²S Master Mode Timing Parameters, WS and SCK as Outputs

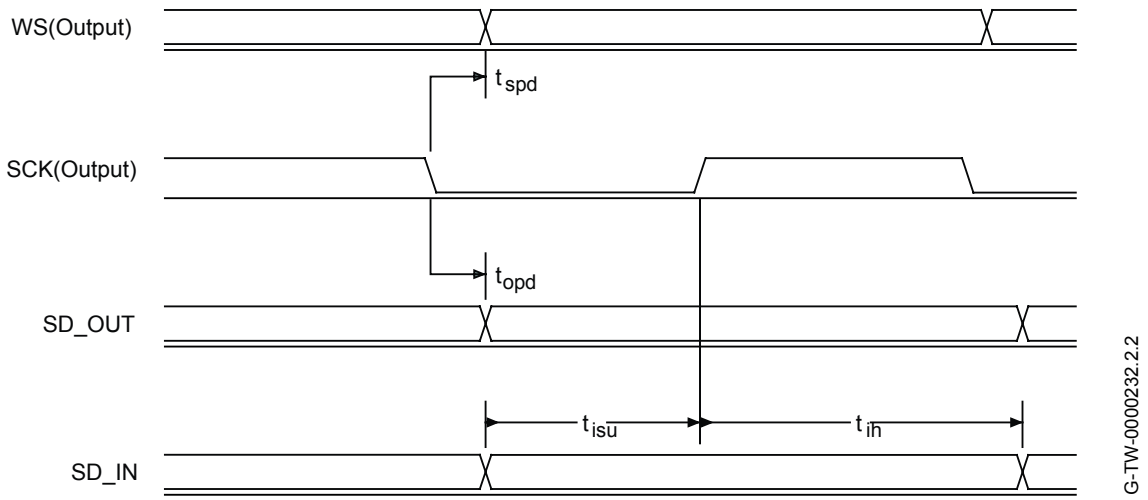


Figure 9.22: Digital Audio Interface Master Timing

10 Power Control and Regulation

For greater power efficiency the CSR8615 QFN contains 2 switch-mode regulators:

- 1 generates a 1.80V supply rail with an output current of 185mA, see Section 10.1.
- 1 generates a 1.35V supply rail with an output current of 160mA, see Section 10.2.
- Combining the 2 switch-mode regulators in parallel generates a single 1.80V supply rail with an output current of 340mA, see Section 10.3.

CSR8615 QFN contains 4 LDO linear regulators:

- 3.30V bypass regulator, see Section 10.4.
- 0.85V to 1.20V VDD_DIG linear regulator, see Section 10.5.
- 1.35V VDD_AUX linear regulator, see Section 10.6.
- 1.35V VDD_ANA linear regulator, see Section 10.7.

The recommended configurations for power control and regulation on the CSR8615 QFN are:

- 3 switch-mode configurations:
  - A 1.80V and 1.35V dual-supply rail system using the 1.80V and 1.35V switch-mode regulators, see Figure 10.1. This is the default power control and regulation configuration for the CSR8615 QFN.
  - A 1.80V single-supply rail system using the 1.80V switch-mode regulator.
  - A 1.80V parallel-supply rail system for higher currents using the 1.80V and 1.35V switch-mode regulators with combined outputs, see Figure 10.2.
- A linear configuration using an external 1.8V rail omitting all regulators

Table 10.1 shows settings for the recommended configurations for power control and regulation on the CSR8615 QFN.

Supply Configuration	Regulators				Supply Rail	
	Switch-mode		VDD_AUX Linear Regulator	VDD_ANA Linear Regulator		
	1.8V	1.35V			1.8V	1.35V
Dual-supply SMPS	ON	ON	OFF	OFF	SMPS	SMPS
Single-supply SMPS	ON	OFF	ON	ON	SMPS	LDO
Parallel-supply SMPS	ON	ON	ON	ON	SMPS	LDO
Linear supply	OFF	OFF	ON	ON	External	LDO

Table 10.1: Recommended Configurations for Power Control and Regulation

For more information on CSR8615 QFN power supply configuration see the *Configuring the Power Supplies on CSR8670* application note.

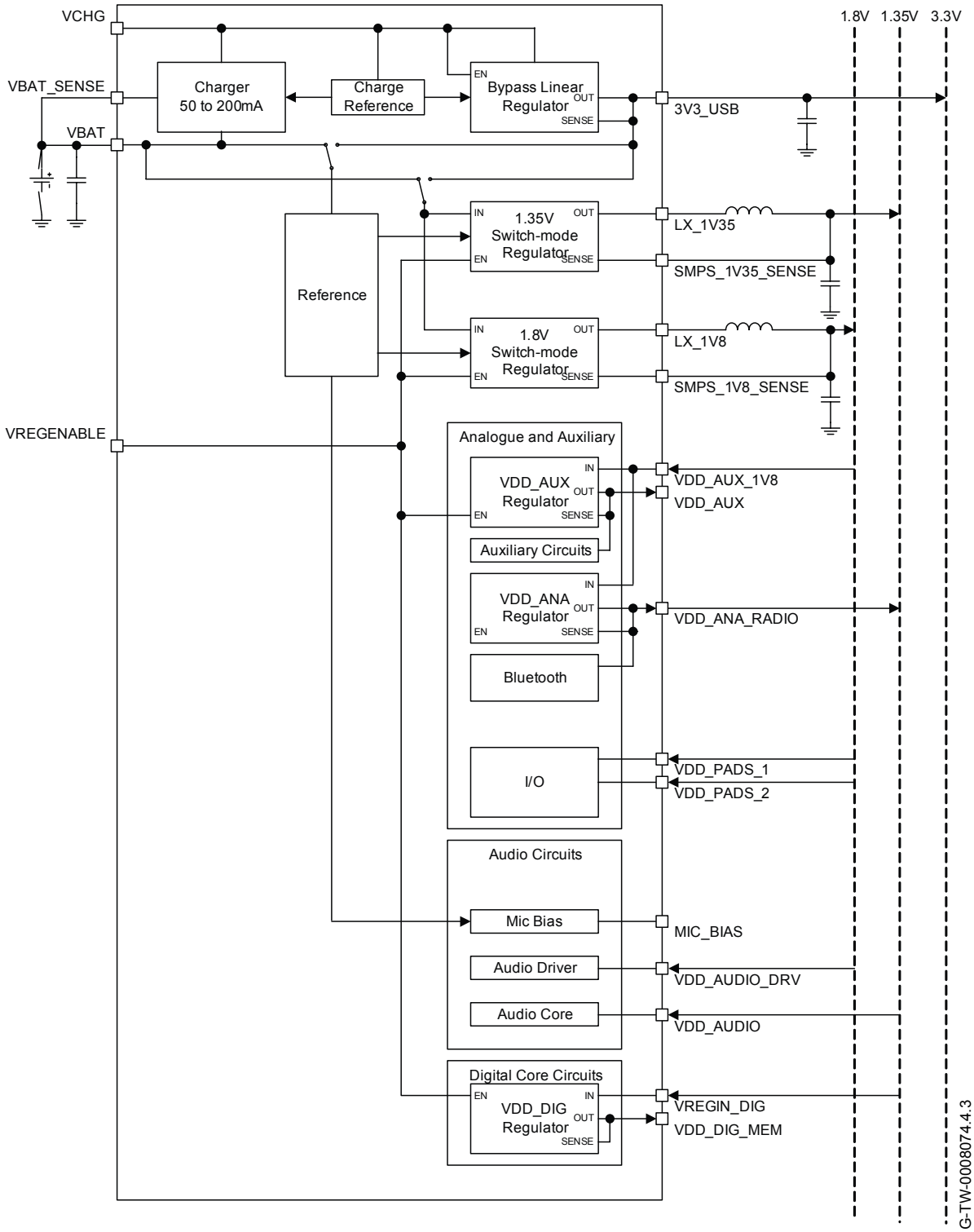


Figure 10.1: 1.80V and 1.35V Dual-supply Switch-mode System Configuration

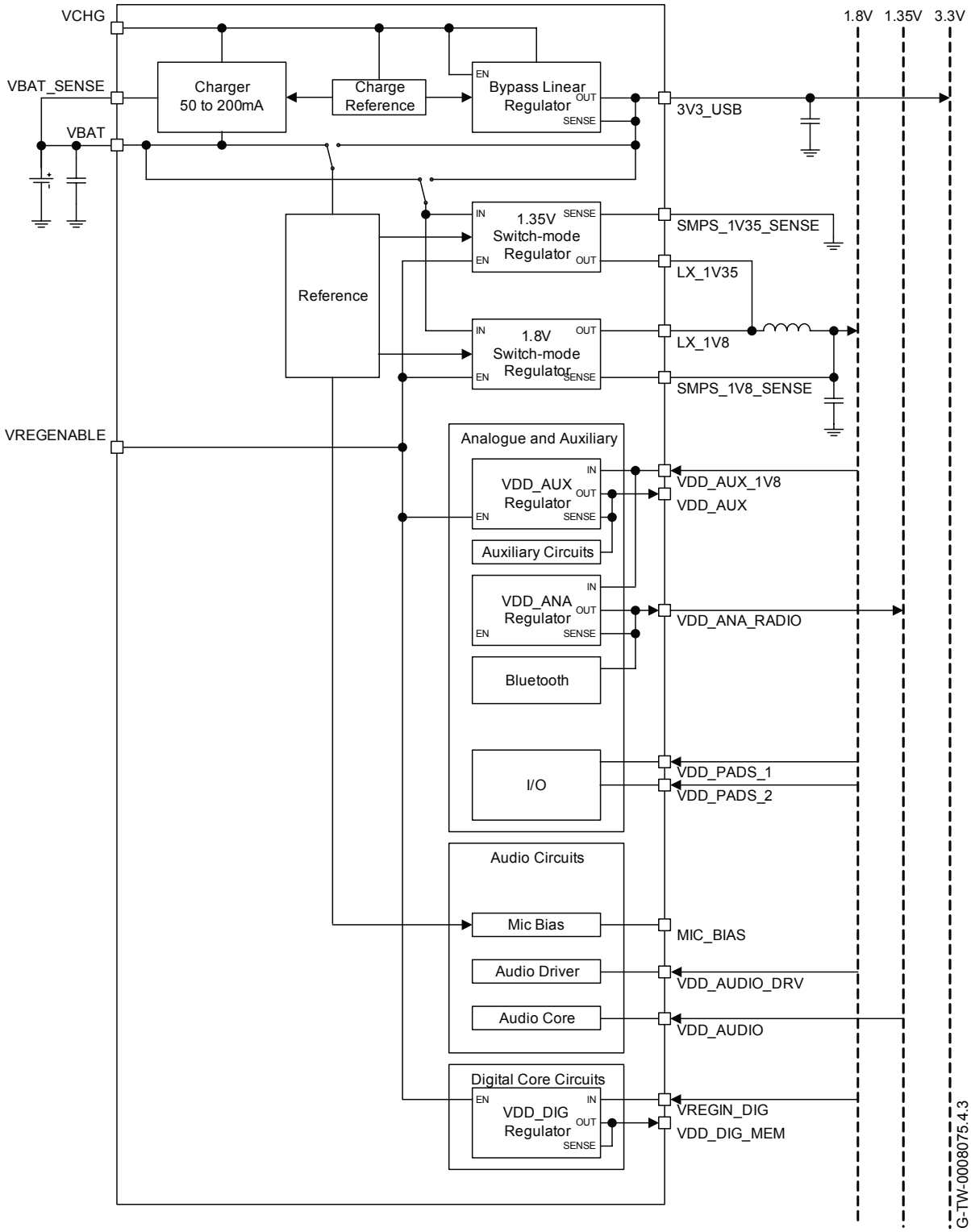


Figure 10.2: 1.80V Parallel-supply Switch-mode System Configuration

10.1 1.8V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.80V supply rail.

Figure 10.3 shows that an external LC filter circuit of a low-resistance series inductor, L1 (4.7µH), followed by a low ESR shunt capacitor, C3 (2.2µF), is required between the LX_1V8 terminal and the 1.80V supply rail. Connect the 1.80V supply rail and the VDD_AUX_1V8 pin.

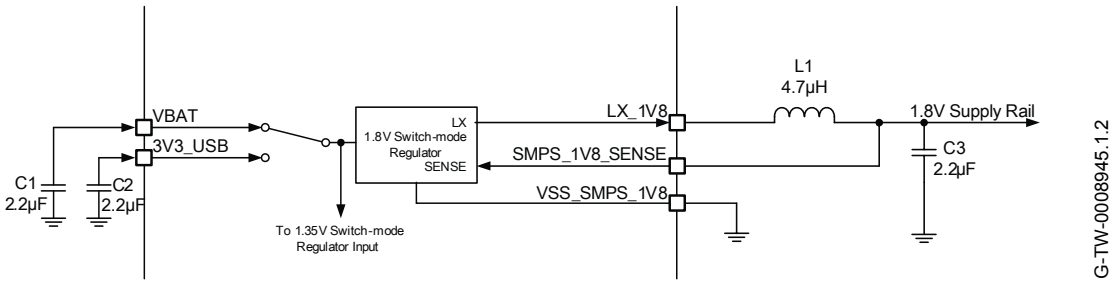


Figure 10.3: 1.8V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, VBAT and 3V3_USB, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V8.

Also minimise the collective parasitic capacitance on the track between LX_1V8 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 13.3.1.1 requires a total resistance of <1.0Ω (<0.5Ω recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80V supply rail.

The following enable the 1.80V switch-mode regulator:

- VREGENABLE pin
- The CSR8615 QFN firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.35V switch-mode regulator.

When the 1.80V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and 3V3_USB
- The regulator output LX_1V8

10.2 1.35V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.35V supply rail.

Figure 10.4 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7µH), followed by a low ESR shunt capacitor, C3 (4.7µF), is required between the LX_1V35 terminal and the 1.35V supply rail. Connect the 1.35V supply rail and the SMPS_1V35_SENSE pin.

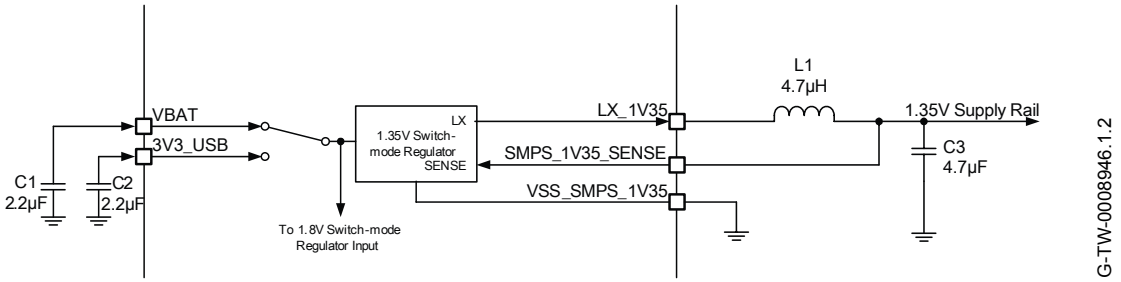


Figure 10.4: 1.35V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, VBAT and 3V3_USB, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 13.3.2.1 requires a total resistance of <1.0Ω (<0.5Ω recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.35V supply rail.

The following enable the 1.35V switch-mode regulator:

- VREGENABLE pin
- The CSR8615 QFN firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.80V switch-mode regulator.

When the 1.35V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and 3V3_USB
- The regulator output LX_1V35

10.3 1.8V and 1.35V Switch-mode Regulators Combined

For applications that require a single 1.80V supply rail with higher currents CSR recommends combining the outputs of the integrated 1.80V and 1.35V switch-mode regulators in parallel to power a single 1.80V supply rail, see Figure 10.5.

Figure 10.5 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7µH), followed by a low ESR shunt capacitor, C3 (2.2µF), is required between the LX_1V8 terminal and the 1.80V supply rail. Connect the 1.80V supply rail and the VDD_AUX_1V8 pin and ground the SMPS_1V35_SENSE pin.

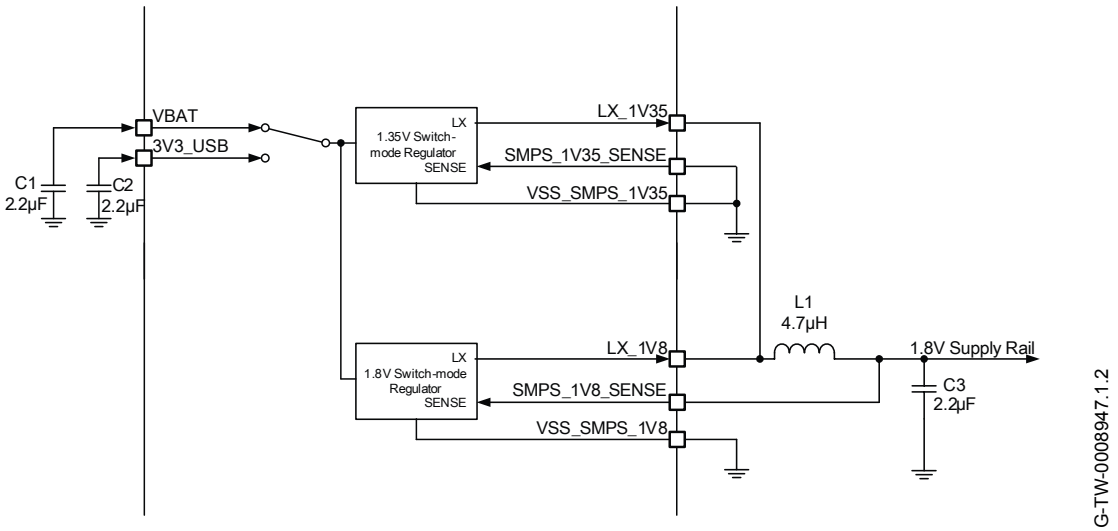


Figure 10.5: 1.8V and 1.35V Switch-mode Regulators Outputs Parallel Configuration

Minimise the series resistance of the tracks between the regulator input VBAT and 3V3_USB, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3, VSS_SMPS_1V8 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V8, LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 13.3.1.2 requires a total resistance of <1.0Ω (<0.5Ω recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8, LX_1V35 and the inductor.
- The inductor L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80V supply rail.

The following enable the 1.80V switch-mode regulator:

- VREGENABLE pin
- The CSR8615 QFN firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET.

When the 1.80V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and 3V3_USB
- The regulator output LX_1V8

10.4 Bypass LDO Linear Regulator

The integrated bypass LDO linear regulator is available as a 3.30V supply rail and is an alternative supply rail to the battery supply. This is especially useful when the battery has no charge and the CSR8615 QFN needs to power up. The input voltage should be between 4.25V to 6.50V.

Note:

The integrated bypass LDO linear regulator can operate down to 3.1V with a reduced performance.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 2.2µF to the 3V3_USB pin.

The output voltage is switched on when VCHG gets above 3.0V.

10.5 Low-voltage VDD_DIG Linear Regulator

The integrated low-voltage VDD_DIG linear regulator powers the digital circuits on CSR8615 QFN. Externally decouple the output of this regulator using a low ESR MLC capacitor of 470nF.

10.6 Low-voltage VDD_AUX Linear Regulator

The integrated low-voltage VDD_AUX linear regulator is optionally available to provide a 1.35V auxiliary supply rail when the 1.35V switch-mode regulator is not used. When using the integrated low-voltage VDD_AUX linear regulator, externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 470nF to the VDD_AUX pin.

10.7 Low-voltage VDD_ANA Linear Regulator

The integrated low-voltage VDD_ANA linear regulator is optionally available to power the 1.35V analogue supply rail when the 1.35V switch-mode regulator is not used. When using the integrated low-voltage VDD_ANA linear regulator, externally decouple the output of this regulator using a 2.2µF low ESR MLC capacitor to the VDD_ANA pin.

10.8 Voltage Regulator Enable

When using the integrated regulators the voltage regulator enable pin, VREGENABLE, enables the CSR8615 QFN and the following regulators:

- 1.8V switch-mode regulator
- 1.35V switch-mode regulator
- Low-voltage VDD_DIG linear regulator
- Low-voltage VDD_AUX linear regulator

The VREGENABLE pin is active high, with a pull-down, typical 100kΩ, which is disabled by PSKEY_VREG_ENABLE_STRONG_PULL.

CSR8615 QFN boots-up when the voltage regulator enable pin is pulled high typically for 10 to 15ms, enabling the regulators. The firmware then latches the regulators on. The voltage regulator enable pin can then be released.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

Note:

VREGENABLE should be asserted after the VBAT supply when VREGENABLE is not used as a power-on button.

10.9 External Regulators and Power Sequencing

CSR recommends that the integrated regulators supply the CSR8615 QFN and it is configured based on the information in this data sheet.

If any of the supply rails for the CSR8615 QFN are supplied from an external regulator, then it should match or be better than the internal regulator available on CSR8615 QFN. For more information see regulator characteristics in Section 13.

Note:

The internal regulators described in Section 10.1 to Section 10.7 are not recommended for external circuitry other than that shown in Section 12.

For information about power sequencing of external regulators to supply the CSR8615 QFN contact CSR.

10.10 Reset, RST#

CSR8615 QFN is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. CSR recommends applying RST# for a period >5ms.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

10.10.1 Digital Pin States on Reset

Table 10.2 shows the pin states of CSR8615 QFN on reset.

Pin Name	I/O Type	Full Chip Reset	Pin Name	I/O Type	Full Chip Reset
USB_DP	Digital bidirectional	N/A	PIO[10]	Digital bidirectional	PDS
USB_DN	Digital bidirectional	N/A	PIO[11]	Digital bidirectional	PDS
PIO[0]	Digital bidirectional	PUS	PIO[12]	Digital bidirectional	PUS
PIO[1]	Digital bidirectional	PUS	PIO[13]	Digital bidirectional	PDS
PIO[2]	Digital bidirectional	PDW	PIO[14]	Digital bidirectional	PUS
PIO[3]	Digital bidirectional	PDW	PIO[15]	Digital bidirectional	PUS
PIO[4]	Digital bidirectional	PDW	PIO[16]	Digital bidirectional	PUS
PIO[5]	Digital bidirectional	PDW	PIO[17]	Digital bidirectional	PDS
PIO[6]	Digital bidirectional	PDS	PIO[18]	Digital bidirectional	PDW
PIO[7]	Digital bidirectional	PDS	PIO[19]	Digital bidirectional	PDW
PIO[8]	Digital bidirectional	PUS	PIO[20]	Digital bidirectional	PDW
PIO[9]	Digital bidirectional	PDS	PIO[21]	Digital bidirectional	PDW

Table 10.2: Pin States on Reset

Note:

PUS = Strong pull-up

PDS = Strong pull-down

PUW = Weak pull-up

PDW = Weak pull-down

10.10.2 Status After Reset

The status of CSR8615 QFN after a reset is:

- Warm reset: baud rate and RAM data remain available
- Cold reset: baud rate and RAM data not available

10.11 Automatic Reset Protection

CSR8615 QFN includes an automatic reset protection circuit which restarts/resets CSR8615 QFN when an unexpected reset occurs, e.g. ESD strike or lowering of RST#. The automatic reset protection circuit enables resets from the VM without the requirement for external circuitry.

Note:

The reset protection is cleared after typically 2s (1.6s min to 2.4s max).

If RST# is held low for >2.4s CSR8615 QFN turns off. A rising edge on VREGENABLE or VCHG is required to power on CSR8615 QFN.

11 Battery Charger

11.1 Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the VM, see Section 11.3.The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see Table 11.1 and Figure 11.1.

The internal charger circuit can provide up to 200mA of charge current, for currents higher than this the CSR8615 QFN can control an external pass transistor, see Section 11.5.

Mode	Battery Charger Enabled	VBAT_SENSE
Disabled	No	X
Trickle charge	Yes	>0 and <V_{fast}
Fast charge	Yes	>V_{fast} and <V_{float}
Standby	Yes	I_{term} [(a)] and >(V_{float} - V_{hyst})
Error	Yes	>(VCHG - 50mV)

Table 11.1: Battery Charger Operating Modes Determined by Battery Voltage and Current

[(a)] I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting

Figure 11.1 shows the mode-to-mode transition voltages. These voltages are fixed and calibrated by CSR, see Section 11.2. The transition between modes can occur at any time.

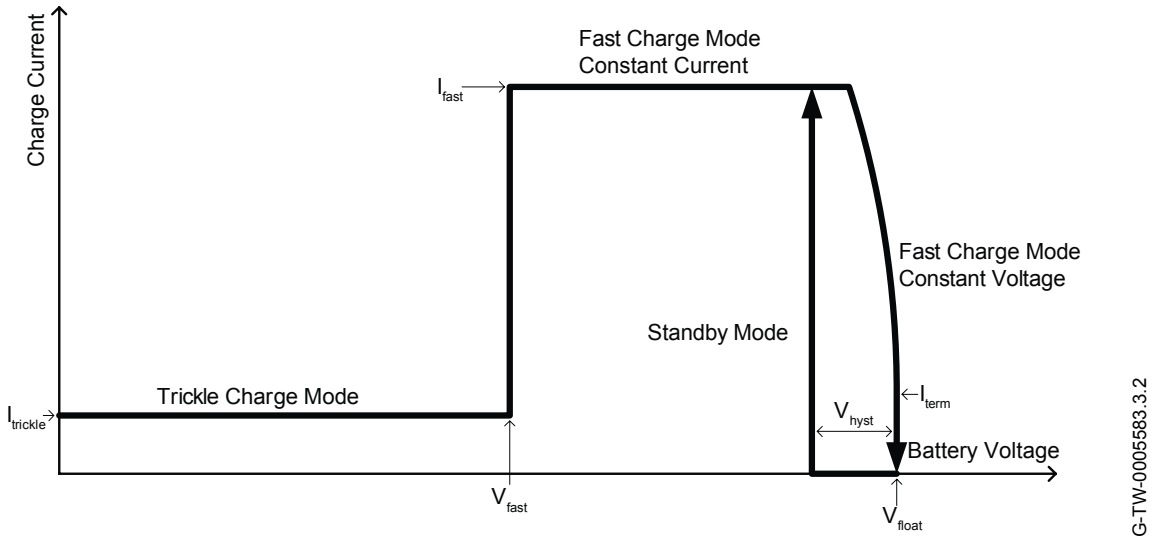


Figure 11.1: Battery Charger Mode-to-Mode Transition Diagram

Note:

The battery voltage remains constant in Fast Charge Constant Voltage Mode, the curved line on Figure 11.1 is for clarity only.

11.1.1 Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

11.1.2 Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast}, is sourced from the VBAT pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

11.1.3 Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast}, the current sourced from the VBAT pin increases to I_{fast}. I_{fast} is between 10mA and 200mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float}, then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term}, the charging stops and the charger enters standby mode. I_{term} is typically 10% of the fast charge current.

11.1.4 Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float}, the charger re-enters fast charge mode.

11.1.5 Error Mode

The charger enters the error mode if the voltage on the VCHG pin is too low to operate the charger correctly (VBAT_SENSE is greater than VCHG - 50mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

11.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written by CSR into non-volatile memory when each IC is characterised. CSR provides various PS Keys for overriding the default trims, see Section 11.4.

11.3 VM Battery Charger Control

The VM charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information
- Driving the user visible charger status LED(s)

11.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and traps called from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

For more information on the CSR8615 QFN, including details on setting up, calibrating, trimming and the PS Keys, see *Lithium Polymer Battery Charger Calibration and Operation for CSR8670* application note.

11.5 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, R_{sense}, connected in series with the external pass device, see Figure 11.2. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across R_{sense} is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

In Figure 11.2, R1 (220mΩ) and C1 (4.7µF) form an RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be <1.0Ω.

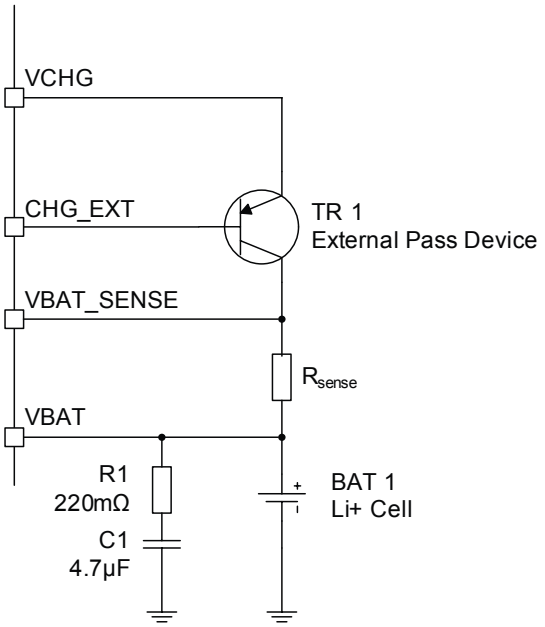


Figure 11.2: Battery Charger External Mode Typical Configuration

12 Example Application Schematic

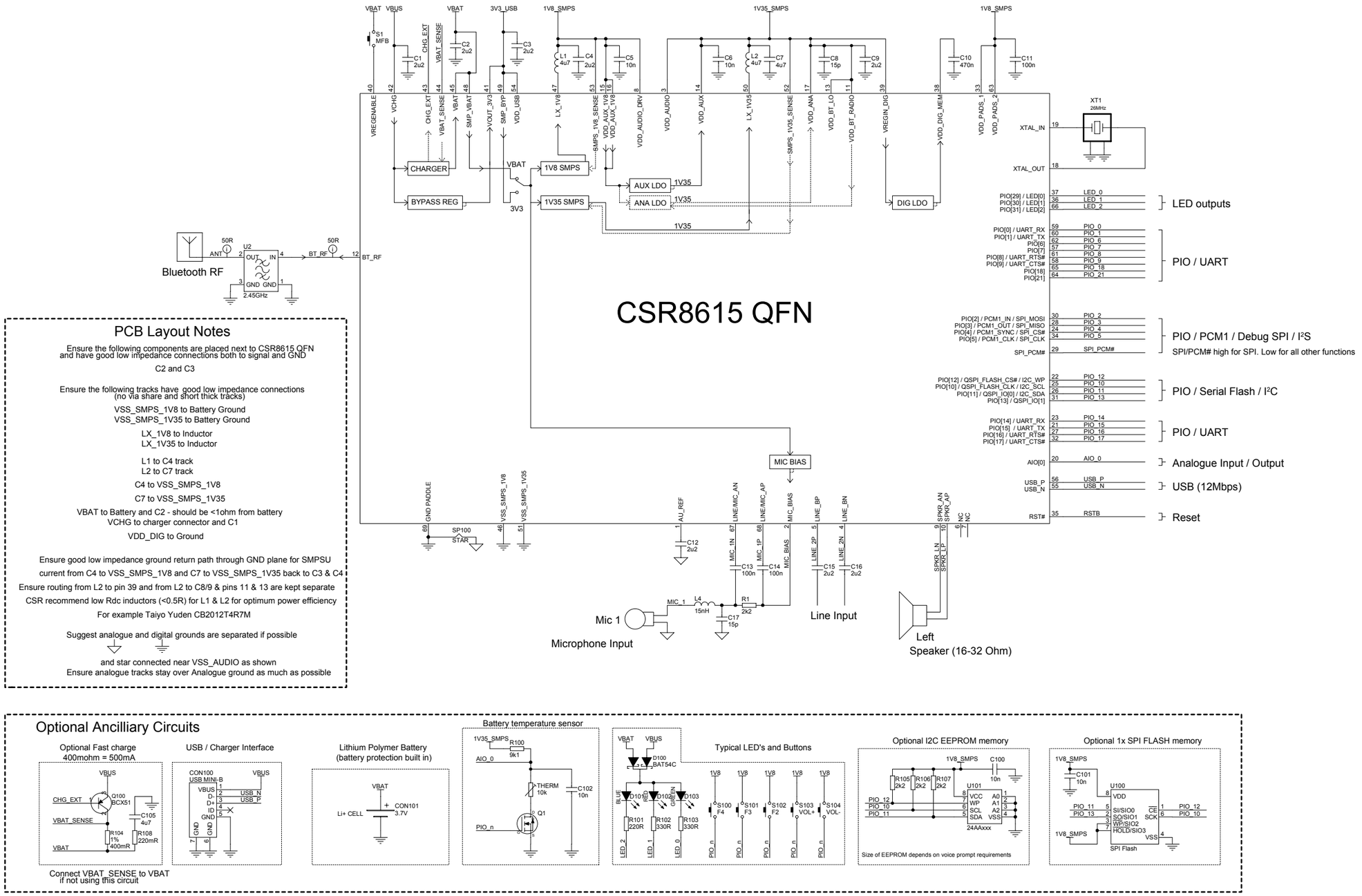


Figure 12.1: Single Microphone and Single Line Input

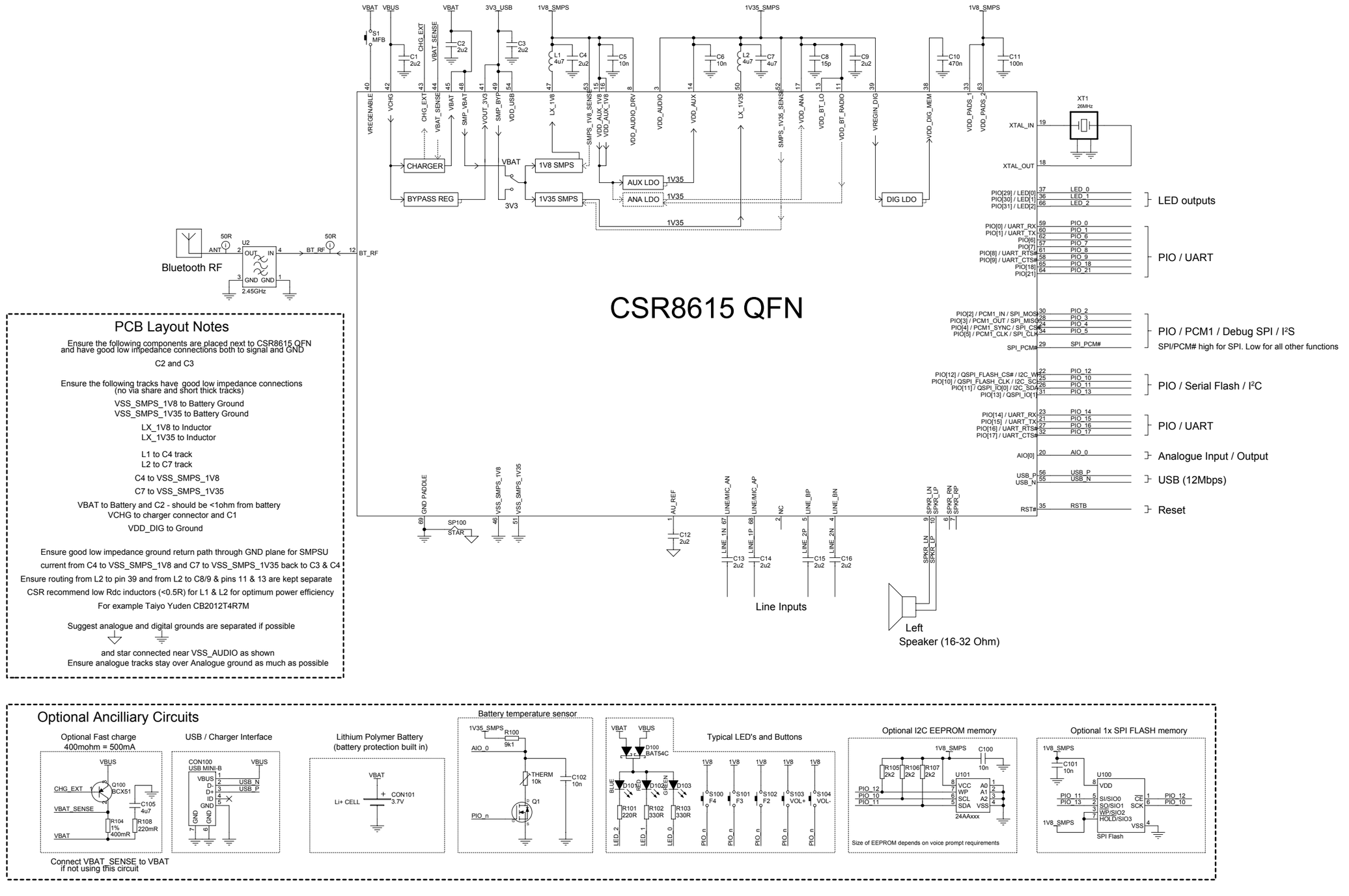


Figure 12.2: Stereo Line Input

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	°C
Supply Voltage				
Charger	VCHG	-0.4	5.75 / 6.50[a]	V
LEDs	LED[2:0]	-0.4	4.40	V
Battery	VBAT_SENSE	-0.4	4.40	V
	VREGENABLE	-0.4	4.40	V
1.8V	VDD_AUDIO_DRV	-0.4	1.95	V
	VDD_AUX_1V8	-0.4	1.95	V
	VDD_PADS_1	-0.4	3.60	V
	VDD_PADS_2	-0.4	3.60	V
1.35V	SMPS_1V35_SENSE	-0.4	1.45	V
	VDD_AUDIO	-0.4	1.45	V
	VREGIN_DIG	-0.4	1.95	V
Other terminal voltages		VSS - 0.4	VDD + 0.4	V

[a] Standard maximum input voltage is 5.75V, a 6.50V maximum requires a correct patch bundle, for more information contact CSR

13.2 Recommended Operating Conditions

Rating		Min	Typ	Max	Unit
Operating temperature range		-40	20	85	°C
Supply Voltage					
Charger	VCHG	4.75 / 3.10[a]	5.00	5.75 / 6.50[b]	V
LEDs	LED[2:0]	1.10	3.70	4.30	V
Battery	VBAT_SENSE	0	3.70	4.25	V
	VREGENABLE	0	3.70	4.25	V
1.8V	VDD_AUDIO_DRV	1.70	1.80	1.95	V
	VDD_AUX_1V8	1.70	1.80	1.95	V
	VDD_PADS_1	1.70	1.80	3.60	V
	VDD_PADS_2	1.70	1.80	3.60	V
1.35V	SMPS_1V35_SENSE	1.30	1.35	1.45	V
	VDD_AUDIO	1.30	1.35	1.45	V
	VREGIN_DIG	1.30	1.35 or 1.80[c]	1.95	V

[a] Minimum input voltage of 4.75 V is required for full specification, regulator operates at reduced load current from 3.1 V

[b] Standard maximum input voltage is 5.75 V, a 6.50 V maximum requires a correct patch bundle, for more information contact CSR

[c] Typical value depends on output required by the low-voltage VDD_DIG linear regulator, see Section 13.3.2.2

13.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

13.3.1 Regulators: Available For External Use

13.3.1.1 1.8V Switch-mode Regulator

1.8V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.70	4.25	V
Output voltage	1.70	1.80	1.90	V
Normal Operation				
Transient settling time	-	30	-	µs
Load current	-	-	185	mA
Current available for external use, audio with 16Ω load[a]	-	-	25	mA
Peak conversion efficiency[b]	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current, audio and 16Ω load	250	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	µs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

[a] More current available for audio loads above 16Ω.

[b] Conversion efficiency depends on inductor selection.

13.3.1.2 Combined 1.8V and 1.35V Switch-mode Regulator

Combined 1.8V and 1.35V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.60	4.25	V
Output voltage	1.70	1.80	1.90	V
Normal Operation				
Transient settling time	-	30	-	µs
Load current	-	-	340	mA
Current available for external use, audio with 16Ω load[a]	-	-	25	mA
Peak conversion efficiency[b]	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current, audio and 16Ω load	400	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	µs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

[a] More current available for audio loads above 16Ω.

[b] Conversion efficiency depends on inductor selection.

13.3.1.3 Bypass LDO Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	4.25 / 3.10[a]	5.00	5.75 / 6.50[b]	V
Output voltage (V_{in} > 4.75V)	3.00	3.30	3.60	V
Output current (V_{in} > 4.75V)	-	-	250	mA

[a] Minimum input voltage of 4.25V is required for full specification, regulator operates at reduced load current from 3.1V

[b] Standard maximum input voltage is 5.75V, a 6.50V maximum requires a correct patch bundle, for more information contact CSR

13.3.2 Regulators: For Internal Use Only

13.3.2.1 1.35V Switch-mode Regulator

1.35V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.60	4.25	V
Output voltage	1.30	1.35	1.40	V
Normal Operation				
Transient settling time	-	30	-	µs
Load current	-	-	160	mA
Current available for external use	-	-	0	mA
Peak conversion efficiency[a]	-	88	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current, audio and 16Ω load	220	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	µs
Load current	0.005	-	5	mA
Current available for external use	-	-	0	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

[a] Conversion efficiency depends on inductor selection.

13.3.2.2 Low-voltage VDD_DIG Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.30	1.35 or 1.80	1.95	V
Output voltage[a]	0.80	0.90 / 1.20	1.25	V
Internal load current	-	-	80	mA

[a] Output voltage level is software controlled

13.3.2.3 Low-voltage VDD_AUX Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage	1.30	1.35	1.45	V
Internal load current	-	-	5	mA

13.3.2.4 Low-voltage VDD_ANA Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage	1.30	1.35	1.45	V
Load current	-	-	60	mA

13.3.3 Regulator Enable

VREGENABLE, Switching Threshold	Min	Typ	Max	Unit
Rising threshold	1.0	-	-	V

13.3.4 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage, VCHG	4.75 / 3.10[a]	5.00	5.75 / 6.50[b]	V

[a] Reduced specification from 3.1V to 4.75V. Full specification >4.75V.

[b] Standard maximum input voltage is 5.75V, a 6.50V maximum requires a correct patch bundle, for more information contact CSR.

Trickle Charge Mode	Min	Typ	Max	Unit
Charge current $I_{trickle}$, as percentage of fast charge current	8	10	12	%
V_{fast} rising threshold	-	2.9	-	V
V_{fast} rising threshold trim step size	-	0.1	-	V
V_{fast} falling threshold	-	2.8	-	V

Fast Charge Mode		Min	Typ	Max	Unit
Charge current during constant current mode, I_{fast}	Maximum charge setting (VCHG-VBAT > 0.55V)	194	200	206	mA
	Minimum charge setting (VCHG-VBAT > 0.55V)	-	10	-	mA
Reduced headroom charge current, as a percentage of I_{fast}	(VCHG-VBAT < 0.55V)	50	-	100	%
Charge current step size		-	10	-	mA
V_{float} threshold, calibrated		4.16	4.20	4.24	V
Charge termination current I_{term}, as percentage of I_{fast}		7	10	20	%

Standby Mode	Min	Typ	Max	Unit
Voltage hysteresis on VBAT, V_{hyst}	100	-	150	mV

Error Charge Mode	Min	Typ	Max	Unit
Headroom[(a)] error falling threshold	-	50	-	mV

[(a)] Headroom = VCHG - VBAT

External Charge Mode[a]	Min	Typ	Max	Unit
Fast charge current, I_{fast}	200	-	500	mA
Control current into CHG_EXT	0	-	20	mA
Voltage on CHG_EXT	0	-	5.75 / 6.50[b]	V
External pass device h_{fe}	-	50	-	-
Sense voltage, between VBAT_SENSE and VBAT at maximum current	195	200	205	mV

[a] In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

[b] Standard maximum input voltage is 5.75V, a 6.50V maximum requires a correct patch bundle, for more information contact CSR.

13.3.5 USB

	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1	3.3	3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3 x VDD_USB	V
V_{IH} input logic level high	0.7 x VDD_USB	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

13.3.6 Stereo Line-in Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	48	kHz
Maximum ADC Input Signal Amplitude	0dB = 1600mV$_{pk-pk}$		13	-	2260	mV$_{pk-pk}$
SNR	f_{in} = 1kHz B/W = 20Hz→F_{sample}/2 (20kHz max) A-Weighted THD+N < 0.1% 1.6V$_{pk-pk}$ input	**F_{sample}**				
		8kHz	-	95.3	-	dB
		16kHz	-	93.8	-	dB
		32kHz	-	94.2	-	dB
		44.1kHz	-	92.4	-	dB
		48kHz	-	91.8	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz→F_{sample}/2 (20kHz max) 1.6V$_{pk-pk}$ input	**F_{sample}**				
		8kHz	-	0.0085	-	%
		48kHz	-	0.0129	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analogue setting = -3dB to 12dB in 3dB steps		-3	-	42	dB
Stereo separation (crosstalk)			-	-88.5	-	dB

13.3.7 Codec: Digital to Analogue Converter

Digital to Analogue Converter							
Parameter	**Conditions**			**Min**	**Typ**	**Max**	**Unit**
Resolution	-			-	-	16	Bits
Output Sample Rate, F_{sample}	-			8	-	96	kHz
SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.1% 0dBFS input	**F_{sample}**	**Load**				
		48kHz	100kΩ	-	95.6	-	dB
		48kHz	32Ω	-	95.5	-	dB
		48kHz	16Ω	-	94.6	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz→20kHz 0dBFS input	**F_{sample}**	**Load**				
		8kHz	100kΩ	-	0.0029	-	%
		8kHz	32Ω	-	0.0024	-	%
		8kHz	16Ω	-	0.0039	-	%
		48kHz	100kΩ	-	0.0034	-	%
		48kHz	32Ω	-	0.0031	-	%
		48kHz	16Ω	-	0.0032	-	%
Digital Gain	Digital Gain Resolution = 1/32			-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB			-21	-	0	dB
Output voltage	Full-scale swing (differential)			-	-	778	mV rms

13.3.8 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7 x VDD	-	VDD + 0.4	V
Tr/Tf	-	-	25	ns
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 X VDD	-	-	V
Tr/Tf	-	-	5	ns
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
C_I Input Capacitance	1.0	-	5.0	pF

13.3.9 LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Current, I_{PAD}	High impedance state	-	-	5	µA
	Current sink state	-	-	10	mA
LED pad voltage, V_{PAD}	I_{PAD} = 10mA	-	-	0.55	V
LED pad resistance	V_{PAD} < 0.5V	-	-	40	Ω
V_{OL} output logic level low[a]		-	0	-	V
V_{OH} output logic level high[a]		-	0.8	-	V
V_{IL} input logic level low		-	0	-	V
V_{IH} input logic level high		-	0.8	-	V

[a] LED output port is open-drain and requires a pull-up

13.3.10 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range[a]		0	-	VDD_AUX	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		1.38	1.69	2.75	µs
Sample rate[b]		-	-	700	Samples/s

[a] LSB size = VDD_AUX/1023

[b] The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

13.3.11 Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Supply voltage, VDD_AUX	1.30	1.35	1.40	V
Output voltage range	0	-	VDD_AUX	V
Full-scale output voltage	1.30	1.35	1.40	V
LSB size	0	1.32	2.64	mV
Offset	-1.32	0	1.32	mV
Integral non-linearity	-1	0	1	LSB
Settling time[a]	-	-	250	ns

[a] The settling time does not include any capacitive load

Important Note:

Access to the auxiliary DAC is firmware-dependent, for more information about its availability contact CSR.

13.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 13.1 shows the ESD handling maximum ratings.

Condition	Class	Max Rating
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2kV (all pins except CHG_EXT; CHG_EXT is rated at 1kV)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500V (all pins)

Table 13.1: ESD Handling Ratings

13.4.1 USB Electrostatic Discharge Immunity

CSR8615 QFN has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

CSR has tested CSR8615 QFN assembled in development kits to assess the Electrostatic Discharge Immunity. The tests were based on IEC 61000-4-2 requirements. Tests were performed up to level 4 (8kV contact discharge / 15kV air discharge).

CSR can demonstrate normal performance up to level 2 (4kV contact discharge / 4kV air discharge) as per IEC 6100-4-2 classification 1. Above level 2, temporary degradation is seen (classification 2).

CSR8615 QFN contains a reset protection circuit and software, which will attempt to re-make any connections lost in a ESD event. If the device at the far end permits this, self-recovery of the Bluetooth link is possible if CSR8615 QFN resets on an ESD strike. This classes CSR8615 QFN as IEC 61000-4-2 classification 2 to level 4 (8kV contact discharge / 15kV air discharge). If self-recovery is not implemented, CSR8615 QFN is IEC 61000-4-2 classification 3 to level 4.

Note:

Any test detailed in the IEC-61000-4-2 level 4 test specification does not damage CSR8615 QFN.

The CSR8615 QFN USB VBUS pin is protected to level 4 using an external 2.2µF decoupling capacitor on VCHG.

Important Note:

CSR recommends correct PCB routing and to route the VBUS track through a decoupling capacitor pad.

When the USB connector is a long way from CSR8615 QFN, place an extra 1µF or 2.2µF capacitor near the USB connector.

No components (including 22Ω series resistors) are required between CSR8615 QFN and the USB_DP and USB_DN lines.

To recover from an unintended reset, e.g. a large ESD strike, the watchdog and reset protection feature can restart CSR8615 QFN and signal the unintended reset to the VM.

Table 13.2 summarises the level of protection.

IEC 61000-4-2 Level	ESD Test Voltage (Positive and Negative)	IEC 61000-4-2 Classification	Comments
1	2kV contact / 2kV air	Class 1	Normal performance within specification limits
2	4kV contact / 4kV air	Class 1	Normal performance within specification limits
3	6kV contact / 8kV air	Class 2 or class 3	Temporary degradation or operator intervention required
4	8kV contact / 15kV air	Class 2 or class 3	Temporary degradation or operator intervention required

Table 13.2: USB Electrostatic Discharge Protection Level

For more information contact CSR.

14 Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	SCO		-	-	TBD	mA
Slave	eSCO		-	-	TBD	mA
Slave	eSCO		-	-	TBD	mA
Slave	SCO	1-mic CVC: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Slave	eSCO	1-mic CVC: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Slave	eSCO	1-mic CVC: ■ 16kHz sampling ■ Wideband	-	-	TBD	mA
Slave	eSCO	1-mic CVC: ■ 16kHz sampling ■ FESI	-	-	TBD	mA
Slave	SCO	1-mic CVC hands-free: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Slave	eSCO	1-mic CVC hands-free: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Slave	eSCO	1-mic CVC hands-free: ■ 16kHz sampling ■ Wideband	-	-	TBD	mA
Slave	eSCO	1-mic CVC hands-free: ■ 16kHz sampling ■ FESI	-	-	TBD	mA
Slave	A2DP Mono streaming SBC high quality: ■ Bit-Pool = 50, 16 blocks and 8 sub-bands ■ 48kHz sampling ■ No sniff ■ White noise		-	-	TBD	mA

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	A2DP Mono streaming SBC low quality: ■ Bit-Pool = 20, 16 blocks and 8 sub-bands ■ 48kHz sampling ■ No sniff ■ White noise		-	-	TBD	mA
Slave	ACL	Sniff = 500ms	-	-	TBD	µA
Slave	ACL	Sniff = 1280ms	-	-	TBD	µA
Master	SCO		-	-	TBD	mA
Master	eSCO		-	-	TBD	mA
Master	eSCO		-	-	TBD	mA
Master	SCO	1-mic CVC: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Master	eSCO	1-mic CVC: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Master	eSCO	1-mic CVC: ■ 16kHz sampling ■ Wideband	-	-	TBD	mA
Master	eSCO	1-mic CVC: ■ 16kHz sampling ■ FESI	-	-	TBD	mA
Master	SCO	1-mic CVC hands-free: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA
Master	eSCO	1-mic CVC hands-free: ■ 8kHz sampling ■ Narrowband	-	-	TBD	mA

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Master	eSCO	1-mic CVC hands-free: ▪ 16kHz sampling ▪ Wideband	-	-	TBD	mA
Master	eSCO	1-mic CVC hands-free: ▪ 16kHz sampling ▪ FESI	-	-	TBD	mA
Master	A2DP Mono streaming SBC high quality: ▪ Bit-Pool = 50, 16 blocks and 8 sub-bands ▪ 48kHz sampling ▪ No sniff ▪ White noise		-	-	TBD	mA
Master	A2DP Mono streaming SBC low quality: ▪ Bit-Pool = 20, 16 blocks and 8 sub-bands ▪ 48kHz sampling ▪ No sniff ▪ White noise		-	-	TBD	mA
Master	ACL	Sniff = 500ms	-	-	TBD	µA
Master	ACL	Sniff = 1280ms	-	-	TBD	µA

Note:

Current consumption values are taken with:

- VBAT pin = 3.7V
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH classification master disabled

15 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2011/65/EU[1].
- EU REACH, Regulation (EC) No 1907/2006[1]:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)[1].
- POP regulation (EC) No 850/2004[1]
- EU Packaging and Packaging Waste, Directive 94/62/EC[1]
- Montreal Protocol on substances that deplete the ozone layer.
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. CSR is a fabless semiconductor company: all manufacturing is performed by key suppliers. CSR have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. CSR shall provide a complete EICC / GeSI template upon request.

CSR has defined the "CSR Green" standard based on current regulatory and customer requirements including free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions CSR specify. For more information on the full "CSR Green" standard, contact product.compliance@csr.com.

[1] Including applicable amendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

16 Software

CSR8615 QFN:

- Includes integrated Bluetooth v4.0 specification qualified HCI stack firmware
- Includes integrated CSR8615 Mono ROM Solution, with 6th generation CVC audio enhancements and a configurable EQ
- Can be shipped with CSR's CSR8615 mono ROM solution development kit for CSR8615 QFN, order code DK-8615-10161-1A

The CSR8615 QFN software architecture enables Bluetooth processing and the application program to run on the internal RISC MCU, and the audio enhancements on the Kalimba DSP.

16.1 CSR8615 Mono ROM Solution

The CSR8615 mono ROM solution software supports:

- 6th generation CVC audio enhancements
- WNR
- PLC / BEC
- mSBC wideband speech codec
- A2DP v1.2
- HFP v1.6 and HSP v1.2
- SCMS-T
- Bluetooth v4.0 specification is supported in the ROM software
- Secure simple pairing
- Proximity pairing (device-initiated pairing) for greatly simplifying the out-of-box pairing process, for more information see Section 16.1.8
- For connection to more than 1 mobile phone, advanced Multipoint is supported. This enables a user to take calls from a work and personal phone or a work phone and a VoIP dongle for Skype users. This has minimal impact on power consumption and is easy to configure.
- Most of the CSR8615 mono ROM solution ROM software features are configured on the CSR8615 QFN using the Headset Configuration Tool. The tool reads and writes device configurations directly to the EEPROM, serial flash or alternatively to a PSR file. Configurable device features include:
  - Bluetooth v4.0 specification features
  - Reconnection policies, e.g. reconnect on power-on
  - Audio features, including default volumes
  - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for last number redial
  - LED indications for states, e.g. device connected, and events, e.g. power on
  - Indication tones for events and ringtones
  - HFP v1.6 supported features
  - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
  - Advanced Multipoint settings
- Configurable 5-band EQ for music playback (rock, pop, classical, jazz, dance etc)
- AAC, SBC, MP3 and Faststream decoder
- Volume Boost
- USB audio mode for streaming high-quality music from a PC whilst charging, enables the device to:
  - Playback high-quality music, e.g. iTunes
  - Use bidirectional audio in conversation mode, e.g. for Skype

- Wired audio mode for pendant-style devices supports music playback using a line-in jack. Enables non Bluetooth operation in low battery modes or when using the device in an airplane-mode.
- Support for smartphone applications (apps)
- The CSR8615 mono ROM solution has undergone extensive interoperability testing to ensure it works with the majority of phones on the market

16.1.1 A2DP Streaming

CSR8615 QFN enables an A2DP v1.2 stream connection. This enables high-quality mono music streaming where the left and right stereo streams are mixed.

16.1.2 Advanced Multipoint Support

Advanced Multipoint enables the connection of 2 devices to a CSR8615 QFN device at the same time, examples include:

- 2 phones connected to a CSR8615 QFN device
- Phone and a VoIP dongle connected to a CSR8615 QFN device
- Phone and tablet

The CSR8615 mono ROM solution:

- Supports up to 2 simultaneous connections (either HFP or HSP)
- Enables multiple-call handling from both devices at the same time
- Treats all device buttons:
  - During a call from one device, as if there is 1 device connected
  - During multiple calls (1 on each device), as if there is a single AG with multiple calls in progress (three-way calling)
  - During multiple calls (more than 1 on each device), as if there are multiple calls on a single device enabling the user to switch between the active and held calls

16.1.3 A2DP Multipoint Support

A2DP Multipoint support enables the connection of 2 A2DP source devices to CSR8615 QFN at the same time, examples include:

- 2 A2DP-capable phones connected to a CSR8615 QFN device
- A2DP-capable phone and an A2DP-only source device, e.g. a PC or an iPod touch

The CSR8615 mono ROM solution enables:

- Music streaming from either of the connected A2DP source devices where the music player is controlled on the source device
- Advanced HFP Multipoint functions to interrupt music streaming for calls, and resume music streaming on the completion of the calls
- AVRCP v1.4 connections to both connected devices, enabling the device to remotely control the primary device, i.e. the device currently streaming audio

16.1.4 Wired Audio Mode

CSR8615 QFN supports a wired audio mode for playing music over a wired connection. This enables operation when the battery is too low for Bluetooth operation or in environments where the use of wireless technologies is not permitted, e.g. airplane-mode.

The CSR8615 mono ROM solution automatically routes the wired audio input to the output when CSR8615 QFN is not powered.

If CSR8615 QFN is powered, the audio path is routed through CSR8615 QFN, including via the DSP, this enables CSR8615 QFN to:

- Mix audio sources, e.g. tones and programmable audio prompts
- Control the volume of the audio, i.e. volume up and volume down
- Utilise the 5 band EQ

In wired audio mode, if required, the CSR8615 QFN is still available for Bluetooth audio. This enables seamless transition from wired audio mode to Bluetooth audio mode and back again. This transition is configurable to occur automatically as the battery voltage of the device reduces to a point at which Bluetooth audio is no longer possible.

16.1.5 Smartphone Applications (Apps)

CSR8615 QFN includes CSR's proprietary mechanism for communicating with smartphone apps, it enables full UI control of the device from within the application running on a smartphone, e.g. Google Android OS-based handset. For more information on this feature contact CSR.

16.1.6 Programmable Audio Prompts

CSR8615 QFN enables a user to configure and load pre-programmed audio prompts from:

- An external EEPROM, in this implementation the prompts are stored in the same EEPROM as the PS Keys, see Figure 16.2. A larger EEPROM is necessary for programmable audio prompts. This implementation supports EEPROMs up to 512Kb. An EEPROM of 512Kb enables approximately 15 seconds of audio storage.
- An external SPI flash, in this implementation the prompts are stored in the same SPI flash as the PS Keys, see Figure 16.1.

The programmable audio prompts provide a mechanism for higher-quality audio indications to replace standard tone indications. A programmable audio prompt is assigned to any user event in place of a standard tone.

Programmable audio prompts contain either voice prompts to indicate that events have occurred or provide user-defined higher quality ring tones/indications, e.g. custom power on/off tones.

The Headset Configuration Tool can generate the content for the programmable audio prompts from standard WAV audio files. The tool also enables the user to configure which prompts are assigned to which user events.

Section 6.5 describes the SPI flash interface and Section 7.4 describes the I²C interface to an external EEPROM.

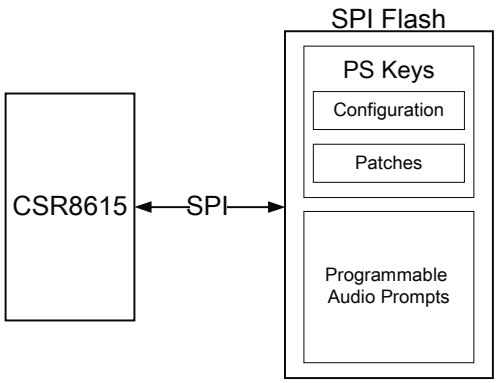


Figure 16.1: Programmable Audio Prompts in External SPI Flash

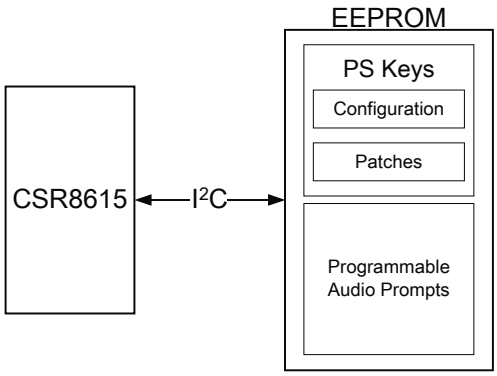


Figure 16.2: Programmable Audio Prompts in External I²C EEPROM

Note:

When using the SPI flash interface for programmable audio prompts, an EEPROM device is not required in the CSR8615 mono ROM solution.

16.1.7 CSR's Intelligent Power Management

IPM extends the available talk time of a CSR8615 QFN-based device, by automatically reducing the audio processing performed by CVC at a series of low battery capacity thresholds.

Configurable IPM features include:

- IPM enable/disable
- The battery capacity that engages IPM
- A user-action to enable or disable the IPM

If engaged, CVC processing reduces automatically on reaching the preset battery capacity. Once the audio is terminated, the DSP shuts down to achieve maximum power savings before the next call.

IPM resets when recharging the device. The talk time extension depends on:

- The battery size
- The battery condition
- The threshold capacity configured for the IPM to engage

16.1.8 Proximity Pairing

Proximity pairing is device-initiated pairing and it simplifies the out-of-box pairing process. Proximity pairing enables the device to find the closest discoverable phone. The device then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus to pair with the new device.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the device pairing is with a PIN code
- For a Bluetooth v2.1 (or above) phone the device pairing is without a PIN code

Proximity pairing is based on finding and pairing with the closest phone. To do this, the device finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and it is defined as the closest device. The device then attempts to pair with and connect to this device.

Proximity pairing is configurable using the Headset Configuration Tool available from www.csrsupport.com.

16.1.9 Proximity Connection

Proximity connection is an extension to proximity pairing, see Section 16.1.8. It enables the device-user to take advantage of the proximity of devices each time the device powers up and not just during a first time pairing event.

Proximity connection enables a user with multiple handsets to easily connect to the closest discoverable phone by comparing the proximity of devices to the device at power-on to the list of previously paired devices.

Proximity connection speeds up the device connection process. It requires the device to initiate a SLC connection to the nearest device first and combines this with the device's storage of the last 8 paired/connected devices. Using proximity connection means functions operate equally well for the most or least recently paired or connected device.

16.2 6th Generation 1-mic CVC ENR Technology for Hands-free and Audio Enhancements

1-mic CVC full-duplex voice processing software is a fully integrated and highly optimised set of DSP algorithms developed to ensure easy design and build of hands-free products.

CVC enables greater acoustic design flexibility for a wide variety of environments and configurations as a result of sophisticated noise and echo suppression technology. CVC reduces the affects of noise on both sides of the conversation and smartly adjusts the receive volume levels and dynamically frequency shapes the voice to achieve optimal intelligibility and comfort for the hands-free user.

The 6th generation CVC features include:

- Full-duplex AEC
- Bit error and packet loss concealment
- Transmit and receive noise suppression including WNR
- Transmit and receive Parametric Equalisation
- Transmit and receive AGC
- Noise dependent volume control
- Receive frequency enhanced speech intelligibility using adaptive equaliser
- Narrowband, wideband and frequency expansion operations

1-mic CVC includes a tuning tool enabling the developer to easily adapt CVC with different audio configurations and tuning parameters. The tool provides real-time system statistics with immediate feedback enabling designers to quickly investigate the effect of changes.

Figure 16.3 shows the functional block diagram of CSR's proprietary 1-mic CVC DSP solution for a hands-free product.

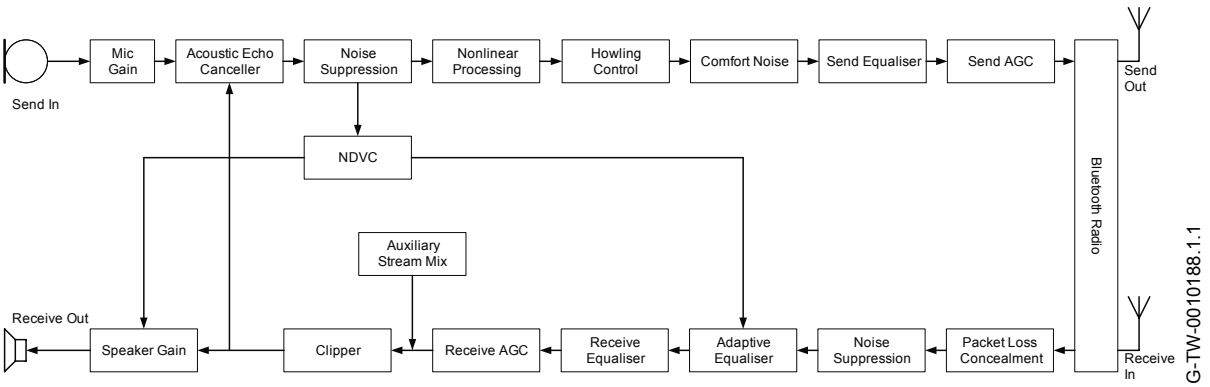


Figure 16.3: 1-mic CVC Block Diagram

Section 16.2.1 to Section 16.2.13 describe the audio processing functions provided within CVC.

16.2.1 Acoustic Echo Cancellation

The AEC includes:

- A referenced sub-band adaptive linear filter that models the acoustic path from the receive reference point to the microphone input
- A non-linear processing function that applies narrowband and wideband attenuation adaptively as a result of residual echo present after the linear filter.

16.2.2 Noise Suppression with Wind Noise Reduction

The signal-channel noise suppression block is implemented in both signal paths. They are completely independent and individually tuned. Noise suppression is a sub-band stationary / quasi-stationary noise suppression algorithm that uses the temporal characteristics of speech and noise to remove the noise from the composite signal while maximising speech quality. The current implementation can improve the SNR by up to 20dB.

In the transmit path, noise suppression aggressiveness is typically 95% improving SNR by 15 to 19dB to compensate for the upstream processing and to maintain superior voice quality, while the Rx is typically tuned down to 80% improving SNR by 8 to 12dB because of the cellular network processing. The user can parametrically adjust these default settings.

The noise suppression block contains a new WNR feature (send path only). The WNR removes unwanted noise during a hands-free conversation, cleaning the audio for the far-end listener. It detects and tackle winds of various intensities and durations. Once the wind is detected, a good balance between voice quality and WNR is achieved.

16.2.3 Non-linear Processing (NLP)

The non-linear processing module detects the presence of echo after the primary sub-band linear filter and adaptively applies attenuation at frequencies where echo is identified. It is used to minimise echo due to non-linearity caused by the system, i.e. the loudspeaker and microphone, amplifiers, electronics etc. CSR recommends minimal use of non-linear processing due to the inherent distortion that it introduces.

16.2.4 Howling Control (HC)

The Howling Control is a programmable coupling threshold that when triggered applies attenuation to the send path. This control enables CVC to operate in car-to-car calls without experiencing echo events during very high volume situations.

16.2.5 Comfort Noise Generator

The CNG:

- Creates a spectrally and temporally consistent noise floor for the far-end listener.
- Adaptively inserts noise modelled from the noise present at the microphone into gaps introduced when the non-linear processing of the AEC applies attenuation. The noise level applied is user-controllable.

16.2.6 Equalisation

The equalisation filters:

- Are independent in the send and receive signal channels
- Are independently enabled
- Are configurable to achieve the required frequency response
- Each channel comprises of 5 stages of cascaded 2nd order IIR filters
- Compensate for the frequency response of transducers in the system, i.e. the microphone and loud speaker

16.2.7 Automatic Gain Control

The AGC block attempts to:

- Normalise the amplitude of the incoming audio signal to a desired range to increase perceived loudness
- Reduce distortion due to clipping
- Reduce amplitude variance observed from different users, phones and networks

Maintaining a consistent long-term loudness for the speech ensures it is more easily heard by the listener and it also provides the subsequent processing block a larger amplitude signal to process. The behaviour of the AGC differs from a dynamic range audio compressor. The convergence time for the AGC is much slower to reduce the non-linear distortion.

16.2.8 Packet Loss Concealment

Bit errors and packet loss can occur in the Bluetooth transmission due to a variety of reasons, e.g. Wi-Fi interference or RF signal degradation due to distance or physical objects. As a result of these errors, the user hears glitches referred to as *pops* and *clicks* in the audio stream. The PLC block improves the receive path audio quality in the presence of bit and packet errors within the Bluetooth link by using a variety of techniques such as pitch-based waveform substitution.

The PLC tries to re-synthesise the lost packet from the history buffer with the same pitch period. The PLC uses a highly efficient 3-phase pitch estimator and performs cross-fading at the concatenation boundaries, i.e. the PLC attempts to clean up the audio signal by removing the *pops* and *clicks* and smoothing out gaps. This improves the audio quality for the user and the improved signal enables proceding processing blocks to perform better.

The PLC significantly improves dealing with bit errors, using the BFI output from the firmware. The DSP calculates an average BER and selectively applies the PLC to the incoming data. This optimises audio quality for a variety of bit errors and packet loss conditions. The PLC is enabled in all modes.

Note:

The PLC is enabled in all modes, HFK (full processing), pass-through and loopback by default.

16.2.9 Adaptive Equalisation (AEQ)

The adaptive equalisation block improves the intelligibility of the receive path voice signal in the presence of near end noise by altering the spectral shape of the receive path signal while maintaining the overall power level. It has been empirically observed that consonants, which are dominantly high frequency based and much lower in amplitude than vowels, significantly contribute to the intelligibility of the voice signal. In the presence of noise, the lower amplitude consonants become masked by this noise. Therefore, by increasing the frequency components that contribute to the consonants while in the presence of noise, the intelligibility can be improved. In order to maintain a consistent amplitude level, the adaptive equalization block will adaptively increase the high frequencies relative to the middle frequencies and also reduce the low frequencies accordingly. The adaptive equalizer also has the capability to compensate for variations in voice transmission channels, which include farend devices and telecommunication channels.

The Frequency Emphasis feature can be used with any standard narrow band call, when the DAC is operating at a sample rate of 8kHz. To complement the AEQ, High Frequency Emphasis can be added to improve the intelligibility of the far end caller. The emphasis feature repairs frequencies (3469Hz to 4000Hz) that were lost due to the filters of the cellular network and Bluetooth link. Information contained in the original speech from 281Hz to 3469Hz is used to reconstruct the lost high frequency content.

The Frequency Expansion feature can be used with any standard narrow band call, but a special mode is invoked when the DAC operate at a sample rate of 16kHz. The frequency expansion allows users to add in frequencies far beyond the band limits caused by the cellular network and Bluetooth link. These expansion frequencies are added between 3469Hz and 6156Hz. As in frequency emphasis, it uses the information contained in the original speech from 281Hz to 3469Hz to reconstruct the lost high frequency content.

16.2.10 Auxiliary Stream Mix

The auxiliary stream mixer enables the system to seamlessly mix audio signals such as tones, beeps and voice prompts with the incoming SCO stream. This avoids any interruption to the SCO stream and as a result prevents any speech from being lost.

16.2.11 Clipper

The clipper block intentionally distorts or *clips* the receive signal prior to the reference input of the AEC in order to more accurately model the behaviour of the post reference input blocks such as the DAC, power amplifier and the loudspeaker. The AEC attempts to correlate the signal received at the reference input and the microphone input. Any non-linearities introduced that are not accounted for after the reference input will significantly degrade the AEC performance. This processing block can significantly improve the echo performance in cheap non-linear system designs.

16.2.12 Noise Dependent Volume Control

The NDVC block improves the intelligibility of the receive path signal by increasing the analogue DAC gain value based on the send noise estimate from the send path noise suppression block. As the send noise estimate increases, the NDVC algorithm increases the analogue DAC gain value. The NDVC uses hysteresis to minimise the artefacts generated by rapidly adjusting the DAC gain due to the fluctuation in the environmental noise.

16.2.13 Input Output Gains

Fixed gain controls are provided at the input to the CVC system. The mic gain is used set the ADC level so that proper levels can be set according to hardware constraints, industry standards and the digital resolution of the DSP fixed point processor. The speake gain represents the output DAC which drive the speaker. The DAC level varies under software control for events such as the Bluetooth volume, NDVC, tone mixing and other volume based activities.

16.3 Music Enhancements

16.3.1 Audio Decoders

CSR8615 QFN supports:

- A wide range of standard decoders:
  - SBC
  - MP3
  - AAC
- Faststream codec:
  - Low-latency
  - No video/lip-sync issues while watching a video or playing games
- Jitter handling and high quality sample rate matching
- Low power consumption

16.3.2 Configurable EQ

The configurable equaliser on the CSR8615 QFN:

- Each EQ filter contains up to 5 fully tuneable stages of cascaded 2nd order IIR filters per bank
- Enables compensation for imperfections in loudspeaker performance and frequency adjustments to the received audio to enhance music brightness
- Contains tiering for multiple customer presets, e.g. rock, pop, classical, jazz, dance etc.
- Contains an easy to use GUI, with drag points, see Figure 16.4

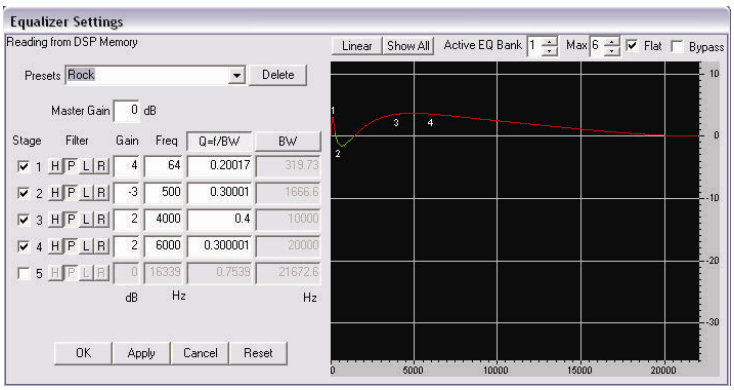


Figure 16.4: Configurable EQ GUI with Drag Points

- Is configurable with up to 6 switchable bank presets. This enables the device user to select between the EQ bank presets through button presses.

16.3.3 Volume Boost

The volume boost feature on the CSR8615 QFN is a dynamic range compander and provides:

- Additional loudness without clipping
- Multi-stage compression and expansion
- Processing modules for dynamic bass boost
- Easy to use GUI, with drag points, see Figure 16.5

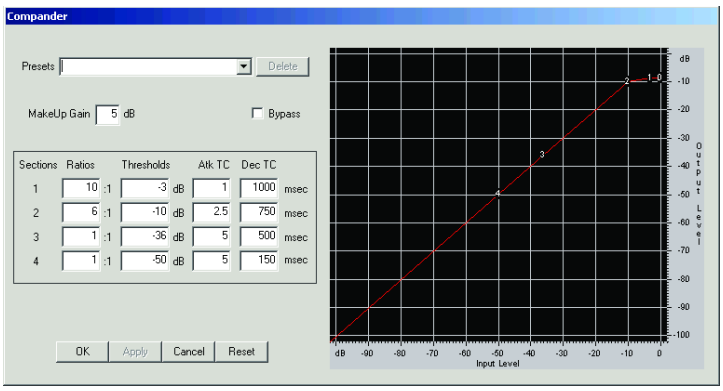


Figure 16.5: Volume Boost GUI with Drag Points

- Louder audio output without distortion

16.4 CSR8615 Mono ROM Solution Development Kit

CSR's audio development kit for the CSR8615 QFN, order code DK-8615-10161-1A, includes a CSR8615 mono ROM solution demonstrator board and necessary interface adapters and cables are available. In conjunction with the CSR8600 ROM Series Configuration Tool and other supporting utilities the development kit provides the best environment for designing audio solutions with the CSR8615 QFN.

Important Note:

The CSR8615 Mono ROM Solution audio development kit is subject to change and updates, for up-to-date information see www.csrsupport.com.

17 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

17.1 Tape Orientation

Figure 17.1 shows the CSR8615 QFN packing tape orientation.

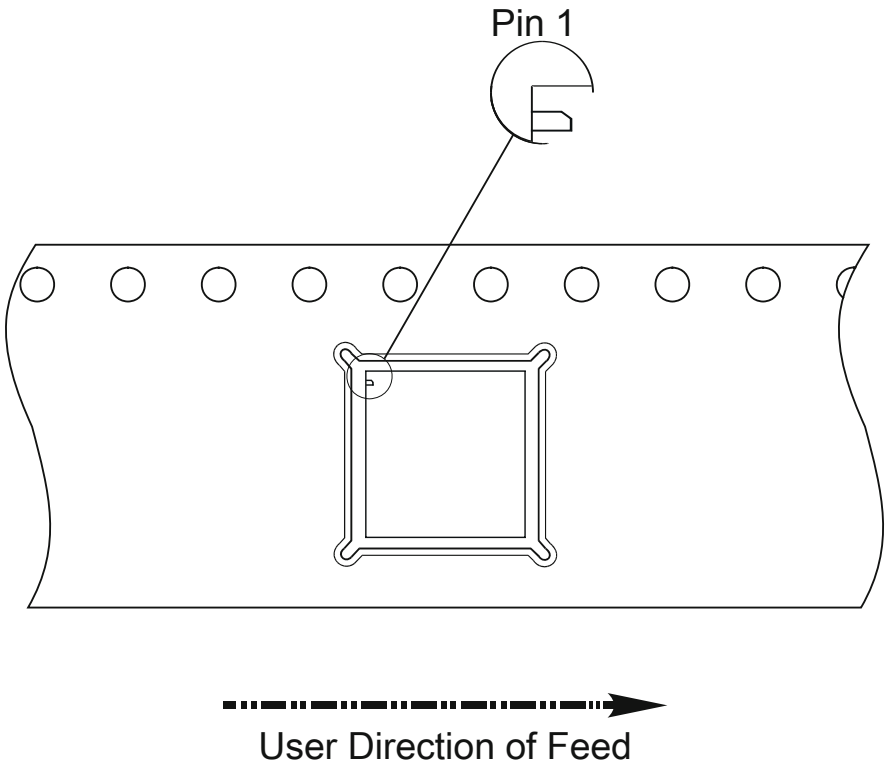
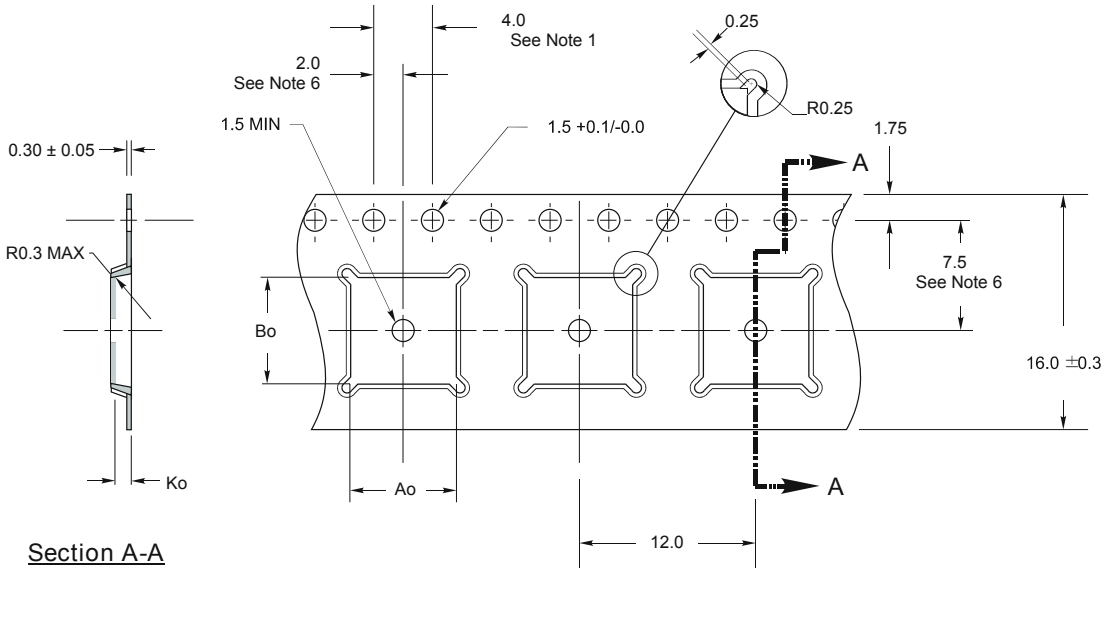


Figure 17.1: CSR8615 QFN Tape Orientation

17.2 Tape Dimensions



A_0	B_0	K_0	Unit	Notes
8.30	8.30	1.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Camber not to exceed 1mm in 100mm 3. Material: PS + C 4. A_0 and B_0 measured as indicated 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

17.3 Reel Information

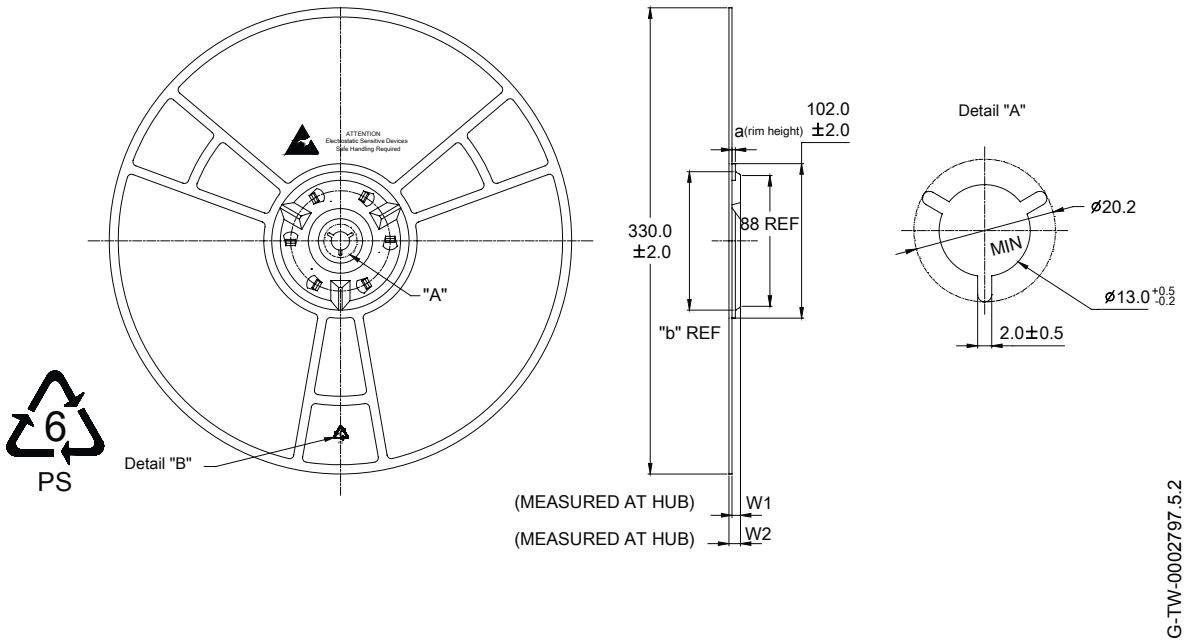


Figure 17.2: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
8 x 8 x 0.9mm QFN	16	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

17.4 Moisture Sensitivity Level

CSR8615 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

18 Document References

Document	Reference, Date
BlueCore Audio API Specification	CS-209064-DD
BlueTest User Guide	CS-102736-UG
Bluetooth and USB Design Considerations	CS-101412-AN
Core Specification of the Bluetooth System	Bluetooth Specification Version 4.0, 17 December 2009
CSR8615 QFN Performance Specification	CS-303739-SP
Electrostatic Discharge (ESD) Sensitivity Testing, Machine Model (MM)	JESD22-A115C
ESDA/JEDEC Joint Standard For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level	ANSI/ESDA/JEDEC JS-001-201
Field-Induced Charged-Device Model Test Method for Electrostatic- Discharge-Withstand Thresholds of Microelectronic Components	JESD22-C101E
IC Packing and Labelling Specification	CS-112584-SP
IEC 61000-4-2 *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*	IEC 61000-4-2, Edition 2.0, 2008-12
Kalimba Architecture 3 DSP User Guide	CS-202067-UG
Lithium Polymer Battery Charger Calibration and Operation for CSR8670	CS-204572-AN

Document	Reference, Date
Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices	IPC / JEDEC J-STD-020
Optimising BlueCore5-Multimedia ADC Performance Application Note	CS-120059-AN
Selection of I²C EEPROMS for Use with BlueCore	bcore-an-008P
Typical Solder Reflow Profile for Lead-free Device	CS-116434-AN
Universal Serial Bus Specification	v2.0, 27 April 2000
USB Battery Charging Specification	v1.2 December 7th 2010, also errata and ECNs through March 15th 2012

Terms and Definitions

Term	Definition
8DPSK	8-phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
μ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
A2DP	Advanced Audio Distribution Profile
AAC	Advanced Audio Coding
AC	Alternating Current
ACL	Asynchronous Connection-oriented
ADC	Analogue to Digital Converter
AEC	Acoustic Echo Cancellation
AFC	Automatic Frequency Control
AFH	Adaptive Frequency Hopping
AG	Audio Gateway
AGC	Automatic Gain Control
ALU	Arithmetic Logic Unit
AVRCP	Audio/Video Remote Control Profile
BCCMD	BlueCore CoMmanD
BCSP	BlueCore Serial Protocol
BEC	Bit Error Concealment
BER	Bit Error Rate
BFI	Bad Frame Indicator
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CNG	Comfort Noise Generation
codec	Coder decoder
CRC	Cyclic Redundancy Check

Term	Definition
CSR	Cambridge Silicon Radio
CTS	Clear To Send
CVC	Clear Voice Capture
CVSD	Continuously Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
DDS	Direct Digital Synthesis
DI	Device Id profile
DMA	Direct Memory Access
DNL	Differential Non Linearity (ADC accuracy parameter)
DSP	Digital Signal Processor (or Processing)
DUT	Device Under Test
e.g.	*exempli gratia*, for example
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
EIA	Electronic Industries Alliance
EMC	ElectroMagnetic Compatibility
EQ	EQualiser
eSCO	extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
etc	*et cetera*, and the rest, and so forth
FIR	Finite Impulse Response (filter)
FSK	Frequency Shift Keying
G.722	An ITU-T standard wideband speech codec operating at 48, 56 and 64 kbps
GCI	General Circuit Interface
GSM	Global System for Mobile communications
GUI	Graphical User Interface
H4DS	H4 Deep Sleep
HBM	Human Body Model

Term	Definition
HCI	Host Controller Interface
HFP	Hands-Free Profile
HSP	HeadSet Profile
I²C	Inter-Integrated Circuit Interface
I²S	Inter-Integrated Circuit Sound
i.e.	*Id est*, that is
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response (filter)
INL	Integral Non-Linearity (ADC accuracy parameter)
IPC	See www.ipc.org
IPM	Intelligent Power Management
IQ	In-Phase and Quadrature
ISDN	Integrated Services Digital Network
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression and file compression / decompression
Kb	Kilobit
LC	An inductor (L) and capacitor (C) network
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LM	Link Manager
LNA	Low Noise Amplifier
LSB	Least Significant Bit (or Byte)
MAC	Multiplier and ACcumulator
Mb	Megabit
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MISO	Master In Slave Out

Term	Definition
MLC	MultiLayer Ceramic
MMU	Memory Management Unit
MP3	MPEG-1 audio layer 3
mSBC	modified Sub-Band Coding
N/A	Not Applicable
NDVC	Noise Dependent Volume Control
NSMD	Non-Solder Mask Defined
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIN	Personal Identification Number
PIO	Parallel Input/Output
PIO	Programmable Input/Output, also known as general purpose I/O
PLC	Packet Loss Concealment
plc	public limited company
PS Key	Persistent Store Key
PWM	Pulse Width Modulation
QFN	Quad-Flat No-lead
RAM	Random Access Memory
RC	A Resistor and Capacitor network
RF	Radio Frequency
RGB	Red Green Blue
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SBC	Sub-Band Coding

Term	Definition
SCL	Serial Clock Line
SCMS	Serial Copy Management System (SCMS-T). A content protection scheme for secure transport and use of compressed digital music
SCO	Synchronous Connection-Oriented
SDA	Serial DAta (line)
SIG	(Bluetooth) Special Interest Group
SLC	Service Level Connection
SMPS	Switch-Mode Power Supply
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TBD	To Be Defined
TCXO	Temperature Compensated crystal Oscillator
THD+N	Total Harmonic Distortion and Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
VoIP	Voice over Internet Protocol
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi®	Wireless Fidelity (IEEE 802.11 wireless networking)
WNR	Wind Noise Reduction