SECTION 2 – VC-401B THEORY OF OPERATION

1. VC-401B Receiver/Synthesizer Module

A. Overview

Communication signals are detected by the VCS-40A VHF Communications System antenna and routed through the transmitter module T/R switch to the receiver module. The T/R switch is a PIN diode circuit. In the transmit mode, this same circuit connects the transmitter RF output to the antenna.

In receive mode, the incoming RF signal is routed to the receiver module (refer to Figure 2-1). The first circuit is a PIN diode attenuator and the ICAO-required FM band reject filter. The signal then goes to a varactor-tuned pre-selector, which rejects receiver image frequencies and other undesired spurious frequencies. The pre-selector accepts the desired modulated RF signals in the 118.00 MHz to 151.975 MHz range. A low noise preamplifier used in conjunction with the pre-selector minimizes losses.

The accepted RF signals are then routed from the pre-selector to a mixer. Here, the pre-selector output signal is mixed (multiplied) with the synthesizer output in the double balanced mixer to produce the IF signal at 21.4 MHz.

The IF signal is amplified and filtered from adjacent channel interference by one of two selectable filters. One filter allows for 8.33 kHz spaced channels and one for 25 kHz spaced channels. IF signal amplification is accomplished by gain controlled IF amplifiers that feed the synchronous AM demodulator. The synchronous AM detector recovers the baseband audio signal from the IF signal. The detected audio signal is routed to the audio module where it is filtered and processed for audio, squelch and level control circuits.

In addition to the demodulated AM audio signal, the detector generates a DC output for the primary Augomatic Gain Control (AGC) for the IF amplifiers and Delayed AGC (DAGC), which controls the first IF controllable amplifier and the PIN diode attenuator (PDA) located in the RF front end.

The AGC signal controls the gain of the receiver. At low signal levels, the AGC feedback is set for maximum gain of the receiver. As the input signal level increases, the detected AGC signal increases until the DAGC threshold is reached and the overall gain of the receiver starts to decrease. This action maintains the 21.4 MHz IF output signal at the detector operating point.

The receiver module synthesizer supplies the excitation for the transmitter and receiver mixer. Channel-frequency data for the synthesizer is provided by the controller in the audio module. The synthesizer operates at frequencies from 118.000 MHz to 151.975 MHz in the transmit mode. In the receive mode, a 21.4 MHz offset results in local oscillator frequencies of 139.400 MHz to 173.375 MHz to provide the high-side mixer local oscillator injection.

When activated, a transmit interlock circuit sets the PDA for a nominal 10 dB of attenuation at the receiver input to reduce crosstalk between transceivers in dual installations. A Digital to Analog Converter (DAC) controlled by the CPU module provides the tuning voltage to tune the varactors in the pre-selector filter.

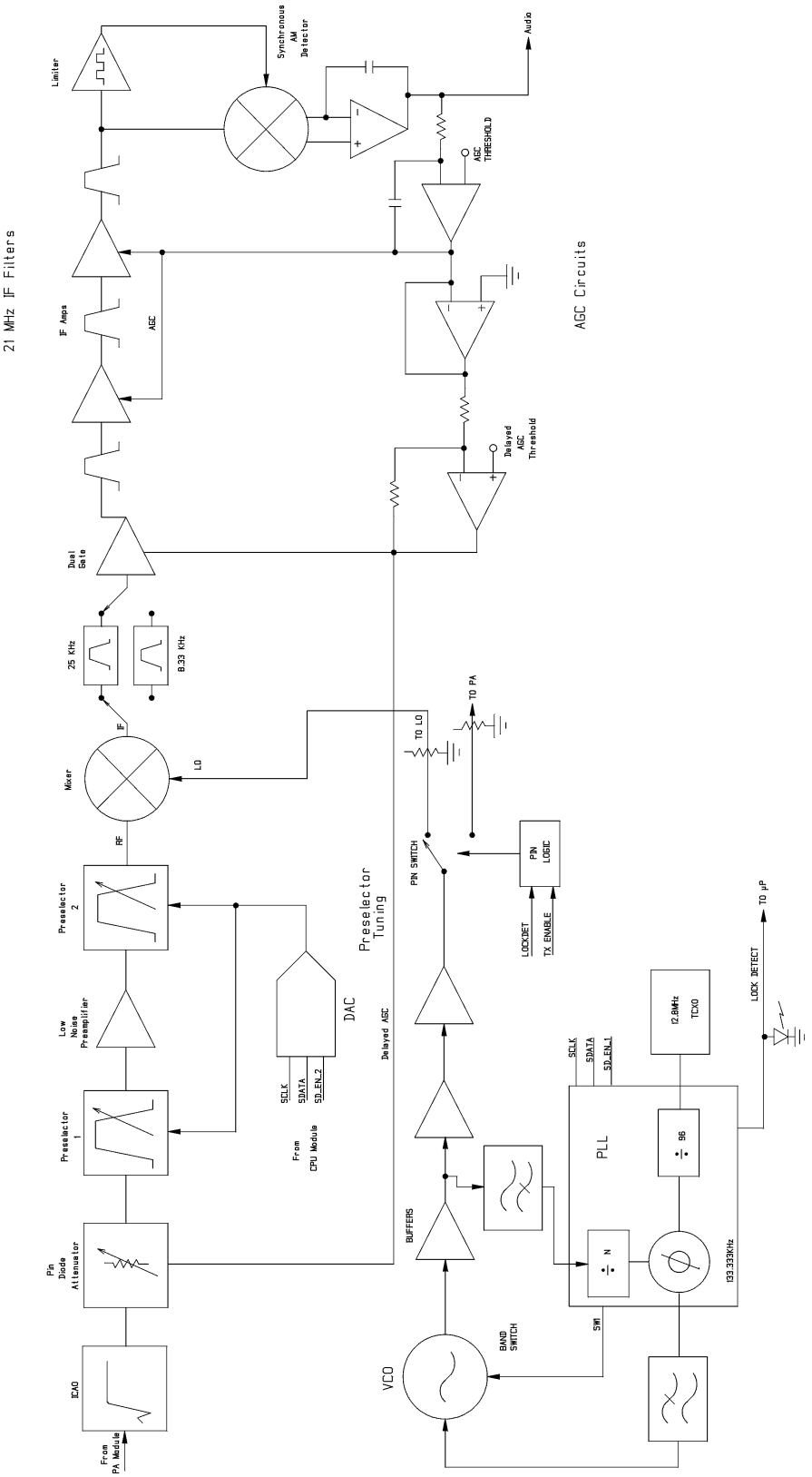

Figure 2-1. VC-401B Receiver/Synthesizer Module Block Diagram

B. Detailed Receiver Circuit Theory

The detailed theory of operation for the VC-401B is covered in the following paragraphs. Each module circuit is described in detail, explaining how the circuit converts the inputs to the desired outputs. Very common circuits are described simply, while new or complex circuits are described more completely.

The VC-401B VHF Communications Transceiver uses a receiver/PLL module combination operating in the 118.000 to 151.975 MHz frequency range with 25 kHz and 8.33 kHz channel spacing. The VC-401B receiver is a solid-state, single-conversion superheterodyne AM receiver featuring a frequency-synthesized local oscillator.

(1) 118.000 to 151.975 MHz Receiver Front-End Circuits

(a) First Pre-selector and PIN diode Attenuator

The received RF signal from the VC-401B antenna is coupled through the transmitter module to the receiver's first pre-selector. Coaxial connectors J301 and J2 and the ribbon cable connector P2 provide the receiver interconnections.

The PIN diode Attenuator (PDA) comprises PIN diodes CR301 and CR302 and associated components. A bias voltage of 10 volts to 0 volts coming from buffer amp U303-A controls the amount of current delivered to the series section (lower diodes of CR301 and CR302) and the parallel section (upper diodes of CR301 and CR302). By controlling the current through the PIN diodes, the resistance of the diodes can be controlled. The diodes are arranged to form a variable attenuation “PI” pad. As a result, the circuits surrounding the PDA remain matched to the 50 ohm source and load impedances as attenuation is increased. In this way, the effects of varying input or circuit impedances are reduced.

The main advantage of using a PDA is to protect the receiver front end from distortion at higher input signal levels. The PDA is actually controlled by the DAGC. The PDA will have minimal insertion loss at low signal levels, and therefore will not adversely affect the receiver sensitivity. When a strong signal coming through the IF has been detected, the DAGC reaches a voltage where the PDA begins to attenuate to protect the receiver front end from overload. As higher level signals are input to the receiver front end, the attenuation of the PDA is increased. The PDA has around 35 dB of control range.

The PDA is also used as part of the receiver’s transmit interlock circuitry. In dual transceiver installations, keying the adjacent transceiver’s transmitter will send a transmit interlock signal to the receiver to turn on Q300. This allows a nominal 2 volts at the input of buffer U303-B to be routed to U303-A to set the PDA for, as an example, 10 dB of attenuation. If the AGC is already setting the PDA for more than the 10 dB of attenuation, the diode OR established by dual diode CR310 will negate the effect of setting the transmit interlock.

Following the PDA is the FM immunity filter comprising C307, C305, C334, C335, C336, C337, C338, C339, L315 and L316. This filter is an elliptic high-pass filter designed to provide additional frequency rejection for strong signals in the FM radio band as required by ICAO.

The FM immunity filter is followed by the first pre-selector filter. The pre-selector is made up of varactor-tuned resonators comprising fixed components and voltage variable capacitors. The fixed portion of the pre-selector includes variable inductors L303 and L305, fixed capacitors C300 and C311, and coupling inductor L304.

Variable inductors L303 and L305 tune the front end to maximize gain by centering the bandpass of the receiver on the desired frequency. Varactors CR304 and CR305 change capacitance as the tuning voltage from U305 changes.

When a tuning voltage is applied to varactor CR304, the capacitance of the varactor is applied electrically in parallel with L303 and C308, causing the new tank circuit configuration to resonate at a higher frequency as shown in Figure 2-2. At the same time that varactor CR304 is electrically tuned, varactor CR305 is also controlled in the same way, adding the capacitance of CR305 in parallel with the C311 and L305 tank circuit. The center frequency changes each time there is a change in the tuning voltage. The resultant signal is routed to RF amplifier Q301.

(b) Digital Pre-selector and Synthesizer Control

The DAC U304 circuit establishes the tuned bandpass center frequency of the pre-selector from serial data received from VC-401B CPU module, which in turn was established by the frequency set on the CD-402B Control Display Unit. The serial data from the CPU module consists of nineteen bits of data to control the PLL frequency synthesizer and eight bits of data to control the selectivity of the first and second pre-selector.

The first nineteen bits of data to be received is routed to PLL frequency synthesizer U100 to establish the operating frequency of the VC-401B. The remaining eight bits of serial data from the CPU module are routed to DAC U304.

The serial data sent to U304 is converted from a current to voltage output in opamp U303D to establish a specific voltage level for the digital equivalent of the frequency desired. The voltage output from U303D pin 14 is level shifted and further amplified by U305 to supply the tuning voltage to the first and second pre-selectors. Figure 2-2 shows how the variable receiver bandpass is controlled by the DAC voltage

(c) RF Amplifier

The output signal from the first pre-selector is amplified by a common gate JFET amplifier Q301. The dynamic range of JFET Q301 provides enough gain without distortion to the RF signal to overcome the insertion loss evidenced in the first stage of filtering.

The filtered output of the first pre-selector appears at pin 2 of L305 and is capacitively coupled through C312 to Q301 source. Q301 amplifies the received signal.

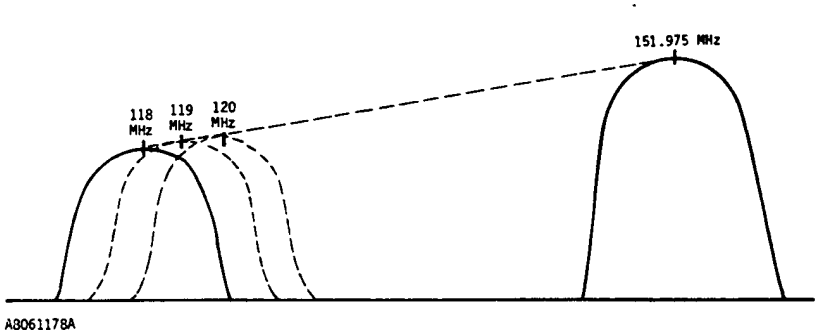

Figure 2-2. Pre-selector Bandpass Control

(d) Second Pre-selector

The amplified RF signal from the drain of Q301 is directly coupled to the second pre-selector. The second pre-selector operates in the same manner as the first pre-selector – it is a tuned varactor resonator comprising fixed and electrically tuned components.

The fixed portion of the pre-selector includes variable inductors L307 and L309, fixed capacitor C317 (in parallel with the output capacitance of Q301), fixed capacitor C318 and coupling inductor L308. Variable inductors L307 and L309 tune the second pre-selector to maximize sensitivity of the receiver by centering the bandpass on the desired frequency. Varactors CR306 and CR308 change capacitance as the tuning voltage from U305 changes.

When a tuning voltage is applied to varactor CR306, the capacitance of the varactor varies electrically in parallel with L307, causing the new tank circuit configuration to resonate at a different frequency. At the same time varactor CR306 is electrically tuned, varactor CR308 is also controlled in the same way, adding the capacitance of CR308 in parallel with the C318 and L309 tank circuit. The center frequency changes each time there is a change in the tuning voltage. The filtered signal is routed to double balanced mixer MX300.

(2) Double Balanced Mixer and the Local Oscillator

Double balanced mixer MX300 functions to heterodyne the received RF signal applied to pin 3 with the injected local oscillator signal applied to pin 6. The local oscillator frequency is developed from the phase-locked loop module and Voltage Controlled Oscillator (VCO). The resulting 21.4 MHz IF frequency at MX300 pin 2 is the difference between the VCO frequency and the desired received RF frequency.

For the VC-401B RF receiver operating in the 118.000 to 151.975 MHz frequency range, the injected local oscillator frequency is offset 21.4 MHz higher for incoming RF signals. The corresponding local oscillator frequency is 139.400 to 173.375 MHz.

(3) First IF Amplifier and Crystal Filters

The first IF amplifier uses a JFET for high dynamic range and low noise figure. The crystal filters provide selectivity and minimize spurious response.

The 21.4 MHz IF output of double balanced mixer MX300 is capacitively coupled through C319 to the source of a common gate JFET amplifier comprising Q302 and associated components. DC bias to Q302's source is fed through L312 from bias control resistor R320. Additionally, inductor L312 and capacitor C319 provide matching to the mixer. Inductors L313 and L314, along with C323, resonate with Q302's output capacitance to match the amplifier to 50 ohms at the IF frequency. Inductor L314 provides bias current feed through from +12 volts DC through R322. The signal is then passed through coupling capacitor C401 to the input IF filter selection PIN diode Switch (PDS) made up of CR401 and CR402.

The VC-401B receiver design incorporates two crystal filter sets, FL401 and FL402. FL401 is designed to operate at 25 kHz channel spacing; FL402 is designed for 8.33 kHz channel spacing. The desired filter is selected by the microprocessor depending on the radio frequency selected.

If the displayed frequency is divisible by 25 kHz (for example, 118.025 or 136.000), the wider bandwidth filter is selected in the radio. If the displayed frequency is divisible by 5 kHz but not by 25 kHz (for example, 118.030 or 136.005), the narrow filter is selected in the radio.

The IF filter section of the receiver consists of the 8.33 kHz crystal filter set, FL402A through FL402E, the 25 kHz crystal filter, FL401A through FL401D, input PDS, CR401 and CR402, output PDS, CR403 and CR404, and the band select drivers, U407C and U407D.

(a) Filter selection

The $\overline{8.33}$/25 control signal is routed from the CD-402B to the receiver where the signal is directed to the band select comparator/drivers, U407C and U407D. If this signal is greater than 2.5 volts (this threshold is established by R455 and R456), the 25IF signal at pin 8 of U407C goes to the high voltage rail of the opamp and the 8IF signal at pin 14 of U407D goes to the low voltage rail of the opamp.

The high voltage on the 25IF signal biases pins 3 to 2 of CR401 and pins 1 to 3 of CR404 “ON”. The amount of current through these diodes is set by R401 and R403 and causes these PIN diodes to have only a few ohms of “ON” resistance. The high voltage also biases pins 1 to 3 of CR402 and pins 2 to 3 of CR403 into the high impedance or “OFF” condition.

When the RF signal path is established through the 25 kHz filter, the negative voltage at 8IF biases pins 2 to 3 of CR402 and pins 3 to 1 of CR403 "ON". R405, R404 and R406 set the “ON” current of these diodes to a few ohms. This same negative voltage on 8IF also biases pins 3 to 1 of CR401 and pins 2 to 3 of CR404 into the “OFF” or high impedance state.

This combination off/on diodes means that any RF signal leaking through the series “OFF” diodes is then shorted to ground through the parallel “ON” diodes. The overall effect is that the input/output PDS’s provide greater than 80 dB of isolation between selected and unselected filters. The 8.33/25 signal going low or less than 2.5 volts selects the 8.33 kHz filter in a similar manner.

(b) 25 kHz Filter

The 25 kHz crystal filter is made of the crystal pole pairs FL401A through FL401D. L402, C403, and C404 are used to match the filter input impedance to 50 ohms. L405, C410, and C409 are used to match the output impedance to 50 ohms. Capacitors C405, C406, and C408 couple the filter pole pairs.

(c) 8.33 kHz Filter

The 8.33 kHz crystal filter is made of the crystal pole pairs FL402A through FL402E. L406, C413, and C414 are used to match the filter input impedance to 50 ohms. L409, C420, and C421 are used to match the filter output impedance to 50 ohms. Capacitors C415, C416, C418, and C419 couple the filter pole pairs.

(4) Second IF Amplifier

Second IF amplifier stage dual gate MOSFET Q401 pin 4 receives the delayed AGC signal supplied from the secondary AGC amplifier circuit. A change in voltage on the gate of this transistor effects a corresponding change in the gain of the device.

The amplified output of Q401 pin 2 is transformer coupled through T401 to input pins 4 and 6 of U401, an integrated IF amplifier with a wide range AGC control. Pins 1 and 8 of U401are transformer coupled through T402 to input pins 4 and 6 of U402, a second integrated IF amplifier. Pins 1 and 8 of U401 are transformer coupled to T403 where the signal is split. The RF signal passes through two pole filter Y400, and is split. One portion of the signal goes to U403, a third integrated IF amplifier used as a limiter and the second portion of the signal passes on to U404, an NE602 monolithic double balanced mixer used as a synchronous AM detector.

(a) Primary AGC

Integrated circuits U401 and U402 are each gain controlled amplifiers that furnish most of the receiver gain and are controlled by the primary Automatic Gain Control (AGC) function. When a weak signal is received, the AGC voltage from AGC amplifier U406A is around 5.5 volts. At a higher received signal level, the AGC voltage will increase (in a positive direction) thus increasing the current into pin 5 of U401 and U402 and decreasing the IF circuit gain. Transformers T401, T402, and T403 are employed for impedance matching and improved frequency response.

(b) TX Enable

The TX Enable signal coming into the receiver goes high when the VC-401B's transmitter is keyed. This places a high rail voltage from U407A on R416. The current through R416 overrides the primary AGC voltage present on R418 and forces U402 to maximum attenuation. This has the effect of immediately cutting off any transmit signal from getting to the AM detector during transmit.

(c) 21.4 MHz 2-pole filter

Y400 is a crystal 2 pole filter with a bandwidth used to limit the IF noise bandwidth going into the detector and limiter circuits.

(5) Detector and AGC Circuits

(a) Synchronous detector

The VC-401B receiver utilizes a synchronous multiplier for detecting the AM radio signals instead of the more common envelope detector. The synchronous detector is much more linear than a conventional non-synchronous diode detector and can have up to 3 dB better sensitivity.

The main components of the synchronous multiplier are the monolithic double balanced mixer U404, the limiting amplifier U403 and the differential opamp filter, U405A. A synchronous detector works by multiplying the AM signal, $[m(t)*A(t)\ \mathrm{Cos}\ (\omega(t) + \phi_1)]$ by a CW carrier, $[B(t)\ \mathrm{Cos}\ (\omega(t) + \phi_2)]$.

- A(t) = carrier amplitude
- m(t) = message signal
- $\omega(t)$ = carrier frequency
- $\phi(t)$ = the carrier phase angle
- B(t) = carrier amplitude of an unmodulated signal

The result of this multiplication, given that the carrier frequencies are identical and the phase angles, ϕ_1 and ϕ_2, are within a few degrees of each other, is twice the IF carrier frequency and the baseband signal which is the detected AM envelope. The multiplication of the two signals is accomplished by U404.

Limiter. The gain control pin for U403 is pulled to ground through R420. This ensures the gain of the IF amplifier is maximum at all times. The drive level to the limiter and the monolithic double balanced mixer, U404, at the output of Y400 is identical. By adjusting the double balanced mixer input level with the voltage divider made up of R422 and R459, the drive level to the limiter can be maintained at a high enough level to guarantee that even a 95% AM modulated signal will be sufficiently limited to ensure good detection. The limiter produces the $[B(t) \text{ Cos } (\omega(t) + \phi_2)]$ unmodulated carrier described previously.

Differential Filter. The differential outputs of the double balanced mixer, U404, are routed to differential input filter, U405A. The function of this filter is to supply a DC average level for the AGC signal and pass the audio signal. The audio signal goes through C454 and C455 where DC component of the detection process is removed. The audio signal is then routed to the VC-401B Audio Processor. The composite AF/AGC signal is sent to the AGC circuits where the audio signal is removed.

(b) AGC Filter and Audio Amplifier Stages

The detected audio amplifier output of U405A is coupled through a low pass RC filter network consisting of resistor R421 and capacitor C468 to filter out the AF components above 1500 Hz. The resulting signal is applied to R467, U405D, R468, and C469, which filters the remaining audio frequencies and acts as the loop filter for the primary AGC. U405D has a DC voltage output proportional to the strength of the received RF signal (or to average noise level if no signal is being received) and is applied to the inverting input, pin 2, of 406A. Resistors R464 and R441 provide a positive voltage reference to set the detector operating point. Resistors R469 and R442 establish the gain of U406A.

The output of U406A is a DC level signal applied directly to U401 and U402, the primary AGC amplifiers in the receiver. The AGC amplifier output from pin 1 of U406A is also summed in with receive audio going the Audio Processor Board. Thirdly, the primary AGC output is fed to the delayed AGC amplifier U406B.

R475 and R448 form a voltage divider that establishes the level that the delayed AGC starts operating. When the primary AGC voltage rises above the delay threshold, U406A comes off the positive voltage rail to cause Q401 and the front end PIN diode Attenuator to begin attenuating the RF/IF signals. The threshold is set to start the delayed AGC at about a 25 dB signal to noise ratio. This two stage method of AGC minimizes amplification of noise and permits operation in strong signal environments.

The output from pin 7 of U406A feeds the delayed AGC linearizer circuit made up of U406C, CR411, R477 and R472. This unique design provides a piecewise linear circuit that has a gain of 1 above a preset threshold and gain of .13 below the threshold. The threshold is set by the ratios R477 and R473 while the gain below the threshold is set by ratios of R477, R472 and R472. Because of the unique circuit design, the “knee” (point where the gain changes) remains stable over temperature. The linearizer is used to smooth the gain sensitivities of the PDA and Q401, the first IF amplifier.

NOTE: R449 and R433 have been removed from the circuit board. This effectively removes U405-C, U405-B, and the associated circuitry from being used in the receiver. This circuit is a peak detector that was intended to allow the AGC to compensate for large transient peaks in the detected audio. This detector was not needed in the final design.

C. Detailed Synthesizer Circuit Theory

(1) Reference Oscillator

The reference oscillator consists of a 12.8 MHz temperature compensated crystal oscillator (TCXO) Y100 and potentiometer R143, which allows approximately ±8 ppm of frequency adjustment. The output of the TCXO is coupled through R162 and C154 to a buffer circuit comprising R149, R150, R151, and Q106. The 12.8 MHz signal is fed through C156 to the reference input of the Phase Lock Loop IC U100. The TCXO, buffer, and TCXO adjustment input voltage supply is fed from L100 and are bypassed by capacitors C153, C155, and C152.

(2) Phase Lock Loop IC

The Phase Lock Loop (PLL) IC U100 is programmed via a three wire serial control bus that originates at the microprocessor. The PLL IC provides fractional divide by n programming and generates error control current pulses based on an internal 133.333 kHz phase/frequency comparison of the reference frequency against the VCO frequency. The PLL IC also generates an analog lock detect signal and a microprocessor-controlled discrete output for VCO band switching. The supply voltage inputs are bypassed by C100 and C101. C102 provides an ac ground reference for the internal VCO input frequency buffer.

(3) Error Amp and Loop Low Pass Filter

The error current control pulses from the PLL are integrated, amplified, and filtered to provide a control voltage to the VCO. The loop amplifier and first order filter consist of U101, C108, C109, R100, R101, C104, R102, C106, C105. A second order filter consisting of R103, R104, C110, and C111 helps to further reduce VCO reference spurs. Diode CR109 acts as a clamp that prevents the VCO tuning voltage from going to the negative voltage rail during out-of-lock conditions. The tuning voltage is coupled to the VCO through inductor L106.

(4) Voltage Controlled Oscillator

The VCO is derivation of a Colpitts oscillator consisting of Q101, C118, C119, R109, R110, L115, C120, R107, R108, C117, L103, C116, C112, and CR101. These components form the low band oscillator, operating from 118 MHz to 146 MHz. Frequencies from 146 MHz to 174 MHz are obtained by switching in inductor L105 and capacitors C146, C147, and C138 by the PIN diode driver circuitry comprising U104-A, R124, R125, C148, R123, C135, R126, and PIN diode CR103. The PIN diode driver control logic is derived from a discrete output from the PLL IC and is controlled in software from the microprocessor.

(5) First VCO Buffer Stage

The VCO signal is padded by R111, R112, R113, R114, C121, and CR104. These components also provide the bias network for the first VCO buffer stage Q102, C122, C123, R115, and L107. The buffered VCO signal is coupled through R133 and C178 back to the PLL IC for phase/frequency comparison to complete the synthesizer loop. The buffered signal is also coupled through C124 to the second and third buffering stages.

(6) Second and Third VCO Buffer Stages

The second and third buffer stages provide additional gain and isolation. The second buffer stage consists of R116, R117, R118, R119, R120, C126, C127, CR104, Q103, C128, C129, R121, and L111.

Resistors R117, R118, R119, and R120 act as an interstage pad and also work with R116 to provide DC bias to Q103. C150 couples the signal to the third buffer stage consisting of R157, R158, R155, R156, R134, C149, C143, CR110, Q107, C144, C145, R154, and L112. Resistors R158, R155, R156, and R134 act as an interstage pad and also work with R157 to provide DC bias to Q107.

The final buffered signal is coupled through C132 to output filter L104, C131, and C130 and then on to the VCO injection steering circuitry. The DC supply to the buffer stages is decoupled by C125, C133, C134, and C151.

(7) VCO Injection Steering Circuitry

The final buffered VCO signal is steered to either the receiver local oscillator injection or the transmitter drive injection through a PIN diode switch. The PIN diode switch consists of U104-B, CR107, R122, R140, C139, L108, CR106, L110, R144, L109, and R145. When the unit is in the receive mode, or if the synthesizer is out of lock, CR107 and U104-B will bias PIN diode CR106 to route the VCO signal through C140 and a pad consisting of R146, R174, and R148 then on to the receiver. When the unit is in the transmit mode and the synthesizer is locked, CR106 will be biased to route the VCO signal through C141 and a pad consisting of R161, R159, and R160 then on to the transmitter.

(8) Lock Detect Circuit

The PLL IC generates analog voltage pulses of which the duty cycle is based on the amount of error between the reference and VCO frequencies. These pulses are coupled through CR105 to a filter consisting of R128, R129, C142, and R130. The output of this filter drives Q104, R131, and lock detector led CR108. This signal is also fed through R132 and R127 to Q105 and R139, which provides the proper logic levels to drive the VCO steering circuitry and the microprocessor lock detect monitor.

2. VC-401B Audio/CPU Module

A. Audio Circuitry

(1) Microphone Audio Input

Microphone bias and input filtering is provided by R201, C139, C211, B200. Microphone transmit audio is coupled by C201 to a 3000 Hz low pass filter comprising R202, C202, R203, R205, C204, and U202-A. Potentiometer R206 provides TX MIC GAIN adjustment. Unprocessed Tx mic audio is fed to the audio processing circuitry through FET switch U300-A, which is enabled only during voice transmit mode. Tx mic audio is also fed to the sidetone amplifier.

(2) Transmit Audio Sidetone Amplifier

Unprocessed Tx mic audio is fed to the sidetone amp, which consists of R325, C326, R324, and U202-D. The voltage supply lines to opamp U202 are bypassed by capacitors C329 and C330. Potentiometer R324 provides gain adjustment for the sidetone output level. Transmit sidetone audio is fed to FET switches U300-D and U304-B. FET switch U300-D feeds audio to the sidetone output amp and is enabled only when the radio is in voice transmit mode and the transmitter power amp is producing power. The voltage supply lines of U300 are bypassed by capacitors C315 and C316. The sidetone output amp comprises R327, R329, C350, U202-C, Q306, Q307, R330, R333, and T301. Transistors Q306 and Q307 provide increased current drive to provide up to 40 mW of sidetone audio through the 600 ohm balanced outputs of transformer T301. Sidetone audio can also be fed to the main audio output amplifier through FET switch U304-B. FET switch U304-B is enabled only when the radio is in voice transmit mode, the transmitter power amp is producing power, and the external SIDETONE STRAP pin on the radio is grounded. No sidetone output is provided during data transmit mode.

(3) Data Transmit Audio Input

Data transmit audio is coupled into the radio through a 600 ohm balanced transformer T200. Transformer T200 feeds a 10 kHz low pass filter consisting of R234, R233, C223, C219, R232, R231, C217, and U310. Potentiometer R210 provides Tx data gain adjustment and feeds the data audio to FET switch U300-B. Switch U300-B is enabled only during data transmit mode and couples the data audio to the audio processing circuitry.

(4) Voice/Data Transmit Audio Processing

During voice transmit mode, unprocessed Tx audio from switch U300-A is fed through FET switch U309-D, which feeds the audio compressor consisting of C300, C301, R300, C302, C303, C304, R301, R302, C305, and U301. The voltage supply lines of U301 and U309 are bypassed by C306, C351, and C352. Audio from the compressor is fed through C307 to the clipper circuit comprising R303, CR300, R347, R348, and buffer U310-A. The compressed and clipped audio is fed through FET switch U309-A to switched capacitor low pass filter consisting of R350, R306, C348, C310, and U303.

The supply line of U303 is bypassed by C311. The cutoff frequency of U303 is set for approximately 2700 Hz by the clocking frequency through R307. The signal from U303 is buffered by U308-A and is fed to a 300 Hz high pass filter comprising C344, C308, C309, R304, R305, and U308-B.

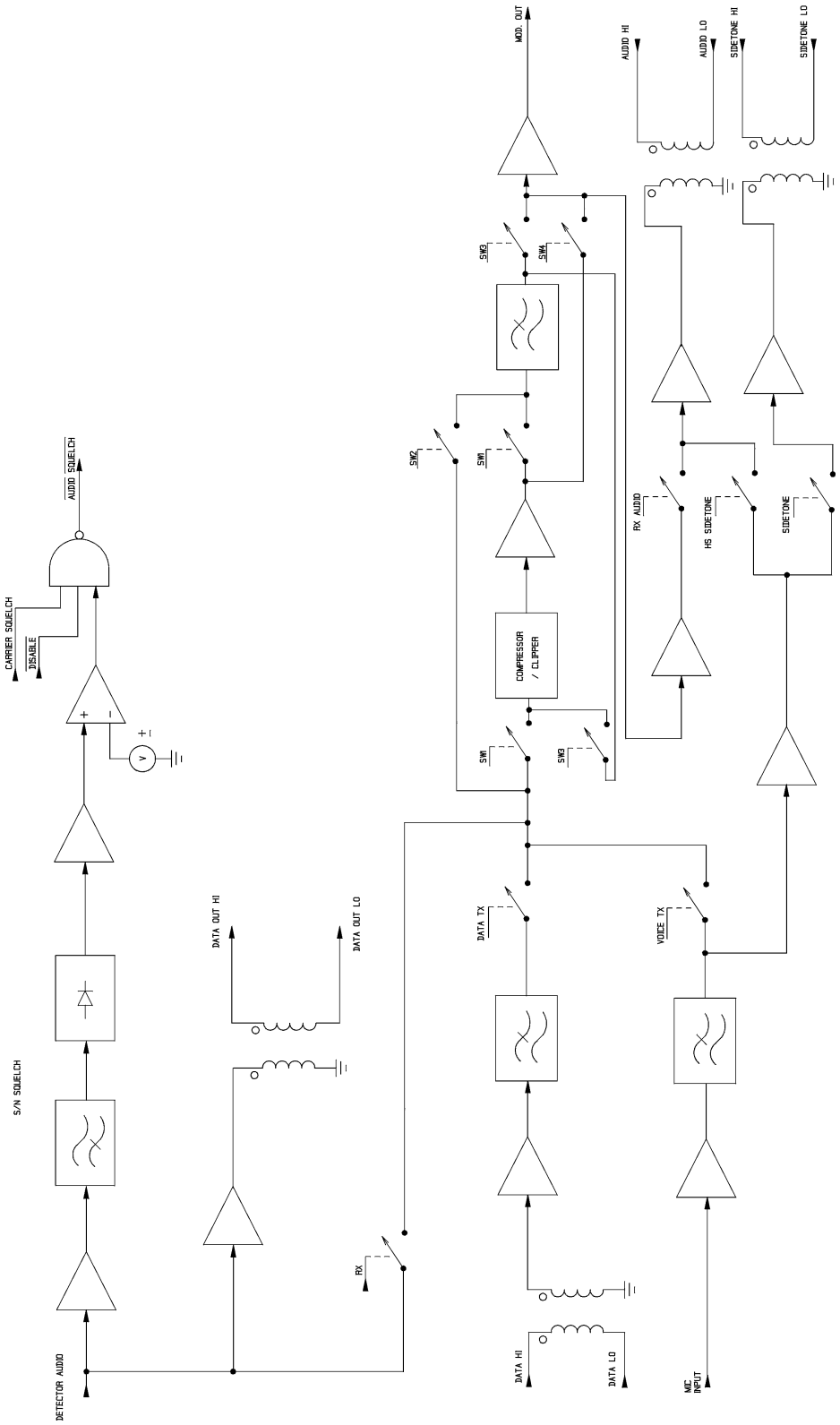

Figure 2-3. VC-401B Audio/CPU Module Block Diagram

FET switch U304-C is enabled, passing the signal to the modulation buffer amplifier consisting of R321, R310, R313, C346, and U310-B. Potentiometer R321 provides adjustment for modulation limiting. Modulation audio is fed to the power amplifier through EMI filter B300 and C341. During data transmit mode, the Tx audio is supplied from FET switch U300-B.

The audio processing path is identical to the voice mode except that the cutoff frequency for the switched capacitor low pass filter U303 is set for approximately 7000 Hz.

(5) Voice Receive Audio Processing

Detector audio from the receiver is fed to FET switch U300-C through AGC blocking cap C212 and resistor pad R221 and R224. FET switches U300-C and U309-B are enabled when the radio is in the receive mode. This routes the receive audio through the switched capacitor low pass filter U303 which is set for a cutoff frequency of approximately 2500 Hz, this provides more than 40 dB of audio reduction at 4000 Hz to accommodate operation within climax networks.

The audio is then passed through the 300 Hz high pass filter U308-B and on to FET switch U309-C. Switch U309-C is enabled, which passes the audio to the compressor and clipper circuit, then on through FET switch U304-A to the receive audio amp. The receive audio amp consists of R309, C317, R308, and U308-C. Potentiometer R308 provides audio output level adjustment.

Received audio is coupled through C318 to the squelch switch U304-D which is enabled whenever the squelch gate detection circuitry is satisfied. The voltage supply lines to FET switch U304-D are bypassed by capacitors C342 and C343. When squelch gate U304-D is enabled, the received audio is passed to the main audio output amplifier comprising R311, R314, C349, U308-D, Q302, Q303, R315, R318, and T300. The voltage supply lines for U308 are bypassed by capacitors C321 and C322.

Transistors Q302 and Q303 provide increased current drive to provide up to 40 mW of receiver audio through the 600 ohm balanced outputs of transformer T300.

(6) Carrier Squelch Detection

The detected receiver audio rides on a DC level derived from the receiver AGC and is DC coupled to the carrier squelch detector comparator comprising R211, C210, R212, R214, R215, R216, R213, and U202-B. Potentiometer R215 provides an adjustment for setting the DC level comparison for AGC carrier detect.

(7) Noise Squelch Detection

The detected receiver audio is routed through a high pass filter consisting of C213, C214, C215, R217, R218, and U204-B. This high pass filter has a low frequency cutoff of approximately 7 KHz. The noise energy is amplified and detected by C218, R219, C222, R220, U204-C, and CR201.

The detected DC noise level is buffered by U310-D then passed to the noise threshold comparator comprising R225, R226, R223, R204, R207, Q201, and U204-D. The voltage supply lines of U204 are bypassed by capacitors C224 and C225.

Potentiometer R223 provides an adjustment for setting the DC level comparison for noise squelch detect.

(8) Squelch Gate

The squelch gate consists of CR203, R222, C220, R227, R228, R229, CR202, R230, and Q200. The squelch gate will enable the receiver audio whenever any of the three gate inputs are brought low. The squelch gate inputs come from the carrier squelch detector, the noise squelch detector, or from the discrete squelch disable signal derived from the control head test function.

(9) Data Receive Audio Processing

Detector data audio from the receiver is routed directly to the data audio output amplifier consisting of C333, R336, R337, R338, C334, U204-A, Q308, Q309, R339, R342, and T302. Potentiometer R336 provides data audio output level adjustment. Transistors Q308 and Q309 provide increased current drive to provide up to 40 mW of received data audio through the 600 ohm balanced outputs of transformer T302.

B. CPU Circuitry

(1) System Control

The operation of the VC-401B is controlled by the microcontroller U101. Within this part reside the CPU, the executable code storage, the scratchpad RAM, and the non-volatile memory. Discrete inputs to the CPU are multiplexed through U105, a CPLD (Complex Programmable Logic Device). This CPLD also generates control signals used to interface the CPU with the ARINC 429 transceiver.

(2) Micro-monitor

A power-on reset, a voltage monitor, and a software watchdog timer function are contained in U102. This circuit will cause the microcontroller U101 to be reset under any of the following circumstances: power has just been applied, the power supply voltage is out of tolerance, or the software has not caused the strobe input to be pulsed within the last second.

(3) ARINC 429 Interface

ARINC 429 slow speed data is received by the VC-401B through the ARINC 429 transceiver U103. The two receive channels connect directly to the transceiver. The single transmit channel uses ARINC 429 line driver U104 to generate the proper output waveforms and voltages.

3. VC-401B Transmitter/PA Module

The power amplifier consists of an input PIN diode attenuator, 4 RF stages, all operating linear class A or class AB, a 7th order elliptic output low pass filter, a forward power directional coupler, a feedback/power control loop, a PIN diode transmit receive switch and the low level DC /switching circuits.

A. PIN Diode Attenuator

The synthesizer drive at a level of +10 dBm is applied to connector J1 and then to the input attenuator/PIN diode switch consisting of CR5, CR6, and associated blocking and bypass components. The output from CR5 controls the drive level to the first pre-driver stage Q17.

B. RF Stages

The gain and subsequently the output power of the power amplifier is controlled by varying the drive level to the PIN diode switch through op amp U5-B, gain controlled amplifier U6 and op-amp U1-C with resistor R72.

The output of pre-driver stage Q17, at 50 ohms impedance, is applied to the second pre-driver stage Q4, which also operates with an output impedance of 50 ohms. This level at approximately 700 milliwatts is applied to the first driver stage Q5, which employs a TMOS ceramic power FET; modulation is simultaneously applied to the gate of Q5 through the feedback/power control loop. The 5 watt 50 ohm unbalance output of driver stage Q5 is applied to balun transformer T1 where it is split equally, driving final output stage Q1 in a balanced manner. Q1, a push pull TMOS ceramic power FET, also operates with low level modulation from the feedback/power control loop applied to its gates.

The output from final amplifier stage Q1 at 100 watts PEP power/25 watts carrier is applied to balun transformer T4. Balun transformer T4 combines the balanced push pull output into an unbalanced 50 ohm point, which is applied to the low pass filter. Transformers T9 and T10, and T5 and T6 perform input 4:1 and output 1:4 impedance transformations, respectively, to Q1. Variable resistors R5 and R1 set the quiescent operating points of the driver and final stages Q5 and Q1, respectively.

C. Low Pass Filter

The output from balun transformer T4 is applied to the 7th order elliptic low pass filter, consisting of components C122, C124, C193, C152, C146, C153, C102, L111, L112, and L113. This filter has less than .5 dB loss in the passband of 118-152 MHz and greater than 60 dB of rejection for frequencies greater than 235 MHz. Additionally, the input and output match of the filter results in a return loss of better than –15dB and typically –20 dB within the passband of 118-152 MHz.

D. Directional Coupler

The directional coupler consists of a 50 ohm piece of coax (DC1), resistors R127, R115, and R120. With Schottky detector diode CR115 and associated bypass and coupling capacitors, it provides a forward coupled component that is 40 dB down from the main RF output level. This RF level is detected and rectified by diode CR115 and capacitors C137 and C123. Op amp U5-D, transistor Q100, and diode CR100 provide a slight forward bias to the detector diode, thereby increasing the linear operating range of the detector and providing a degree of reduction in change over temperature. The output of the detector is applied to the feedback/power control loop through resistors R2, R43, and R88, along with RF bypass capacitor C24, and on to op amp stage U1-C, which acts as a comparator.

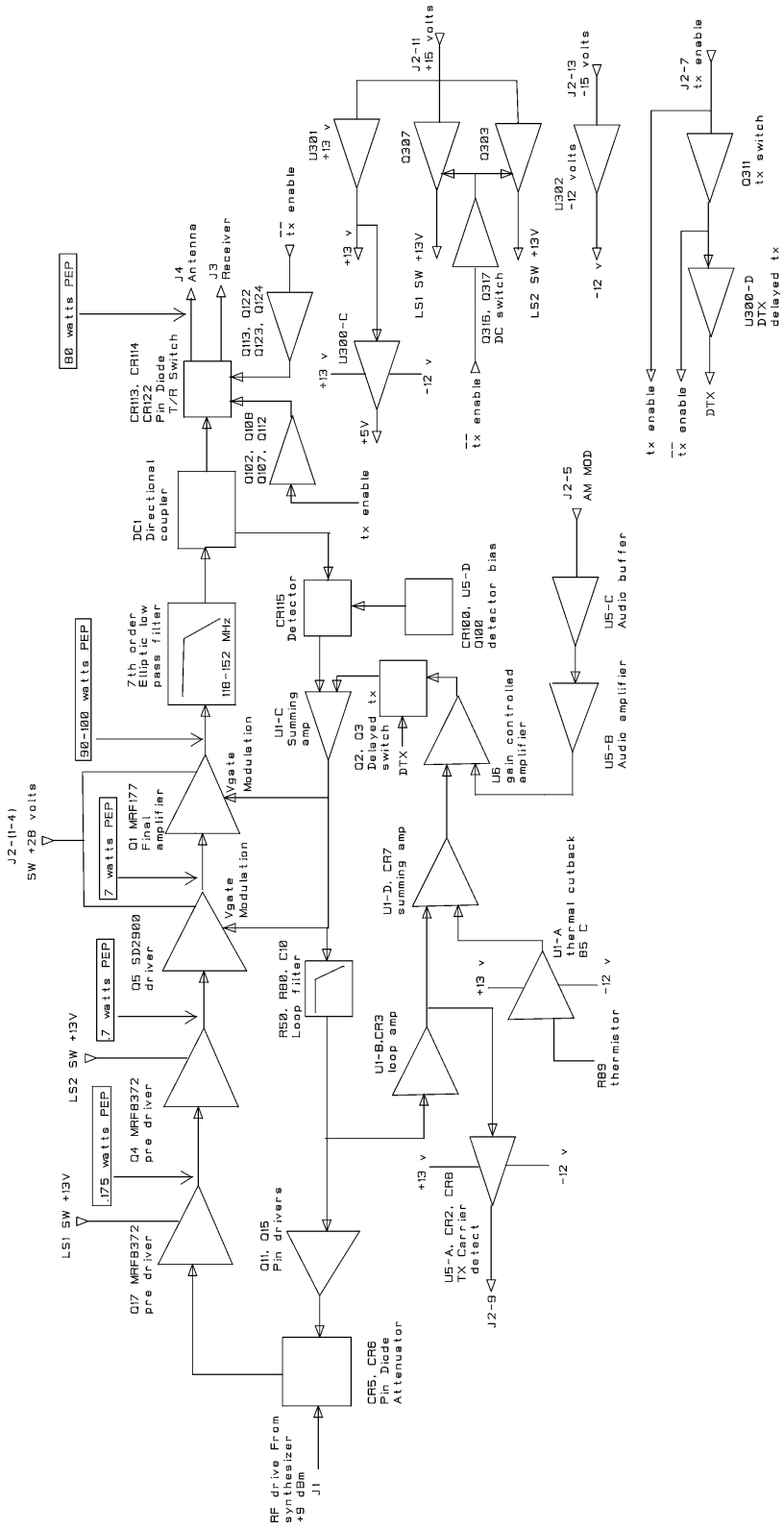

Figure 2-4. VC-401B Transmitter/PA Module Block Diagram

E. Feedback/Power Control Loop

The feedback/power control loop, which consists of op-amps U1-A, U1-B, U1-C, U1-D, U5-A, U5-B, U5-C and gain controlled amplifier U6, obtains a fixed DC reference voltage from variable resistor R72. This fixed DC reference also has a summed audio voltage applied from the modulation input at connector CONN1. This summed DC reference and audio voltage is applied to gain control amplifier U6, which itself has 2 voltages. One comes from resistors R3 and R84, which provide a fixed 2.5 Volt inner loop reference voltage. The second is a varying voltage that comes from the output of op amp U1-D, which also has two input signals summed together by diode CR7.

The main inner loop signal, which is applied to U1-D, comes from the output of U1-B and changes in proportion to the peak level of the signal detected by CR3. The second input comes from temperature control circuit U1-A and thermistor R89. These, along with components R27, R28, R29, R31 and R16, set a trip point of approximately +85 degrees C, where the power is reduced by 3 dB under conditions of extreme heat sink temperature.

The detected RF signal, which is applied to the negative terminal of op amp U1-C, is compared at its positive terminal with the output signal of gain control amplifier U6, which acts as the master power control reference voltage. If the inner loop control voltage applied to pin 3 of U6 changes, the loop will produce a correction voltage, thereby maintaining a constant output voltage to the input PIN diode attenuator. The output from U1-C is AC filtered by resistor R80 and capacitor C10 prior to driving the input PIN diode attenuator's control transistors Q11 and Q15, which set the overall input drive from the synthesizer to the power amplifier. Additionally, prior to AC filtering, the superimposed audio signal is split off and applied to the gates of driver stage Q5 and final stage Q1 through capacitor C18. Op amp stage U5-A, diode CR5, and diode CR8 provide an indication of when the power amplifier is putting out RF. Visual LED CR2 is used as an onboard indicator of RF output power. Silicon diode CR8 is applied to the output/input connector CONN1 and from there to the control head as a visual indication for the operator that the power amplifier is producing RF power.

F. PIN Diode Transmit Receive Switch

The transmit-receive PIN diode switch, which consists of PIN diodes CR113, CR114, and CR122 and various blocking and bypass capacitors and inductors, provides a faster change over from receive to transmit or vice versa than would be possible with a similar mechanical relay. When in transmit, a positive voltage produces a 55 mA forward bias DC level. This is applied to diode CR113, from transistor drivers Q112 and Q107 along with level shifting transistors Q102 and Q108, thereby passing RF from the power amplifier to the antenna through connector J102. Simultaneously, a negative voltage from driver transistors Q122 and Q113 along with level shifting transistors Q123 and Q124. This produces a reverse bias which is applied to series diode CR114, thereby turning CR114 off. It also produces a forward bias to shunt diode CR122, thereby shorting any transmit signal that may get into the receive port to ground. The level of attenuation at J101 while in transmit is typically a minimum of 50 dB. When in receive, the voltages are reversed and PIN diode CR113 is off, as is shunt diode CR122. In addition, diode CR114 is biased "ON", thereby presenting a low impedance from the antenna to the receive connector J101, resulting in passage of the receive signal to the receiver module. The level of insertion loss while in either receive or transmit through the T/R switch is typically less than .3 dB.

G. DC/Switching Circuitry

The DC switching circuitry consists of positive voltage regulatorU301 and negative regulator U302. These provide a fixed +13 volts and –12 volts to the power control loop. Additionally, there are two medium current circuits consisting of transistors Q302, Q303, Q307 and Q317, which provide collector and bias voltages to pre-driver stages Q17 and Q4, along with bias voltages to driver stage Q5 and final stage Q1. Op amp U300-C provides a fixed +5 volt reference voltage. Q311 and op amp U300-D act as logic signal inverters.

4. VC-401B Power Supply Module

A. Introduction

The Power Supply Module performs the following two functions:

- Conditioning of the raw aircraft power.
- Conversion of the nominal 28 volts to regulated voltages for circuit operation.

The operation of each of these functions is described in the following sections.

B. Aircraft Power Conditioning

The power supply conditions the aircraft power by filtering EMI either entering or leaving the box. EMI filtering is performed by the low pass filter consisting of inductors L104, L105, and capacitors C103, C112, C113, and C105.

Voltage spike protection and reverse voltage protection is accomplished by the transorb diode CR113. This diode will clip spikes with a voltage peak higher than 85 Volts. In addition to the input spike clipping, the 28 volts is clamped to a maximum voltage of 37 volts by a voltage regulator consisting of Q107, Q106, Q105, CR114, Q104, and Q103. Voltage clamping occurs when zener diode CR114 begins to conduct which turns on transistors Q104 and Q103. This reduces the drive to Q105-107, clamping the output voltage. The voltage regulator also acts as on/off power switch, which is controlled by the additional transistor Q102 and the input signal /PA Enable.

C. Switching Voltage Converter

The voltage converter is a pulse width modulation (PWM) feed forward power converter. This converter generates +28V, ±15V, and ±7.5V. The transformer T1 is driven in a push-push fashion by transistors Q100 and Q101. The drive of these transistors is modulated in duty cycle in a closed loop mode to regulate the 7.5V output. The output pulses are rectified by diodes CR112, CR111, CR109, CR108, and CR110. The rectified output voltages are filtered by the coupled inductor L100 and capacitors C107-111, and C146-149.

The 7.5V output is divided to 5V and fed back to the comparator input Pin 1 of U105. This voltage is compared to an internal 5V reference and the difference is used as the error signal to control the drive pulse width. The frequency of the switching supply is controlled by a ramp generated by R125 and Q139. This ramp voltage is fed into Pin 7 of U105 by C138 and R129 to provide a voltage to pulse width conversion via an internal comparator. This signal is also used to provide loop compensation by coupling capacitor C137. The drive pulses are generated by U105 on Pins 1 and 14. This voltage is clamped to 8.2V by the diode resistor networks consisting of CR104, CR102, R100, and R105. This clamping limits the short circuit current of Q101 and Q100.

The networks formed by CR100, CR103, C102, C101, R102, R101, R104, and R103 serve to quickly charge and discharge the gate capacitance of the drive transistors. Zener diodes CR101 and CR105 serve to protect the drive transistors from voltage spikes on the drain.

The current feeding the primary windings of transformer T1 is fed through the current sensing resistors R130, R131, and R132. This generates a voltage proportional to current that is fed to Pin 9 of U105 to provide peak current limiting for short circuit protection. R127 and C136 serve to filter the voltage spikes caused by discharging parasitic capacitance.

Regulated voltage is supplied to U105 by voltage regulator U113 on power supply startup. Once the switching supply is generating voltage, the regulated voltage is disconnected by diode CR117 and the voltage is supplied by the 15V output of the switching supply. This reduces power dissipated in U113.