FUNCTION OF EACH ACTIVE CIRCUIT DEVICE

Referring to the PARC Reader RF Module Schematic, 10405, page 2, U2 is a frequency synthesizer chip that operates in conjunction with U9, a voltage controlled oscillator (VCO). These form the primary frequency source. Provisions have been made for an alternate frequency source that would be formed by U1 and U6, but these parts are not installed or used in the PARC Reader. They are labeled as "NO LOAD" on the schematic. Amplifier U5 serves to amplify the VCO signal and switches U8, U10 and U7 would serve to switch between the primary and the (unused) alternate frequency source with a large amount of isolation. Switch U7 is not installed and switches U8 and U10 are always set to select the primary source.

On page 3, the signal path for the transmitter continues. U32 and U33 are passive double-balanced mixers configured as an amplitude modulator with an ON/OFF ratio of more than 40 dB. U27 provides the data modulating signal through a filter to the intermediate frequency (IF) ports of the mixers. An amplifier, U28, follows the modulator. The output signal from U28 is applied to the transmit driver stage, U21. The driver signal is filtered by F2 and applied to the transmit power amplifier (PA), U26. The PA output passes through a directional coupler, U24, which develops a reduced amplitude, coupled signal for the power control function, discussed later.

From the PA, the transmit signal passes through the homodyne on page 5, to a harmonic filter and on to the antenna. In the homodyne, there are two signals moving in opposite directions: the transmit signal to the antenna and the receive signal from the antenna to the homodyne. The transmit signal also acts as a local oscillator for the nonlinear mixer diodes CR15, CR11, CR2 and CR1 to provide conversion of the incoming receive signal from the antenna to the baseband in-phase (I) and quadrature (Q) differential signals, which are applied to the receiver preamp.

The baseband I and Q preamp is shown on pages 6 and 7. The amplified I-Data and Q-Data from page 7 is provided to the PARC Processor Module via pins 7 and 8 of connector P4 on page 1.

The power control circuit works as follows, referring to page 4. U23 is a logarithmic detector/controller. The power level from the directional coupler following the PA, U24 on page 3, is attenuated and applied to pins 2 and 3 of U23. The power level control or reference signal is applied to pin 7 of U23. This reference signal is developed from a D/A converter on the Processor Module, which provides a RF ATTEN signal on pin 6 of connector P4 (page 1). An RF ATTEN voltage of approximately 2.5 volts DC corresponds to a full power output of 2 watts. The voltage divider formed by R154, R166, R182, R190 and R165 precisely adjusts the reference voltage for a full power output of 2 watts. Capability is provided to decrease power up to 10 dB in one dB steps by varying the RF ATTEN signal under software control. A detected power level indication is provided to the Processor Module by CR20 and U30 on page 3.

The output of the log detector/controller IC, U23, is buffered and filtered by U30 and U31 and applied to the power control input at pin 2 of U26, the PA device.