EXHIBIT C

GENERAL INFORMATION

GENERAL INFORMATION REQUIREMENTS

Paragraph 2.983(a)

Name of Applicant: **BBM Electronics Group Ltd.**

Address of Applicant: **Kestrel House, Garth Road**
Morden, Surrey
UK SM4 4LP

Name of Manufacturer: **BBM Electronics Group Ltd.**

Address of Manufacturer: **Kestrel House, Garth Road**
Morden, Surrey
UK SM4 4LP

Paragraph 2.983(b)

Equipment Identification: **FCC ID: F3S4KMTX**

Paragraph 2.983(c)

Quantity: **1000 per year**

Production: **Unknown**

Paragraph 2.983(d)

(1) Type of Emission: **F3E**

(2) Frequency Range: **782.0 to 806.0 MHz**

(3) Power Output: **20 milliwatts**

(4) Maximum Power Rating: **20 milliwatts**

(5) DC Voltages and Currents in all elements of the final RF Stage: **See Exhibit D**

GENERAL INFORMATION REQUIREMENTS (continued)

Paragraph 2.983(d) (continued)

(6) Function of Solid State Devices:

NAME	DESCRIPTION/FUNCTION
IC1a	**AF Input Buffer**
VR1	**AF Input Buffer with IC1a**
IC2a - IC1b	**Main Audio Processor**
IC5	**LPF/Limiter**
IC10	**Digitally Controlled Attenuator**
IC11	**8 Bit Microcontroller**
IC9	**Peripheral E2 Memory**
IC8	**3 Legged Monolithic Voltage Regulator**
IC1	**PLL**
Q2	**RF Buffer**
Q3	**Driver Transistor**
Q4	**Final Power Amplifier**
Q5	**Allows Driver and Output Stages to be biased, controlled by IC11**

(7) Circuit Diagrams: **See Exhibit E**

(8) Instruction Manual: **See Exhibit F**

(9) Tune Up Procedure: **See Exhibit G**

Paragraph 2.983(d) (continued)

(10) Description of all circuitry and devices provided for determining and stabilizing frequency:

VCO & PLL

The RF signal is generated by VCO X1 which has a center frequency of 794 MHz and a control gain of approximately 10 MHz/V. The VCO is controlled via its Control Port by a PLL IC1 which consists of a 64/65 prescaler and a dual modulus digital frequency synthesizer.

The synthesizer is fed from the RF Output of the VCO via R11.

The frequency reference of the synthesizer is derived from an internal reference oscillator an external 10.0 MHz crystal X2 on board IC1. This 10.0 MHz frequency reference has a stability of +/- 15 ppm and a temperature range of -30°C to 50°C. Adjustment of frequency reference is accomplished by via trimmer VC1. This reference is internally divided by 20 to create a 25 kHz reference (Channel Spacing). The phase detector Output of IC1 is applied to R2-C1-C2-R9-C13 which form a 3 Pole Loop Filter with an LPF characteristic with a corner frequency of approximately 40 MHz. This signal is applied to the Control Terminal of the VCO.

The previous bandwidth limited AF signal present is AC coupled to the modulation pin of the VCO via C38.

(11) Circuits For Suppression of Spurious Emissions, Limiting Modulation and Limiting Power:

SPURIOUS EMISSIONS:

RF filtering is realized via Stripline filter and variable caps VC2-VC3. This filter has a band pass characteristic with 3dB points of approximately 40 Mhz coupled together with LPF elements, L7-C44-C25 thus ensuring spurious emissions are attenuated by at least -45 dB below carrier.

LIMITING MODULATION AND POWER

The frequency locked signal is applied from the VCO via C15 to RF Buffer Q2 which isolates the RF signal from the output of the VCO. The collector of Q2 is then coupled via reactive elements C17-L5 to the driver which comprises of Q3 and related tuned elements L6-C19-C45. Q3 is biased into Class A conduction over the entire frequency range. This stage is biased into Class AB conduction and provides a nominal 20 milliwatt output. Q4 as opposed to all preceding stages is powered from the 9V rail. In addition the output stage bias chain R20-R22 and driver Q3 are controlled by Q5 which allows only the driver and output stages to be biased on when the PLL is in a locked condition. Q5 is controlled via the microcontroller IC11.

(12) Digital Modulation: **Not Applicable**

Paragraph 2.983(e)

All tests and measurements shown in this report were made in accordance with the applicable FCC Rules and Regulations noted. All testing was performed at RETLIF TESTING LABORATORIES whose complete facility data package is on file with the FCC at the Laurel, Maryland laboratory. Prior to testing, the test sample is certified by the applicant to be tuned up in accordance with the manufacturer specifications and all gain controls are positioned for maximum gain during all testing.

See **Exhibit H** For Test Data and Measurement Procedures.

Paragraph 2.983(f)

Equipment Label: **See Exhibit A**

Paragraph 2.983(g)

Equipment Photographs: **See Exhibit B**

Paragraph 2.02(c)(1)

Necessary Bandwidth Determination:

The necessary bandwidth was calculated utilizing the following formula:

$B_n = 2M + 2D$ M = 15.0 kHz
D = 24.8 kHz

$B_n = 2(15.0) + 2(24.8) = 79.6$ kHz

EXHIBIT D

Paragraph 2.983 (d)(5)

DC Voltages and Currents in all
elements of the final RF stage.

Paragraph 2.983 (d)(5)

DC Voltages and Currents in all elements of the final RF stage:

STAGE	VOLTAGE (VDC)			CURRENT, mA
Final	**Base**	**Emitter**	**Collector**	**Final**
Q4	0.449	0.394	7.75	Ic = 9.55 (Q4)