Retlif Testing Laboratories

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PART 74 TYPE ACCEPTANCE
TEST REPORT ON
WIRELESS
BELTPACK TRANSMITTER
MODEL No: S3500LTX
FCC ID: F3S3K5LTX

CUSTOMER NAME: BBM Electronics Group Ltd.

CUSTOMER P.O.: A090/SB/RP

DATE OF REPORT: April 1, 1998

TEST REPORT NO.: R-7456-4

TEST START DATE: March 9, 1998

TEST FINISH DATE: March 10, 1998

TEST TECHNICIAN: D. Cortes, N. Accardi

TEST ENGINEER: T. Schneider

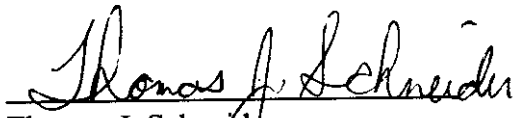
SUPERVISOR: R.J. Reitz

REPORT PREPARED BY: L. Anderson

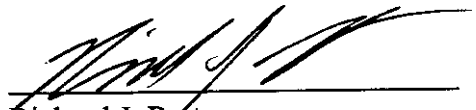
GOVERNMENT SOURCE INSPECTION: Not Applicable

CERTIFICATION AND SIGNATURES

We certify that this report is a true report of the results obtained from the tests of the equipment stated. We further certify that the measurements shown in this report were made in accordance with the procedures indicated and vouch for the qualifications of all Retlif Testing Laboratories personnel taking them.



Thomas J. Schneider
EMC Test Engineer
NVLAP Approved Signatory



Richard J. Reitz
Laboratory Manager
NVLAP Approved Signatory

NON-WARRANTY PROVISION
The testing services have been performed, findings obtained, and reports prepared in accordance with generally accepted testing laboratory principles and practices. This warranty is in lieu of all other warranties, either express or implied.

NON-ENDORSEMENT
This test report contains only findings and results arrived at after employing the specific test procedures and standards listed herein. It is not intended to constitute a recommendation, endorsement, or certification of the product or material tested. This report must not be used by the client to claim product endorsement by NVLAP or any agency of the U.S. Government.

TABLE OF EXHIBITS

EXHIBIT C

GENERAL INFORMATION

GENERAL INFORMATION REQUIREMENTS

Paragraph 2.983(a)

Name of Applicant:	**BBM Electronics Group Ltd.**
Address of Applicant:	**Kestrel House, Garth Road** **Morden, Surrey** **UK SM4 4LP**
Name of Manufacturer:	**BBM Electronics Group Ltd.**
Address of Manufacturer:	**Kestrel House, Garth Road** **Morden, Surrey** **UK SM4 4LP**

Paragraph 2.983(b)

Equipment Identification: **FCC ID: F3S3K5LTX**

Paragraph 2.983(c)

Quantity:	**1000 per year**
Production:	**Unknown**

Paragraph 2.983(d)

(1)	Type of Emission:	**F3E**
(2)	Frequency Range:	**174.0 to 216.0 MHz**
(3)	Power Output:	**10 milliwatts**
(4)	Maximum Power Rating:	**10 milliwatts**
(5)	DC Voltages and Currents in all elements of the final RF Stage:	**See Exhibit D**

Paragraph 2.983(d) (continued)

(6) Function of Solid State Devices:

NAME	DESCRIPTION/FUNCTION
IC1a	**AF Input Buffer**
VR1	**AF Input Buffer with IC1a**
IC2a - IC1b	**Main Audio Processor**
IC5	**LPF/Limiter**
IC10	**Digitally Controlled Attenuator**
IC11	**8 Bit Microcontroller**
IC9	**Peripheral E2 Memory**
IC8	**3 Legged Monolithic Voltage Regulator**
IC1	**PLL**
Q2	**RF Buffer**
TR1	**Driver Transistor**
TR2	**Final Power Amplifier**
TR3	**Allows Driver and Output Stages to be biased, controlled by IC11**

(7) Circuit Diagrams: **See Exhibit E**

(8) Instruction Manual: **See Exhibit F**

(9) Tune Up Procedure: **See Exhibit G**

Paragraph 2.983(d) (continued)

(10) Description of all circuitry and devices provided for determining and stabilizing frequency:

VCO & PLL

The RF signal is generated by VCO X1 which has a center frequency of 182 or 206 MHz depending on the status of the Bandswitch line which is controlled via the Microcontroller. The VCO has a voltage gain of approximately 6 MHz/V. The VCO is controlled via its DC Control Port by a PLL IC1 which consists of a 64/65 prescaler and a dual modulus digital frequency synthesizer.

The synthesizer is fed from the RF Output of the VCO via R19 which is directly after the VCO Buffer Q2.

The external reference of the synthesizer is derived from an internal reference oscillator an external 10.0 MHz crystal X2 on board IC1. This 10.0 MHz frequency reference has a stability of +/- 15 ppm and a temperature range of -30°C to 50°C. This reference is internally divided by 200 to create a 25 kHz reference (Channel Spacing).

The phase detector Output of IC1 is applied to R35-C73-C74-C49 which form a 2 Loop Filter with an LPF characteristic with a corner frequency of approximately 40 MHz. This signal is applied to the DC Control Terminal of the VCO.

The previous bandwidth limited AF signal present is AC coupled to the modulation pin of the VCO via C70.

(11) Circuits For Suppression of Spurious Emissions, Limiting Modulation and Limiting Power:

SPURIOUS EMISSIONS:

The main Output Filter consists of 4 poles filtering to remove any spurious harmonics of the RF Output. The first pole L7- C69 provides LPF. The preceding 2 poles possess bandpass characteristics L10-C37-L9-C38-C68-C-67. The final pole L8-C66 matches the output to 50 ohms and also acts as the final LPF section.

LIMITING MODULATION AND POWER

The frequency locked signal is applied from the VCO to RF Buffer Q2 which isolates the RF signal from the output of the VCO from the PLL. The RF signal is then attenuated by a 3 dB pad which also provides coupling to the PLL RF Input. Driver transistor TR1 has an amplifier with a low Q tuned based circuit in the collector L4-R25-C58-C60. This in turn drives the final power amplifier TR2. This stage is biased int Class AB conduction and provides a nominal 10 milliwatt output. In addition the output stage bias chain R31-R32 and driver TR1 are controlled by TR3 which only allows the driver and output stages to be biased on when the PLL is in a locked condition. TR3 is controlled via the microcontroller IC11.

(12) Digital Modulation: **Not Applicable**

Paragraph 2.983(e)

All tests and measurements shown in this report were made in accordance with the applicable FCC Rules and Regulations noted. All testing was performed at RETLIF TESTING LABORATORIES whose complete facility data package is on file with the FCC at the Laurel, Maryland laboratory. Prior to testing, the test sample is certified by the applicant to be tuned up in accordance with the manufacturer specifications and all gain controls are positioned for maximum gain during all testing.

See **Exhibit H** For Test Data and Measurement Procedures.

Paragraph 2.983(f)

Equipment Label: **See Exhibit A**

Paragraph 2.983(g)

Equipment Photographs: **See Exhibit B**

Paragraph 2.02(c)(1)

Necessary Bandwidth Determination:

The necessary bandwidth was calculated utilizing the following formula:

$B_n = 2M + 2D$ M = 15.0 kHz
D = 31.8 kHz

$B_n = 2(15.0) + 2(31.8) = 93.6$ kHz

EXHIBIT D

Paragraph 2.983 (d)(5)

DC Voltages and Currents in all
elements of the final RF stage.

Paragraph 2.983 (d)(5)

DC Voltages and Currents in all elements of the final RF stage:

STAGE	VOLTAGE (VDC)			CURRENT, mA
Final	**Base**	**Emitter**	**Collector**	**Final**
TR2	0.9	0.203	5.0	Ic = 11.25 (Q4)

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April 7, 1998

Federal Communications Commission
Equipment Approval Services
PO Box 358315
Pittsburgh, PA 15251-5315

Dear Sir/Madam:

Enclosed you will find an application for Type Acceptance of a S3500LTX Wireless Beltpack Transmitter, FCC ID: F3S3K5LTX. Type Acceptance is requested under Part 74 of the Commission's rules. This application is being filed by Retlif Testing Laboratories on behalf of BBM Electronics Group Ltd. Also enclosed is the applicable filing fee, and form 731.

I trust that you will find the enclosed application to be complete however should you have any questions or require any additional information please feel free to contact me.

Very truly yours,

RETLIF TESTING LABORATORIES

Lesley Anderson

Lesley Anderson
Administrative Coordinator

Enc. (as stated)