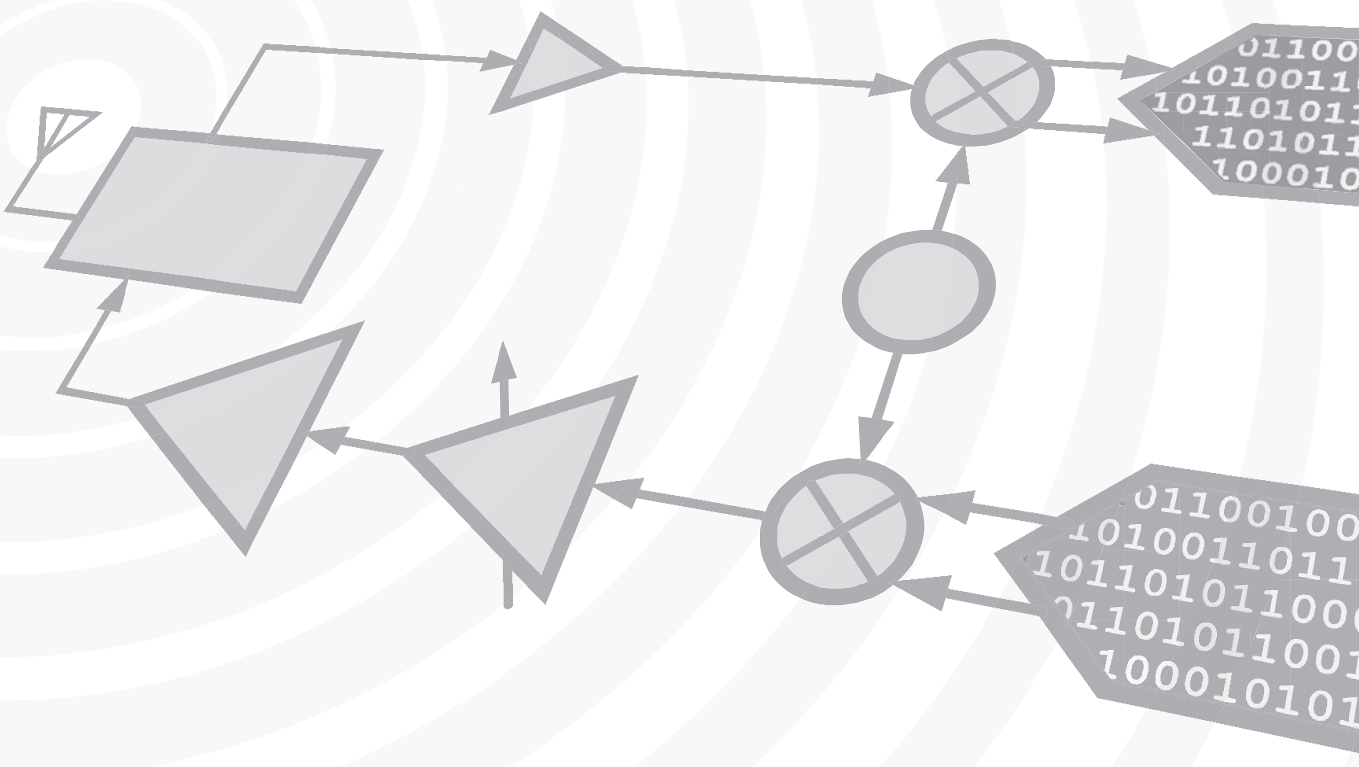
Table of Contents for Spec Sheets

Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



www.analog.com

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Hittite MICROWAVE PRODUCTS FROM ANALOG DEVICES

RoHS EARTH FRIENDLY

HMC199AMS8 / 199AMS8E

v00.0814

DUAL SPDT SWITCH DC - 2.5 GHz

Typical Applications

The HMC199AMS8 / 199AMS8E is ideal for:

- Cellular
- ISM Basestations
- PCS

Features

RoHS-Compliant Product

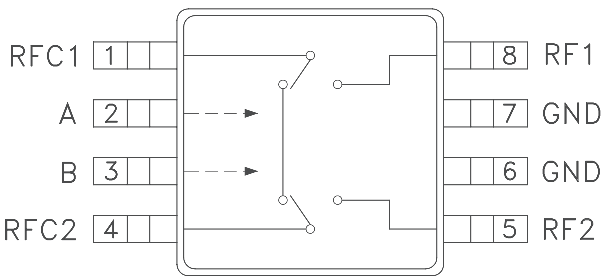
Integrated Dual SPDTs

Low Insertion Loss: <0.5 dB @ 2 GHz

Positive Control: 0/+5V, 0/+3V

Ultra Small MSOP8 Package: 14.8 mm^2

Functional Diagram



General Description

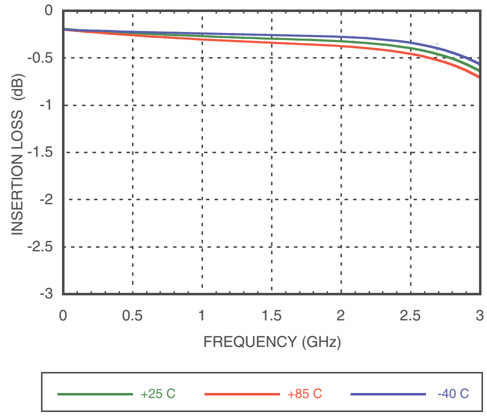
The HMC199AMS8 & HMC199AMS8E are low-cost general purpose dual SPDT GaAs “bypass” switches in 8-lead MSOP packages covering DC to 2.5 GHz. These four-RF-port components integrate two SPDT switches and a through line onto a single IC. The designs provide low insertion loss of less than 0.5 dB while switching passive or active external circuit components in and out of the signal path. Port to port isolations are typically 25 to 30 dB. On-chip circuitry enables positive voltage control operation at very low DC currents with control inputs compatible with CMOS and most TTL logic families. Applications include LNA or filter bypass switching and single bit attenuator switching. The HMC199AMS8E is a RoHS-compliant product.

Electrical Specifications, T_A = +25° C, Vctl = 0/+5 Vdc, 50 Ohm System

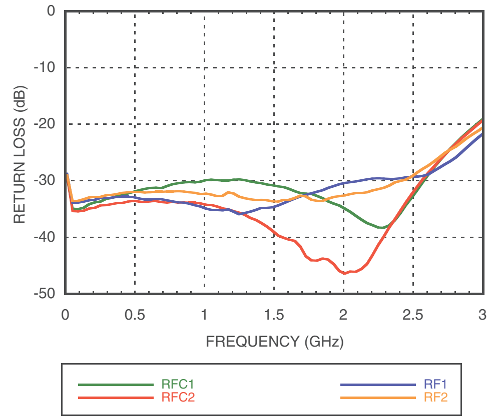
Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz		0.3 0.4 0.6	0.6 0.8 1.0	dB dB dB
Isolation (Between Ports RFC1 and RFC2 / RF1 / RF2)	DC - 2.0 GHz DC - 2.5 GHz	22 17	25 22		dB dB
Return Loss (On State, Any Port)	DC - 2.0 GHz DC - 2.5 GHz	20 20	30 30		dB dB
Input Power for 1 dB Compression	0.5 - 2.0 GHz	25	28		dBm
Input Third Order Intercept (Two-tone Input Power = 13 dBm Each Tone)	0.5 - 2.0 GHz	40	55		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 2.5 GHz		 20 40		 ns ns

For price, delivery and to place orders: Analog Devices, Inc., 2 Elizabeth Drive, Chelmsford, MA 01824
Phone: 978-250-3343 • Fax: 978-250-3373 • Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

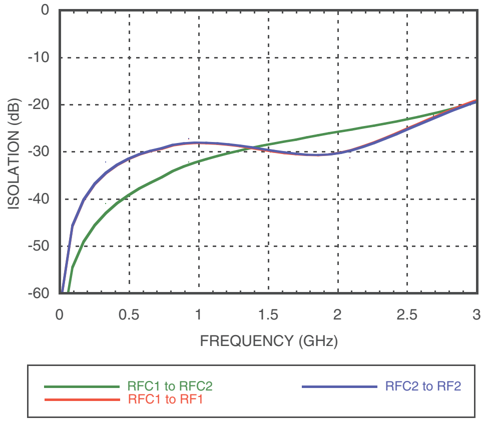
Insertion Loss



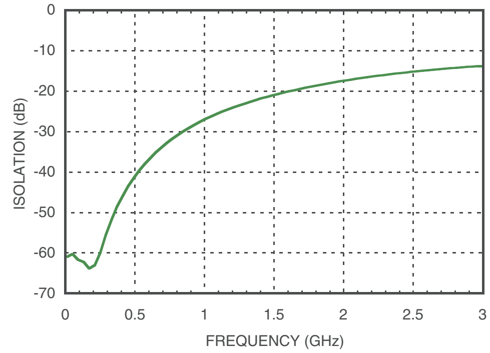
Return Loss



Isolation Between Ports RFC1 and RFC2 / RF1 / RF2

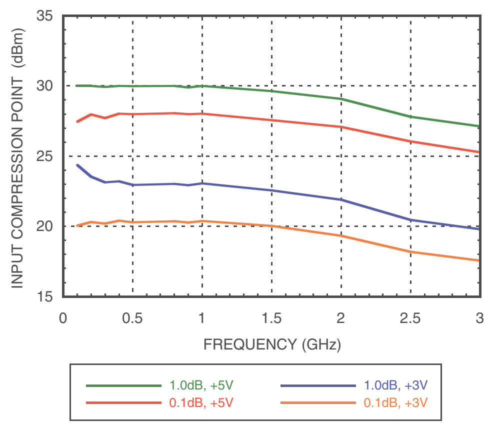


Isolation Between Ports RF1 and RF2

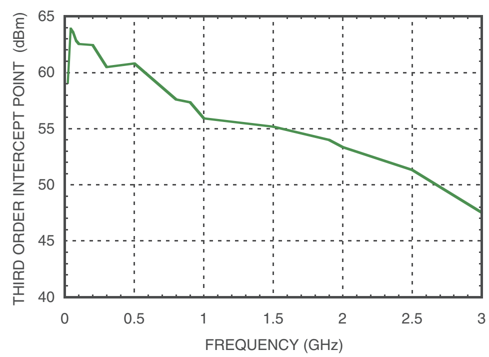


Note: RFC1 - RFC2 is in insertion loss state

0.1 and 1 dB Compression Point



Input Third Order Intercept Point



Absolute Maximum Ratings

RF Input Power V_{CTL} = 0/+5V	+29.3 dBm
Control Voltage Range (A & B)	-0.5 to +7.5 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 5.85 mW/°C above 85 °C)	0.38 W
Thermal Resistance	171 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

Truth Table

**Control Input Tolerances are ± 0.5 Vdc*

Control Input*		Control Current (Typical)		Signal Path		
A (Vdc)	B (Vdc)	Ia (μA)	Ib (μA)	RFC1 to RFC2	RFC1 to RF1	RFC2 to RF2
0	+5	-1	1	ON	OFF	OFF
+5	0	1	-1	OFF	ON	ON
0	+3	-0.1	0.1	ON	OFF	OFF
+3	0	0.1	-0.1	OFF	ON	ON

DC blocking capacitors are required at ports RFC1, RFC2, RF1, RF2. Choose value for lowest frequency of operation.

Distortion vs. Frequency

Control Input	Input Third Order Intercept (dBm) 0 dBm Each Tone	
(Vdc)	900 MHz	1900 MHz
+5	56	52
+3	52	47

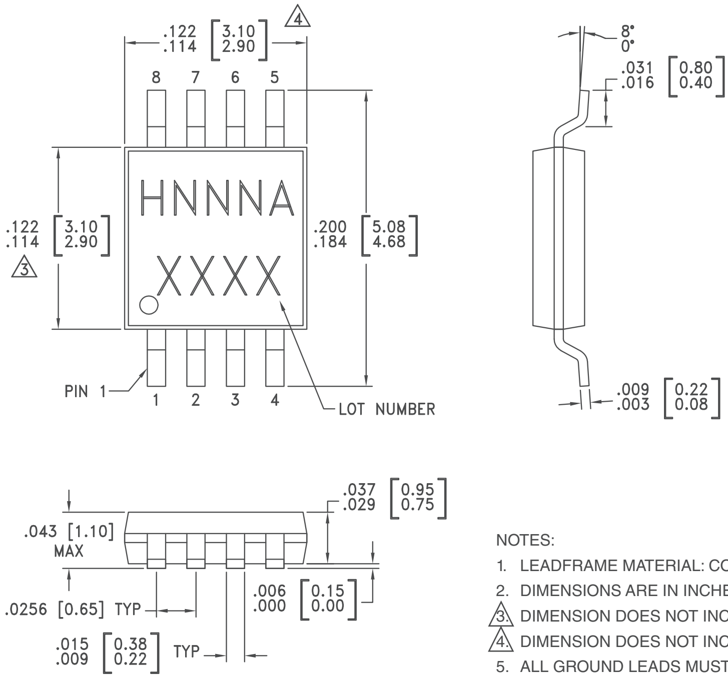
Compression vs. Frequency

	Carrier at 900MHz		Carrier at 1900MHz	
CTL Input	Input Power for 0.1 dB Compression	Input Power for 1.0 dB Compression	Input Power for 0.1 dB Compression	Input Power for 1.0 dB Compression
(Vdc)	(dBm)	(dBm)	(dBm)	(dBm)
+5	28	30	27	29
+3	20	23	20	22

Caution: Do not operate continuously at RF power input greater than 1 dB compression and do not “hot switch” power levels greater than +22 dBm (Control = 0/+5Vdc).

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

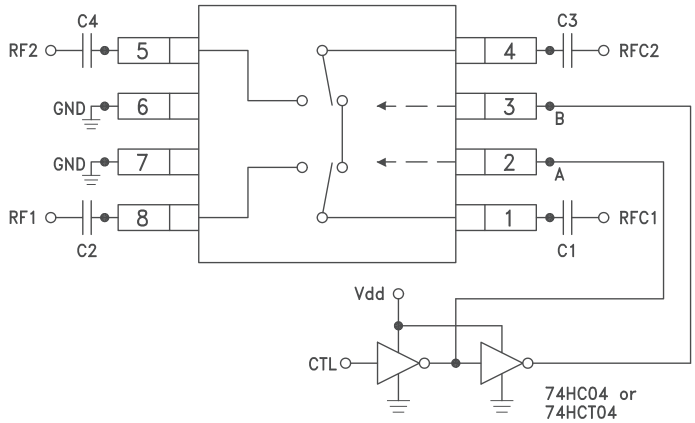
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC199AMS8	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H199A XXXX
HMC199AMS8E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H199A XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

DUAL SPDT SWITCH DC - 2.5 GHz

Typical Application Circuit



Notes:

1. Set A/B control to 0/+5V, Vdd = +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd = 5 to 7 Volts applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Vdd = +7V and A/B set to 0/+7V.

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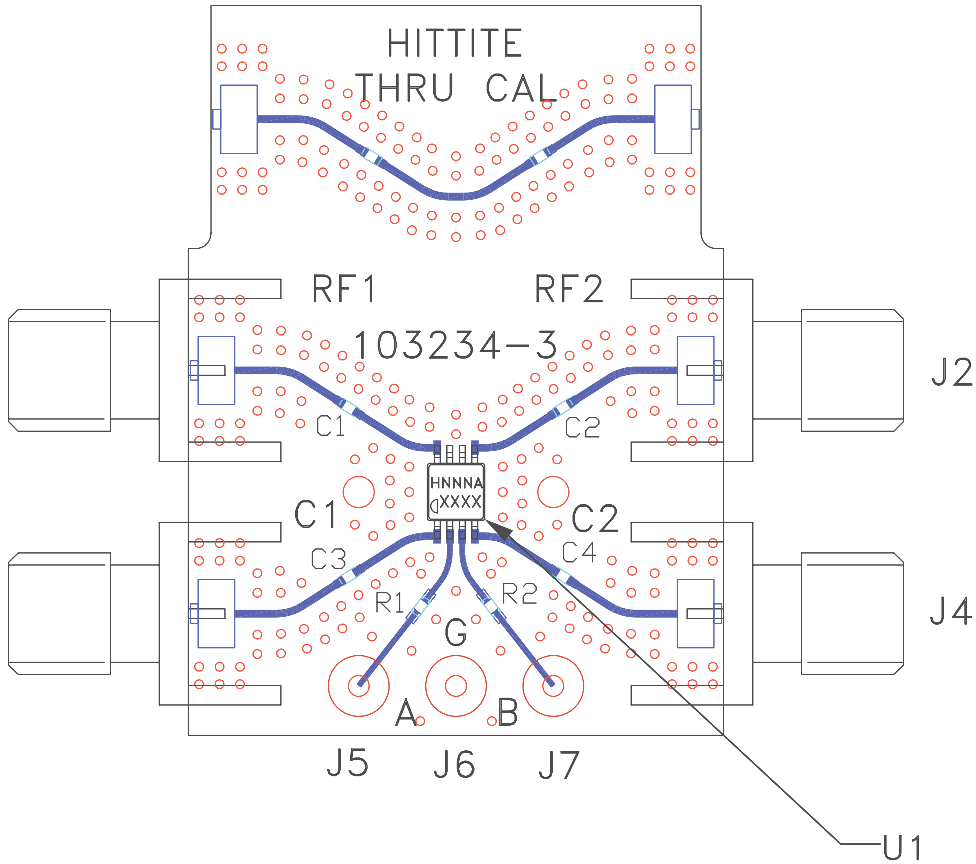
Application Support: Phone: 978-250-3343 or apps@hittite.com

Evaluation PCB



List of Materials for Evaluation PCB EV1HMC199AMS8 [1]

Item	Description
J1 - J4	PCB Mount SMA RF Connector
J5 - J7	DC Pin
C1 - C4	Chip Capacitor, 0402 Pkg. Choose value for lowest frequency of operation. 330 pF is provided on PCB.
R1 - R2	100 Ohm Resistor, 0402 Pkg.
U1	HMC199AMS8 / 199AMS8E Bypass Switch
PCB [2]	103234 Evaluation PCB 1.5” x 1.5”

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF ports should have 50 ohm impedance. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

**R1 & R2 = 100 Ohm.*
These optional resistors will provide more RF path to control circuit isolation.

20 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 10 GHz

Typical Applications

The HMC802LP3E is ideal for both RF and IF applications:

- Test Equipment and Sensors
- ISM, MMDS, WLAN, WiMAX, WiBro
- Microwave Radio & VSAT
- Cellular Infrastructure

Features

± 0.6 dB Typical Step Error

Low Insertion Loss: 3 dB

High IP3: +55 dBm

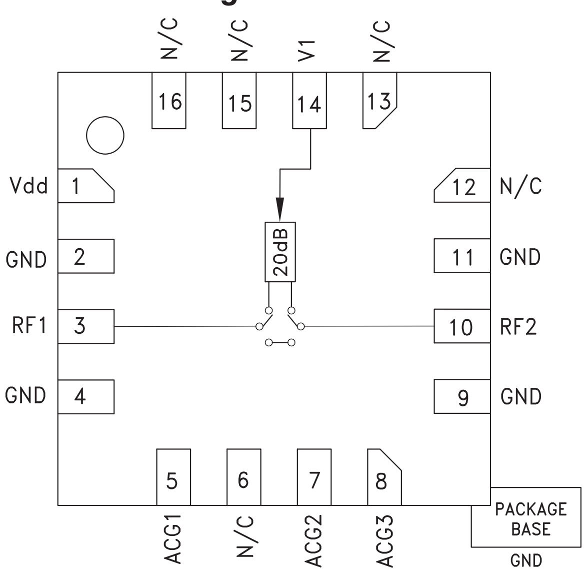
Single Control Line

TTL/CMOS Compatible Control

Single +5V Supply

16 Lead 3x3mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC802LP3E is a broadband bidirectional 1-bit GaAs IC digital attenuator in a low cost leadless surface mount package. This single positive control line digital attenuator utilizes off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 10 GHz, the insertion loss is less than 3 dB typical and attenuation accuracy is excellent at ±0.6 dB typical. The attenuator also features a high IIP3 of +55 dBm. One TTL/CMOS control input is used to select the attenuation state and a single Vdd bias of +5V is required.

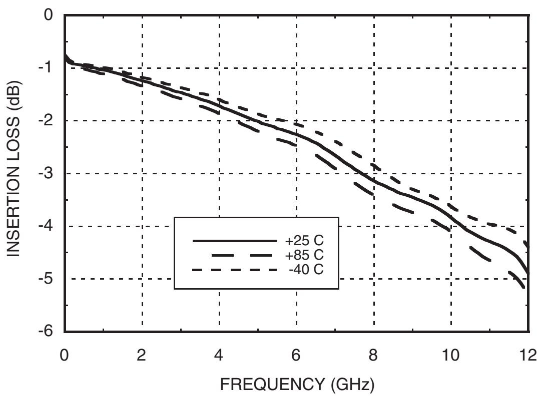
Electrical Specifications, T_A = +25° C, With Vdd = +5V & Vctl = 0/+5V

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 4 GHz 4 - 8 GHz 8 - 10 GHz		1.5 3.0 3.5	2.5 4.0 4.5	dB dB dB
Attenuation Range	DC - 10 GHz		20		dB
Return Loss (RF1 & RF2, Both States)	DC - 6 GHz 6 - 10 GHz		18 12		dB dB
Attenuation Accuracy: (Referenced to Insertion Loss)	DC - 8 GHz 8 - 10 GHz		± 0.4 ± 0.8	± 0.6 ± 1.2	dB dB
Input Power for 0.1 dB Compression	DC - 0.4 GHz 0.4 - 10 GHz		20 30*		dBm dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	DC - 0.4 GHz 0.4 - 10 GHz		45 55		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 10 GHz		120 150		ns ns

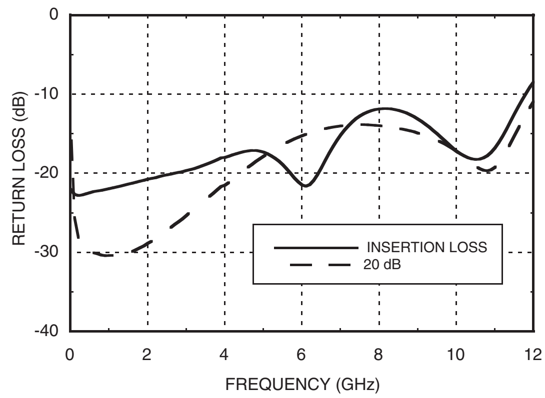
* For frequencies greater than 0.4 GHz, the 0.1 dB compression point is greater than the absolute maximum RF input power of 30 dBm.

20 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 10 GHz

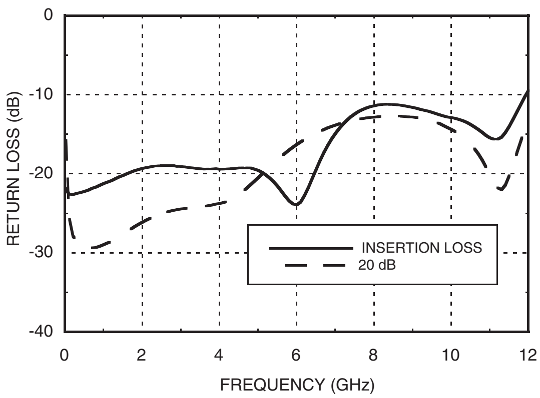
Insertion Loss



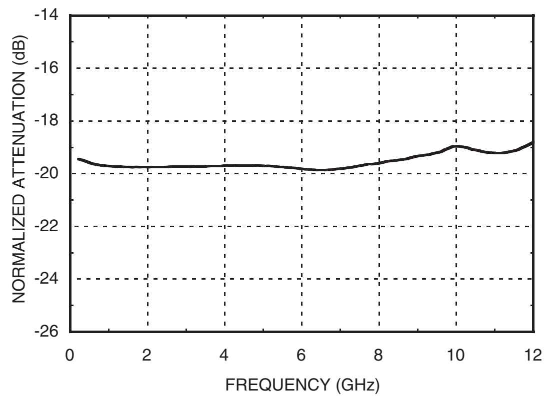
Input Return Loss



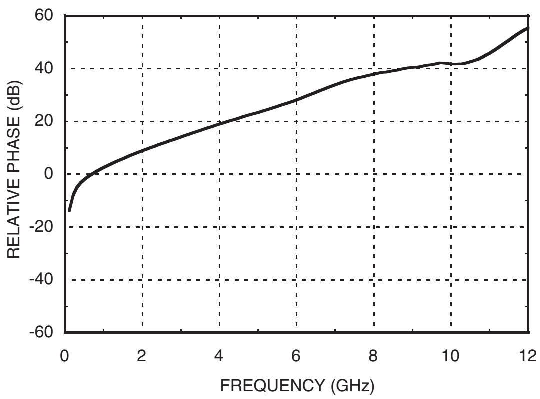
Output Return Loss



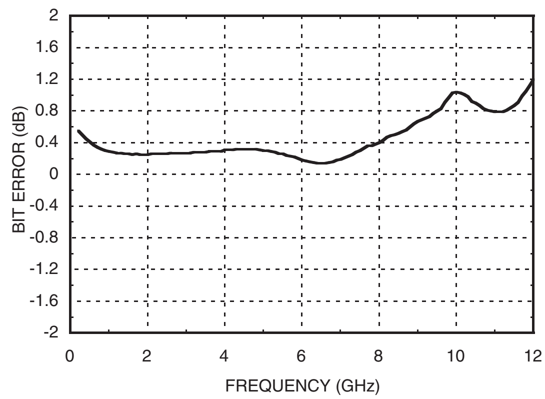
Relative Attenuation



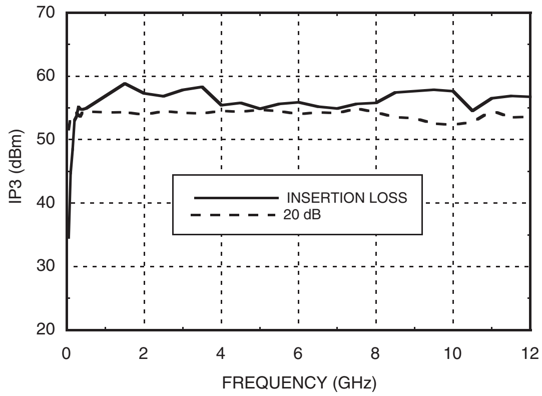
Relative Phase vs. Frequency



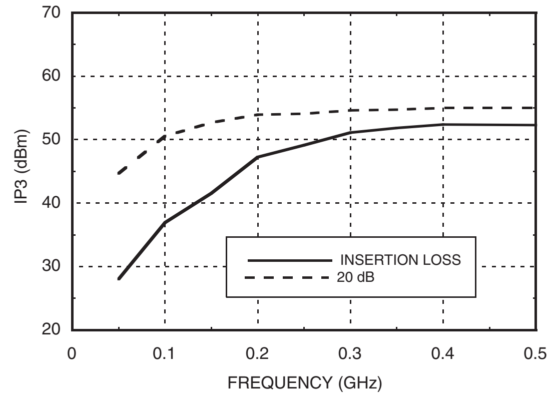
Bit Error vs. Frequency



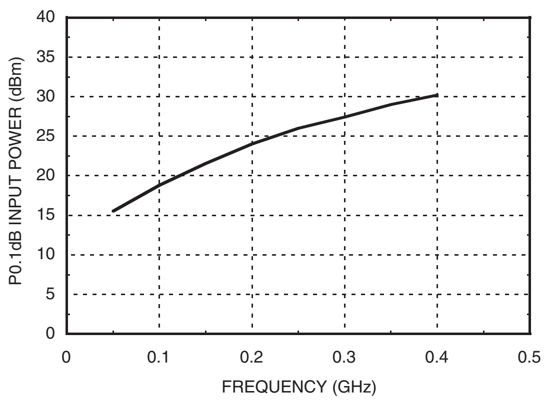
Input IP3 vs. Frequency



Input IP3 vs. Frequency
(Low Frequency Detail)



Input Power for 0.1 dB Compression*
(Low Frequency Detail)



Truth Table

Control Voltage Input	Attenuation State RF1 - RF2
V1	
High	Reference Insertion Loss
Low	20 dB

Bias Voltage & Current

Vdd = +5 Vdc ± 10%	
Vdd (Vdc)	Idd (Typ.) (mA)
4.5	0.21
5.0	0.23
5.5	0.25

Control Voltage

State	Bias Condition
Low	0 to +0.8V @ -1 µA Typ.
High	+2 to +5V @ 30 µA Typ.
Note: Vdd = +5V	

* For frequencies greater than 0.4 GHz, the 0.1 dB compression point is greater than the absolute maximum RF input power of 30 dBm.

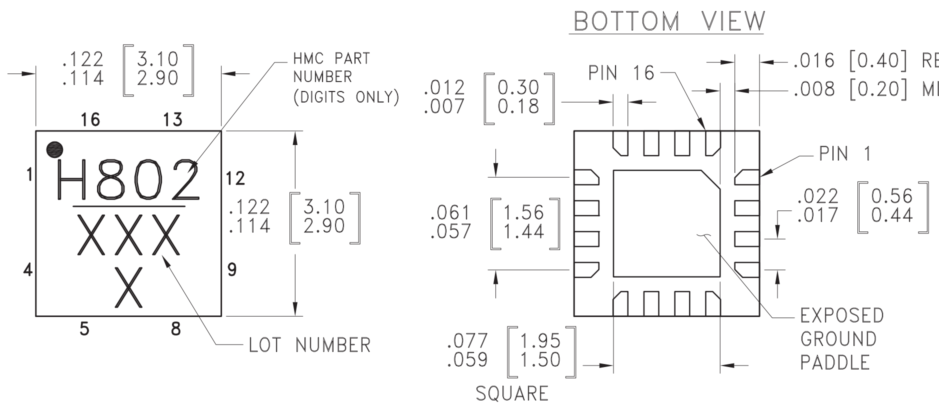
20 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 10 GHz

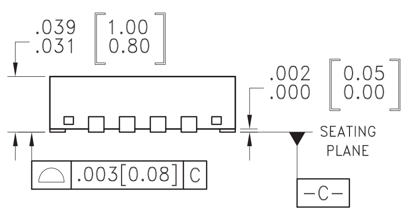
Absolute Maximum Ratings

RF Input Power (DC - 10 GHz)	+30 dBm
Control Voltage Range (V1)	-1 to Vdd + 1V
Bias Voltage (Vdd)	+7 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 12 mW/°C above 85 °C)	0.783 W
Thermal Resistance (channel to ground paddle)	83 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing





NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC802LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H802 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Hittite
MICROWAVE CORPORATION

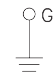
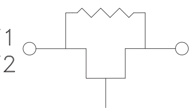
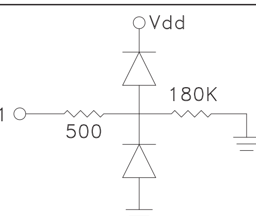
v00.0110

RoHS ✓ EARTH FRIENDLY

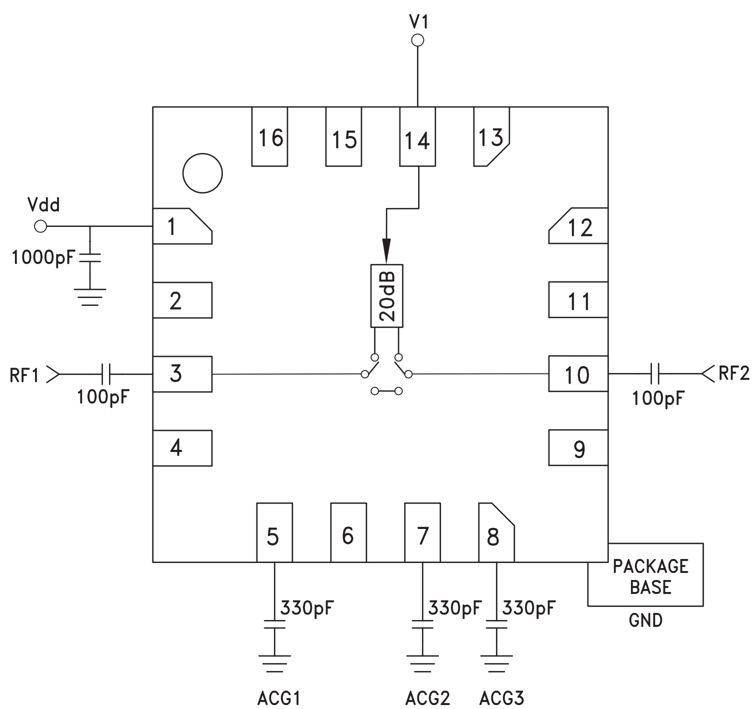
HMC802LP3E

20 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 10 GHz

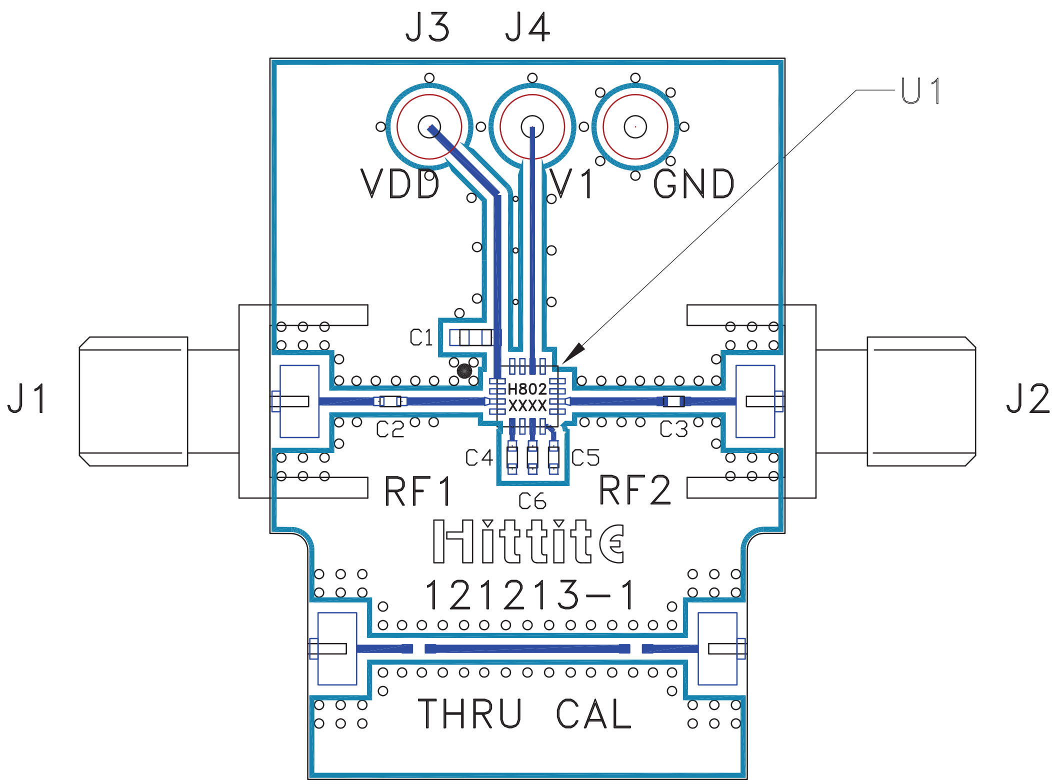
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2, 4, 9, 11	GND	These pins and the exposed ground paddle must be connected to RF/DC ground.	
3, 10	RF1, RF2	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
5, 7, 8	ACG1, ACG2, ACG3	External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
6, 12, 13, 15, 16	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
14	V1	See truth table and control voltage table.	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 127103 [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3, J4	DC Connector
C1	1000 pF Capacitor, 0603 Pkg.
C2, C3	100 pF Capacitor, 0402 Pkg.
C4 - C6	330 pF Capacitor, 0402 Pkg.
U1	HMC802LP3E Digital Attenuator
PCB [2]	121213 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

MSiP™ *Mini-Circuits System In Package*

Ultra High IP3 Amplifier Module HXG-122+

50Ω 0.5 to 1.2 GHz

Ceramic Package

The Big Deal

- Industry leading High IP3, 47 dBm typ.
- Integrated optimization circuits
- Linearity with low current consumption

☛ *LTE Performance*

Product Overview

The HXG-122+ (RoHS compliant) is an advanced amplifier module combining high dynamic range MMIC technology and optimization circuits to provide industry leading linearity over a focused frequency range. It is packaged in a Mini-Circuits System in Package (MSiP) module (6.4mm x 7.0mm x 2.4mm) using a sealed ceramic cover and having gold over Ni for excellent solderability.

Key Features

Feature	Advantages
Optimized Frequency Range: 500 to 1200 MHz	Covering primary wireless communications bands: LTE, cellular and GSM
Extremely High IP3: 47 dBm typ at 700 MHz versus DC Power Consumption of 146mA	The HXG-122+ offers industry leading IP3 performance relative to device size and power consumption. The combination of the design and E-PHEMT provides enhanced linearity over a broad frequency range as evidence in the IP3. This feature makes this amplifier ideal for use in: • Driver amplifiers for complex waveform up converter paths • Drivers in linearized transmit systems • Secondary amplifiers in ultra High Dynamic range receivers
No External Matching Components Required	Unlike competing products, Mini-Circuits HXG-122+ provides Input and Output Return Loss of 10 dB up to 0.9 GHz without the need for any external matching components
Low Noise Figure: 2.2dB typ.	A unique feature of the HXG-122+ which separates this design from all competitors is the low noise figure performance in combination with the high dynamic range.

MSiP™ *Mini-Circuits System In Package*

Ultra High IP3 Amplifier Module 0.5-1.2GHz

Product Features
- Ultra High IP3, +47 dBm typ.
- Gain, 15.3 dB typ. at 900 MHz
- High Pout, P1dB +23 dBm typ. at 900 MHz
- Low noise figure, 2.2 dB at 900 MHz
- Internally matched for optimized IP3 performance
- No external matching components required

HXG-122+

CASE STYLE: LZ1671
PRICE: $3.41ea. QTY. (50)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

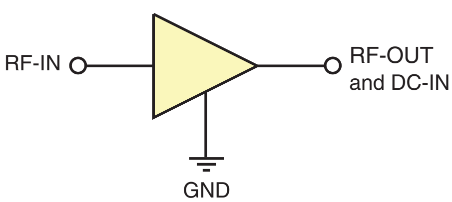
The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

☛ *LTE Performance*

Typical Applications
- LTE
- Base station infrastructure
- Portable Wireless

General Description
The HXG-122+ (RoHS compliant) is an advanced amplifier module in a Mini-Circuits System in Package (MSiP) which includes internal matching networks to offer extremely high dynamic range module. It is housed in a ceramic package 6.4mm x 7.0mm x 2.4mm.

simplified schematic and pin description



Function	Pin Number	Description
RF IN	2	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.
RF-OUT and DC-IN	5	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in "Recommended Application Circuit", Fig. 2
GND	1,3,4,6, Paddle	Connections to ground. Use via holes as shown in "Suggested Layout for PCB Design" to reduce ground path inductance for best performance.

Electrical Specifications[1] at 25°C and 5V, unless noted

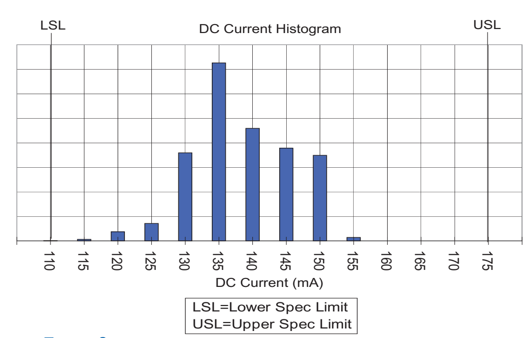
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.5		1.2	GHz
Gain	0.5		16.0		dB
	0.7		15.7		
	0.9	13.9	15.3	17.0	
	1.2		14.5		
Input Return Loss	0.5		18.7		dB
	0.7		15.9		
	0.9		13.2		
	1.2		9.4		
Output Return Loss	0.5		14.2		dB
	0.7		12.1		
	0.9		10.3		
	1.2		8.0		
Reverse Isolation	0.9		21.0		dB
Output Power @1 dB compression	0.5		22.9		dBm
	0.7		23.0		
	0.9		23.3		
	1.2		23.0		
Output IP3	0.5		43.8		dBm
	0.7		47.0		
	0.9		46.0		
	1.2		40.8		
Noise Figure	0.5		2.1		dB
	0.7		2.2		
	0.9		2.2		
	1.2		2.2		
Device Operating Voltage (V_d)		4.8	5.0	5.2	V
Device Operating Current		110	146	180	mA
Device Current Variation vs. Temperature[2]			+14		µA/°C
Device Current Variation vs Voltage			0.05		mA/mV
Thermal Resistance, junction-to-ground lead			85		°C/W

(1) Measured on Mini-Circuits Characterization test board TB-641-1+. See Characterization Test Circuit (Fig. 1)
(2) Current at 85°C — Current at -45°C)/130

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Operating Current at 5V	210 mA
Power Dissipation	1 W
Input Power (CW)	24 dBm
DC Voltage on Pin 3	6 V

Note:
Permanent damage may occur if any of these limits are exceeded.
Electrical maximum ratings are not intended for continuous normal operation.



Characterization Test Circuit

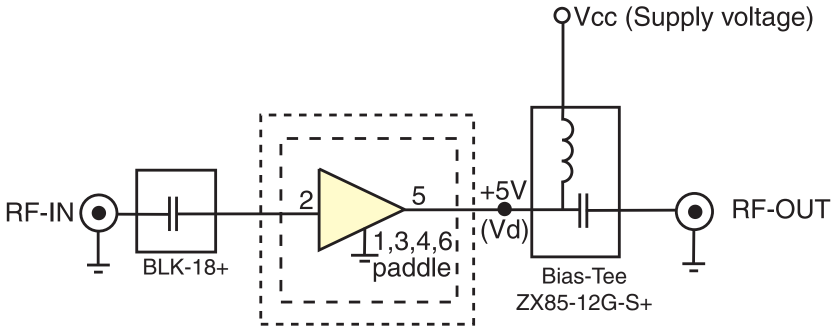


Fig 1. Block Diagram of Test Circuit used for characterization. (DUT soldered on Mini-Circuits Characterization test board TB-641-1+) Gain, Return loss, Output power at 1dB compression (P1 dB) , output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.

Recommended Application Circuit

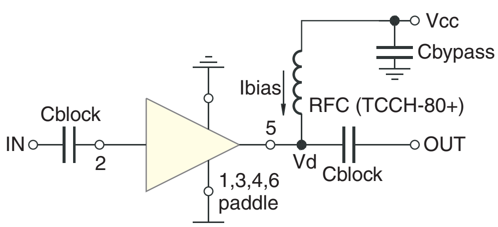
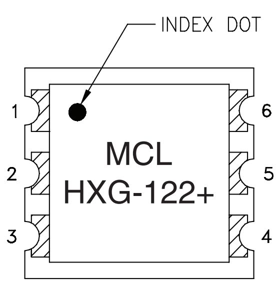


Fig 2. Test Board includes case, connectors, and components soldered to PCB

Product Marking



Markings in addition to model number designation may appear for internal quality control purposes.

Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	LZ1671 *Ceramic package, exposed paddle, lead finish: gold plating over nickel*
Tape & Reel **Standard quantities available on reel**	F78 *7" reels with 20, 50, 100, 200 and 13" with 500, or 1K devices.*
Suggested Layout for PCB Design	PL-350
Evaluation Board	TB-641-1+
Environmental Ratings	ENV-59

ESD Rating

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1-2001

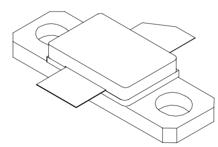
Machine Model (MM): Class M1 (<100V) in accordance with ANSI/ESD STM 5.2-1999 passes 25V

LET9045C

RF power transistor from the LdmoST family of n-channel enhancement-mode lateral MOSFETs

Features

- Excellent thermal stability
- Common source configuration
- P_{OUT} (@28 V) = 45 W with 18.5 dB gain @ 960 MHz
- P_{OUT} (@36V) = 70 W with 18.5 dB gain @ 960 MHz
- BeO free package
- In compliance with the 2002/95/EC European directive



M243
epoxy sealed

Description

The LET9045C is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The LET9045C is designed for high gain and broadband performance operating in common source mode at 28 V. It is ideal for base station applications requiring high linearity.

Figure 1. Pin out

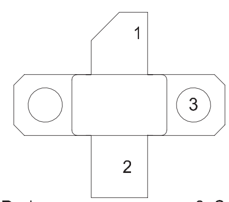


Table 1. Device summary

Order code	Package	Branding
LET9045C	M243	LET9045C

1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	-0.5 to +15	V
I_D	Drain current	9	A
P_{DISS}	Power dissipation (@ T_C = 70 °C)	108	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Junction-case thermal resistance	1.2	°C/W

2 Electrical characteristics

T_C = 25 °C

Table 4. Static

Symbol	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V; I_{DS} = 10 mA	80			V
I_{DSS}	V_{GS} = 0 V; V_{DS} = 28 V			1	µA
I_{GSS}	V_{GS} = 20 V; V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	V_{DS} = 28 V; I_D = 300 mA	2.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V; I_D = 3 A		0.9	1.2	V
G_{FS}	V_{DS} = 10 V; I_D = 3 A	2.5			mho
C_{ISS}	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz		58		pF
C_{OSS}	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz		29		pF
C_{RSS}	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz		0.8		pF

Table 5. Dynamic

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	V_{DD} = 28 V; I_{DQ} = 300 mA; P_{IN} = 1 W; f = 960 MHz	45	59		W
G_{PS}	V_{DD} = 28 V; I_{DQ} = 300 mA; P_{IN} = 1 W; f = 960 MHz	16.5	17.7		dB
h_D	V_{DD} = 28 V; I_{DQ} = 300 mA; P_{IN} = 1 W; f = 960 MHz	60	65		%
Load mismatch	V_{DD} = 28 V; I_{DQ} = 300 mA; P_{IN} = 1 W; f = 960 MHz All phase angles	10:1			VSWR

3 Impedance data

Figure 2. Impedance data

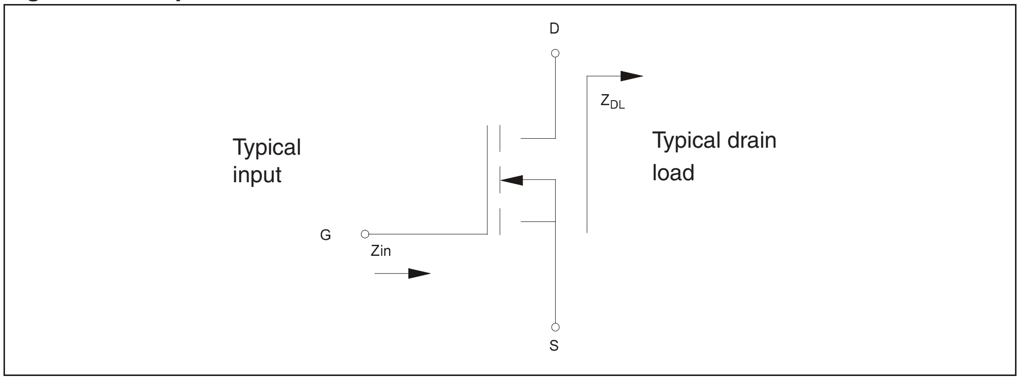


Table 6. Impedance data

Frequency	Z_{IN} (Ω)	Z_{DL} (Ω)
920	0.8 - j 0.08	5.3 + j 0.63
945	0.7 - j 0.4	5 + j 1.5
960	0.6 - j 0.6	4.7 + j 2

4 Typical performances

Figure 3. Gain vs output power and bias current, freq = 960 MHz, Vdd = 28 V

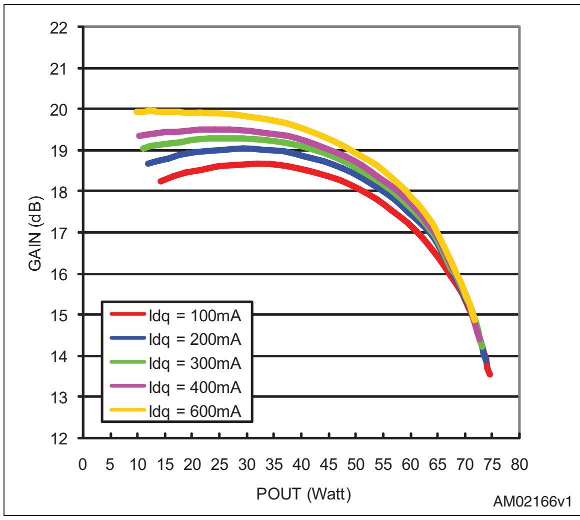


Figure 4. Gain and efficiency vs output power, freq = 960 MHz, Vdd = 28 V, Idq = 300 mA

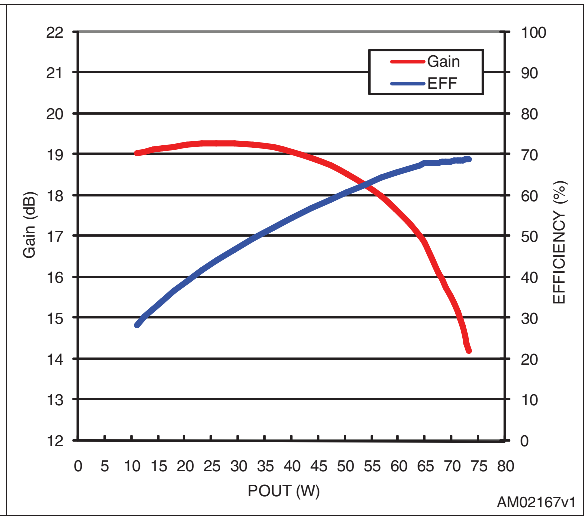
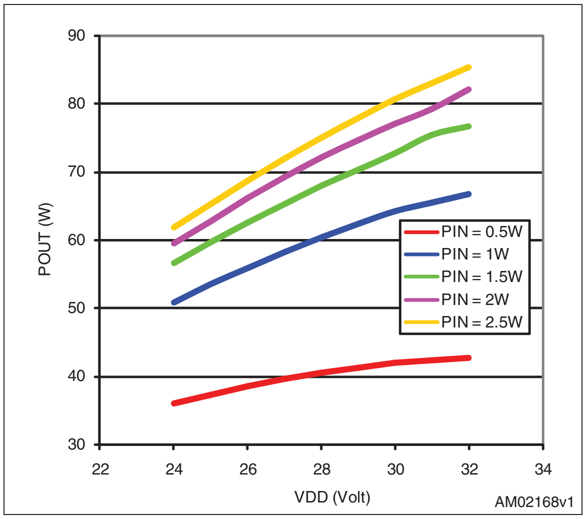


Table 7. Output power vs supply voltage freq = 960 MHz, Vdd = 28 V, Idq = 300 mA



5 Test circuit

Figure 5. Test circuit

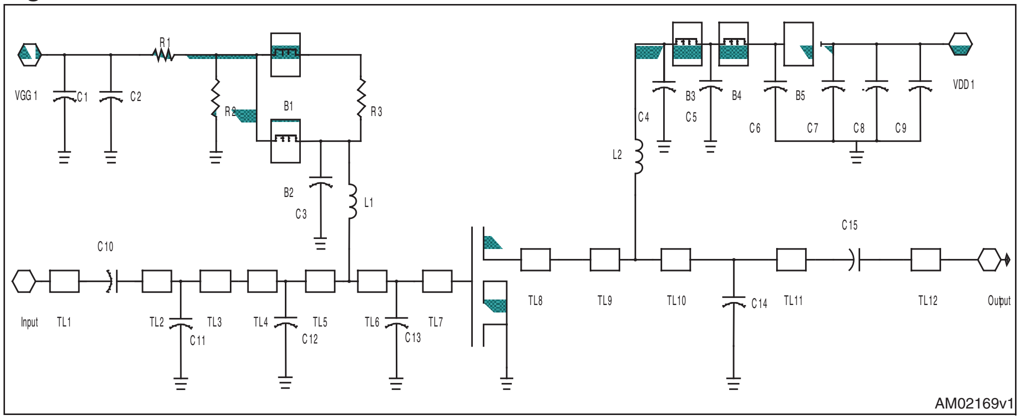


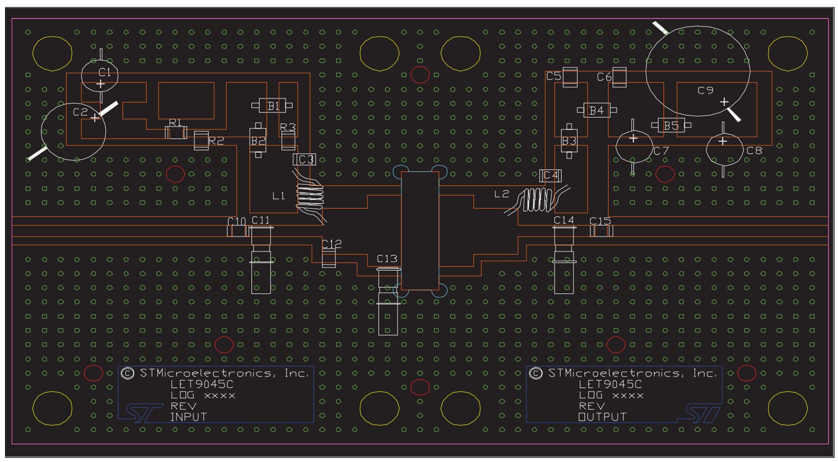
Table 8. LET9045C components list

Item	Qty	Part number	Vendor	Description
R1, R2	2	CR1206-8W-112JB	VENKEL	1.1 kΩ 1/8W surface mount chip resistor
R3	1	CR1206-8W-100JB	VENKEL	10 Ω 1/8W surface mount chip resistor
Coil	2		BELDEN	Inductor 5 turns air WOUND#20AWG ID =0.130 in (3.3 mm) bylon coated
B1,B2,B3,B4,B5	5	2743021447	FAIR-RITE CORP	Surface mount EMI sheild bead
C1,C7, C8	3	T491D106K035AT	Kemet	10 µF 35 V tantalum capacitors
C2	1			100 µF 63 V electrolytic capacitor
C3, C4, C10, C15	4	ATC100B470XXXX	ATC	47 pF chip capacitor
C5, C6	2	ATC200B393MW	ATC	39000 pF chip capacitor
C9	1			330 uF 50 V electrolytic capacitor
C11, C13, C14	3	27291PC	Johanson	0.8-8 pF giga trim variable capacitor
C12	1	ATC100B110XXXX	ATC	11 pF chip capacitor
TL1				L = 1.350in [34.29 mm] W = 0.082in [02.08 mm]
TL2				L = 0.144in [3.65 mm] W = 0.082in [02.08 mm]
TL3				L = 0.311in [7.91 mm] W = 0.082in [02.08 mm]
TL4				L = 00.82in [2.09 mm] W = 0.323in [08.21 mm]
TL5				L = 0.194 in [4.94 mm] W = 0.323in [08.21 mm]

Table 8. LET9045C components list (continued)

Item	Qty	Part number	Vendor	Description
TL6				L = 0.059in [1.49 mm] W= 0.506in [12.85 mm]
TL7				L = 0.144in [3.65 mm] W = 0.506in [12.85 mm]
TL8				L = 0.208in [5.28 mm] W = 0.506in [12.85 mm]
TL9				L = 0.275in [6.98 mm] W = 0.323in [08.21 mm]
TL10				L = 0.210in [5.33 mm] W = 0.082in [02.08 mm]
TL11				L = 0.260in [6.60 mm] W = 0.082in [02.08 mm]
TL12				L = 1.350in [34.29 mm] W = 0.082in [02.08 mm]
Board 3X5	1		Rogers corp	Er=2.55 t=0.0026in h=0.030in

Figure 6. Circuit layout



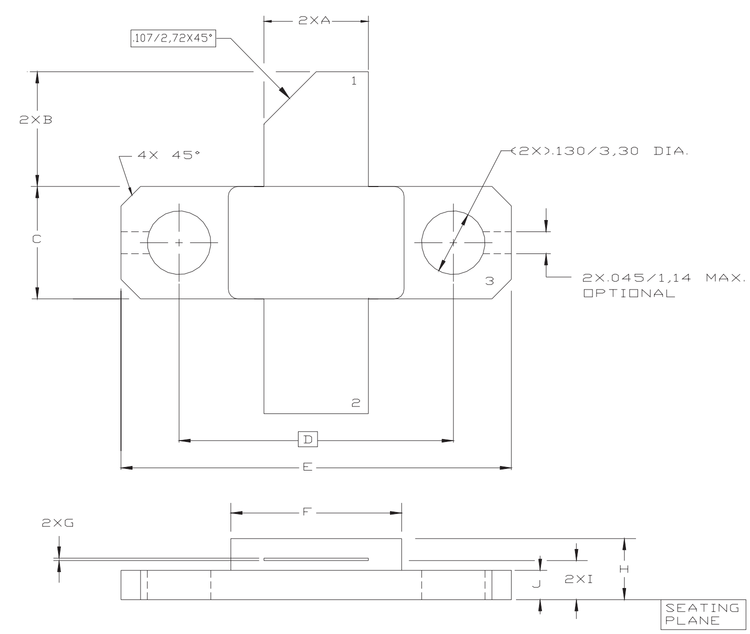
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. M243 (.230 x .360 2L N/HERM W/FLG) mechanical data

Dim.	mm			inch		
	Min.	Typ	Max.	Min.	Typ	Max.
A	5.21		5.72	0.205		0.225
B	5.46		6.48	0.215		0.255
C	5.59		6.1	0.22		0.24
D		14.27			0.562	
E	20.07		20.57	0.79		0.81
F	8.89		9.4	0.35		0.37
G	0.1		0.15	0.004		0.006
H	3.18		4.45	0.125		0.175
I	1.83		2.24	0.072		0.088
J	1.27		1.78	0.05		0.07

Figure 7. M243 package dimensions



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Mar-2009	1	Initial release.
02-Nov-2009	2	Udated *Figure 4*.
11-Feb-2010	3	Changed test condition for $V_{(BR)DSS}$ in *Table 4: Static*.
15-Apr-2011	4	Updated features in cover page.

MGA-30689

40MHz - 3000MHz

Flat Gain High Linearity Gain Block

Data Sheet

Description

Avago Technologies' MGA-30689 is a flat gain, high linearity, low noise, 22dBm Gain Block with good OIP3 achieved through the use of Avago Technologies' proprietary 0.25um GaAs Enhancement-mode pHEMT process.

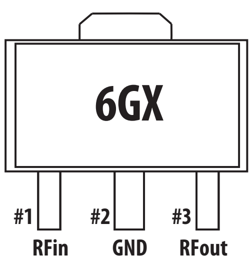
The device required simple dc biasing components to achieve wide bandwidth performance. The temperature compensated internal bias circuit provides stable current over temperature and process threshold voltage variation.

The MGA-30689 is housed inside a standard SOT89 package (4.5 x 4.1 x 1.5 mm).

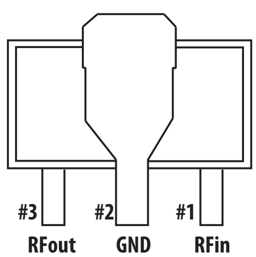
Applications

- IF amplifier, RF driver amplifier
- General purpose gain block

Component Image



Top View



Bottom View

Notes:
Package marking provides orientation and identification
"6G" = Device Code
"X" = Month of manufacture

Features

- Flat Gain 14dB +/-0.5dB, 40MHz to 2600MHz
- High linearity
- Built in temperature compensated internal bias circuitry
- No RF matching components required
- GaAs E-pHEMT Technology[1]
- Standard SOT89 package
- Single, Fixed 5V supply
- Excellent uniformity in product specifications
- MSL-2 and Lead-free halogen free
- High MTTF for base station application

Specifications

- 900MHz; 5V, 104mA (typical)
  - 14.3 dB Gain
  - 43 dBm Output IP3
  - 3.0 dB Noise Figure
  - 22.3 dBm Output Power at 1dB gain compression
- 1950MHz, 5V, 104mA (typical)
  - 14.6 dB Gain
  - 40 dBm Output IP3
  - 3.3 dB Noise Figure
  - 22.5 dBm Output Power at 1dB gain compression

Note:
1. Enhancement mode technology employs positive gate voltage, thereby eliminating the need of negative gate voltage associated with conventional depletion mode devices.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 75 V
ESD Human Body Model = 450 V
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Absolute Maximum Rating [2] T_A=25°C

Symbol	Parameter	Units	Absolute Max.
$V_{dd,max}$	Device Voltage, RF output to ground	V	5.5
$P_{in,max}$	CW RF Input Power	dBm	20
P_{diss}	Total Power Dissipation [4]	W	0.75
$T_{j, max}$	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance [3] θ_{jc} = 53.5°C/W (Vdd = 5V, Ids = 100mA, Tc = 85°C)

Notes:
2. Operation of this device in excess of any of these limits may cause permanent damage.
3. Thermal resistance measured using Infrared measurement technique.
4. This is limited by maximum Vdd and Ids. Derate 18.7 mW/°C for Tc>110°C.

Product Consistency Distribution Charts[5, 6]

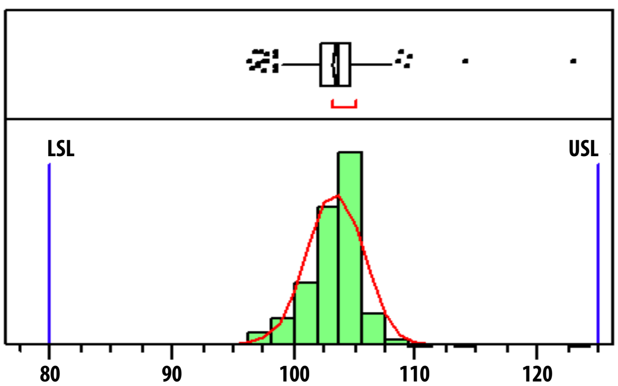


Figure 1. Ids, LSL=80mA , nominal=104mA, USL=125mA

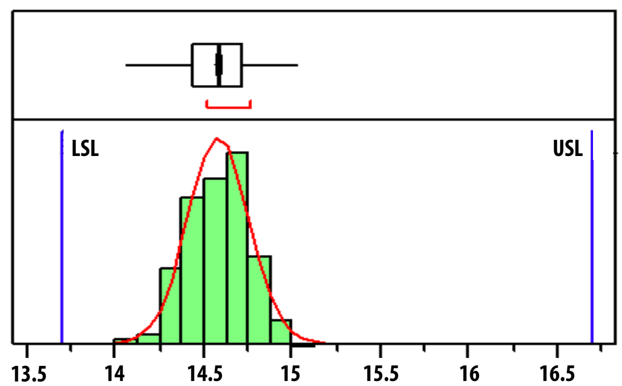


Figure 2. Gain, LSL=13.7dB, nominal=14.6dB, USL=16.7dB

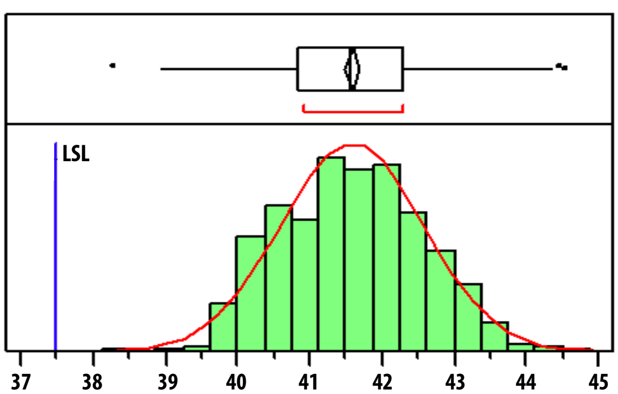


Figure 3. OIP3, LSL=37.5dBm, nominal=41.5dBm

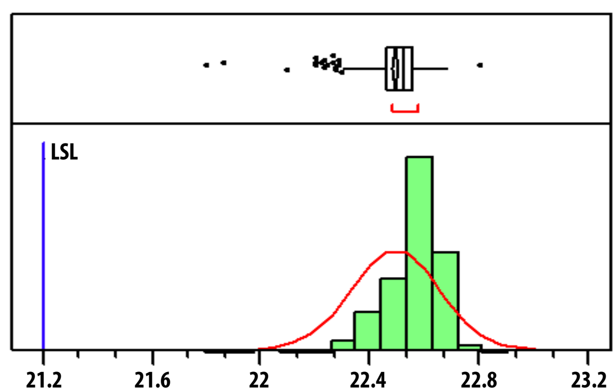


Figure 4. P1dB, LSL=21.2dBm, nominal=22.5dBm

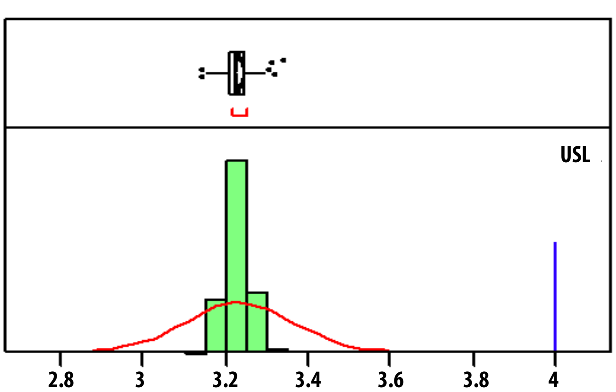


Figure 5. NF, nominal=3.23dB, USL=4dB

Notes:
5. Distribution data sample size is 500 samples taken from 3 different wafer lots and 6 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements were made on a characterization test board, which represents a trade-off between optimal OIP3, gain and P1dB. Circuit trace losses have not been de-embedded from measurements above.

Electrical Specifications [7]

T_A = 25°C, Vdd =5V

Symbol	Parameter and Test Condition	Frequency	Units	Min.	Typ.	Max.
Ids	Quiescent current	N/A	mA	80	104	125
Gain	Gain	40MHz 900MHz 1950MHz	dB	 13.7	14.8 14.3 14.6	 16.7
OIP3 [8]	Output Third Order Intercept Point	40MHz 900MHz 1950MHz	dBm	 37.5	40 43 40	 –
NF	Noise Figure	40MHz 900MHz 1950MHz	dB	 –	2.9 3.0 3.3	 4
S11	Input Return Loss, 50Ω source	40MHz 900MHz 1950MHz	dB		-13 -12 -15	
S22	Output Return Loss, 50Ω load	40MHz 900MHz 1950MHz	dB		-18 -15 -12	
S12	Reverse Isolation	40MHz 900MHz 1950MHz	dB		-20 -22 -25	
OP1dB	Output Power at 1dB Gain Compression	40MHz 900MHz 1950MHz	dBm	 21.2	21.8 22.4 22.5	 –

Notes:

7. Measurements obtained using demo board described in Figure 30 and 31. 40MHz data was taken with 40MHz – 2GHz Application Test Circuit, 900MHz data with 0.2GHz – 3GHz Application Test Circuit and 1.95GHz data with 1.5GHz – 2.6GHz Application Test Circuit respectively.
8. OIP3 test condition: $F_{RF1} - F_{RF2}$ = 10MHz with input power of -15dBm per tone measured at worse side band.
9. Use proper bias, heat sink and de-rating to ensure maximum channel temperature is not exceeded. See absolute maximum ratings and application note (if applicable) for more details.

Typical Performance (40MHz – 2GHz)

TA = +25°C, Vdd = 5V, Input Signal = CW. Application Test Circuit is shown in Figure 30 and Table 1.

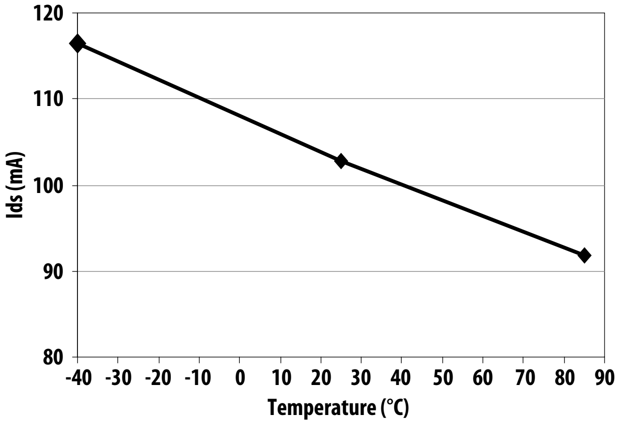


Figure 6. Ids over Temperature

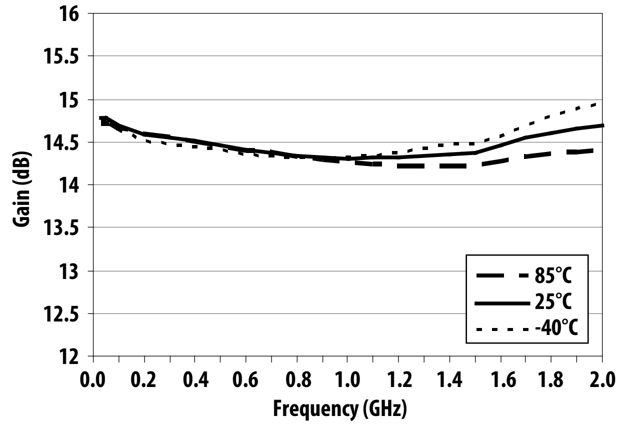


Figure 7. Gain over Frequency and Temperature

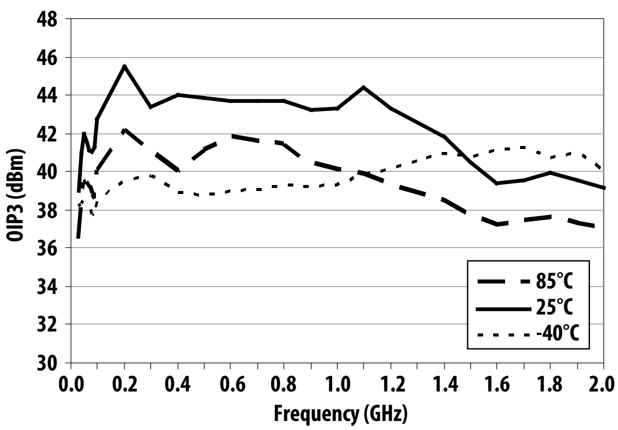


Figure 8. OIP3 over Frequency and Temperature

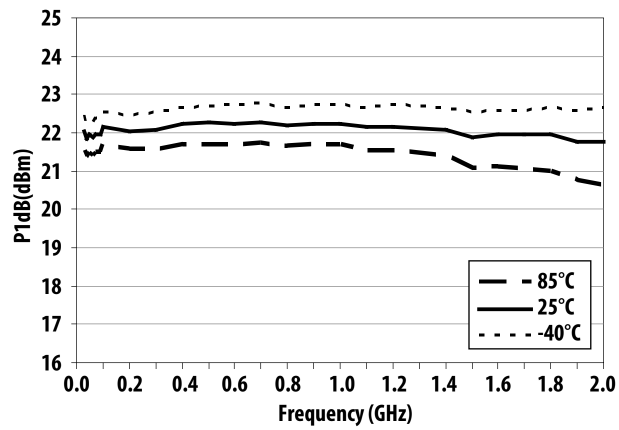


Figure 9. P1dB over Frequency and Temperature

Typical Performance (40MHz – 2GHz)

TA = +25°C, Vdd = 5V, Input Signal = CW. Application Test Circuit is shown in Figure 30 and Table 1.

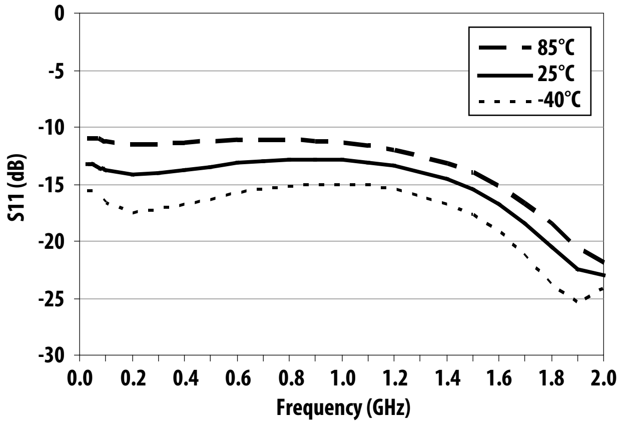


Figure 10. S11 over Frequency and Temperature

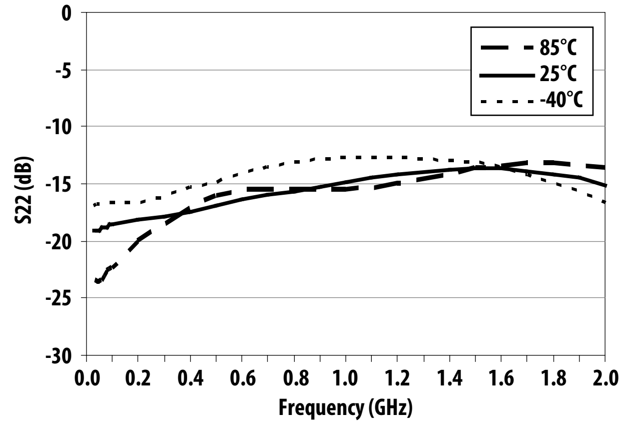


Figure 11. S22 over Frequency and Temperature

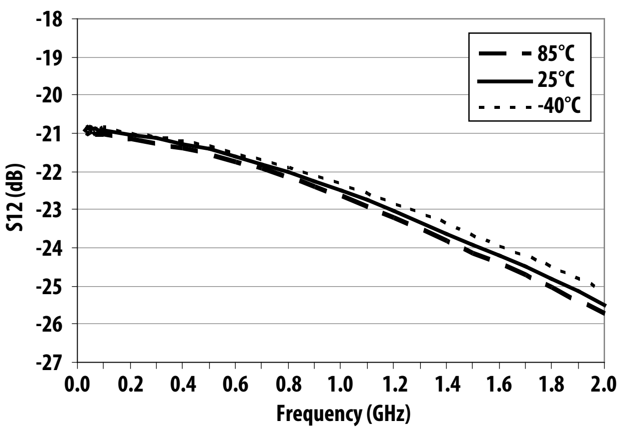


Figure 12. S12 over Frequency and Temperature

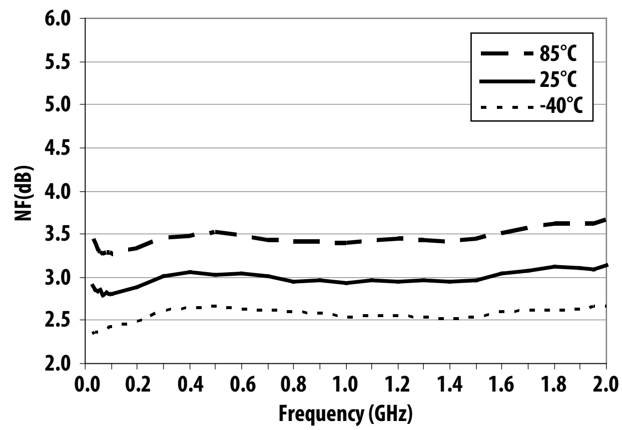


Figure 13. Noise Figure over Frequency and Temperature

Typical Performance (0.2GHz – 3GHz)

TA = +25°C, Vdd = 5V, Input Signal = CW. Application Test Circuit is shown in Figure 30 and Table 2.

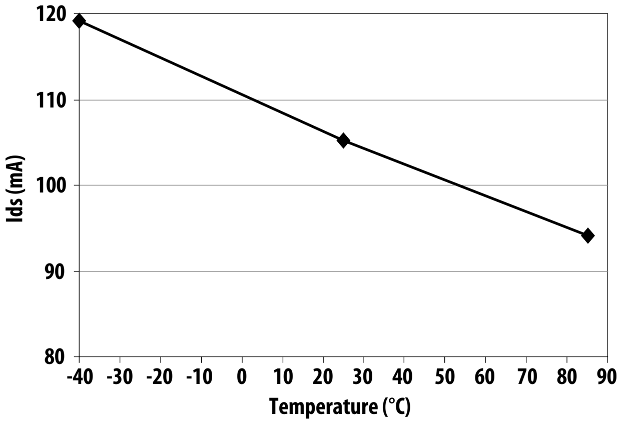


Figure 14. Ids over Temperature

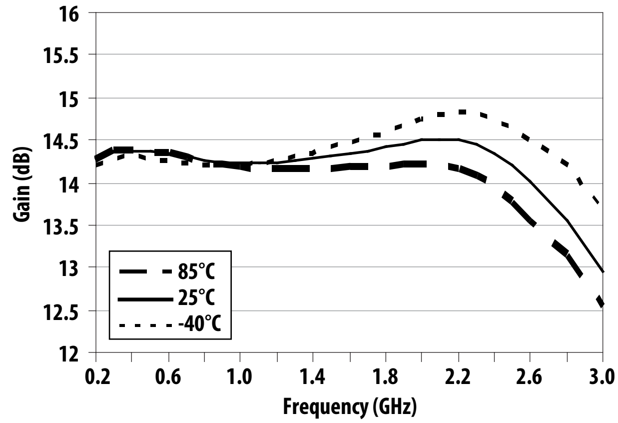


Figure 15. Gain over Frequency and Temperature

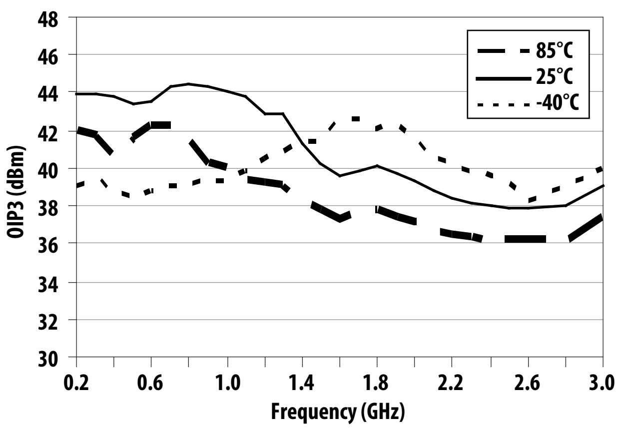


Figure 16. OIP3 over Frequency and Temperature

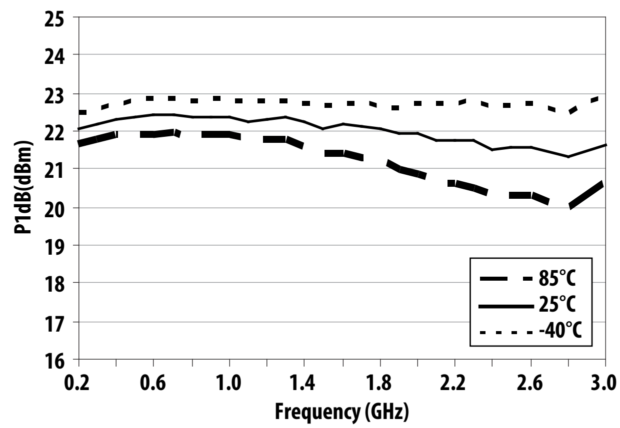


Figure 17. P1dB over Frequency and Temperature

Typical Performance (0.2GHz – 3GHz)

TA = +25°C, Vdd = 5V, Input Signal = CW. Application Test Circuit is shown in Figure 30 and Table 2.

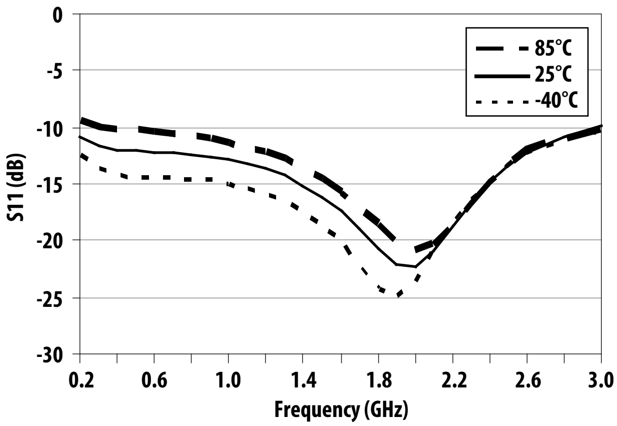


Figure 18. S11 over Frequency and Temperature

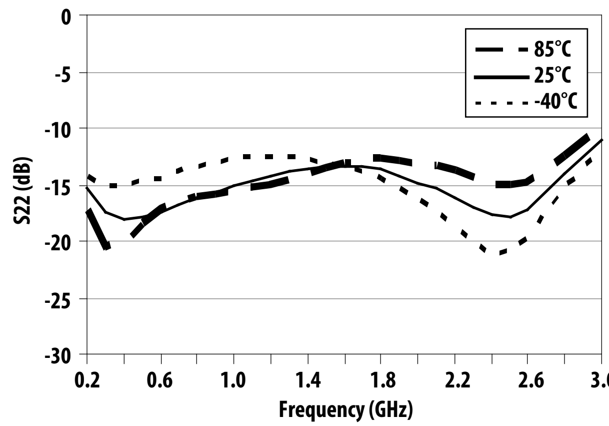


Figure 19. S22 over Frequency and Temperature

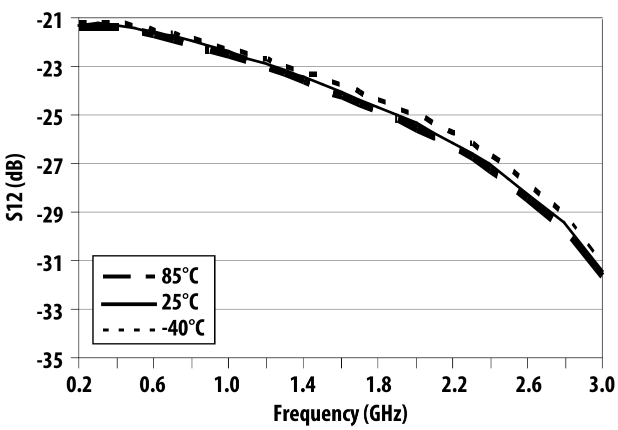


Figure 20. S12 over Frequency and Temperature

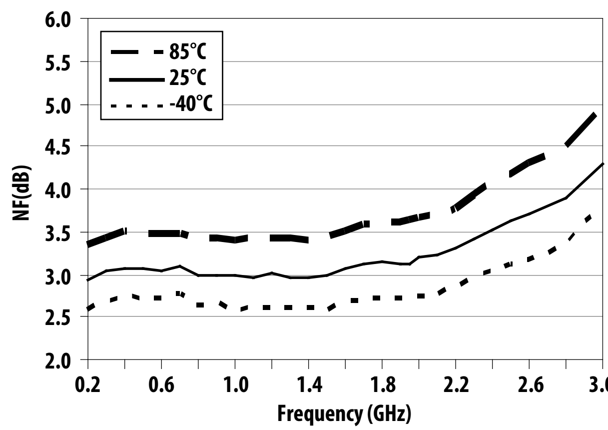


Figure 21. Noise Figure over Frequency and Temperature

Typical Performance (1.5GHz – 2.6GHz)

TA = +25°C, Vdd = 5V, Input Signal = CW. Application Test Circuit is shown in Figure 30 and Table 3.

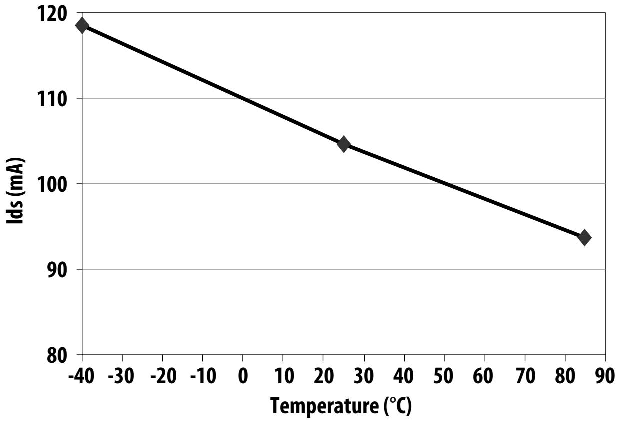


Figure 22. Ids over Temperature

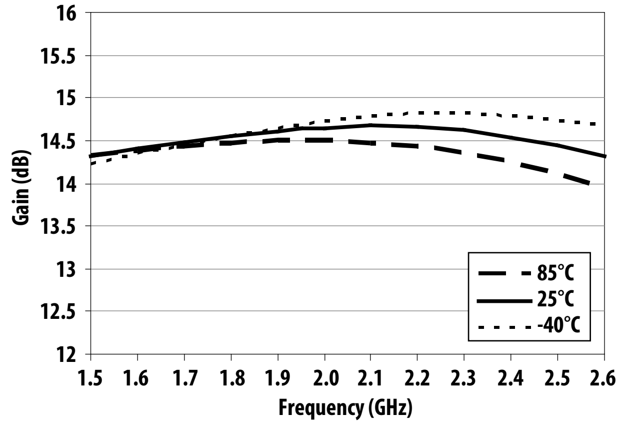


Figure 23. Gain over Frequency and Temperature

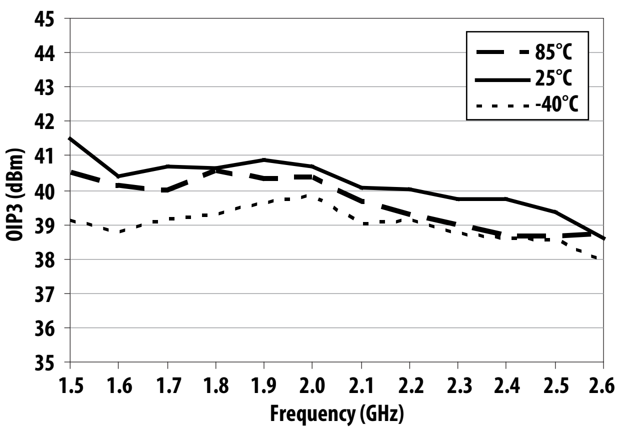


Figure 24. OIP3 over Frequency and Temperature

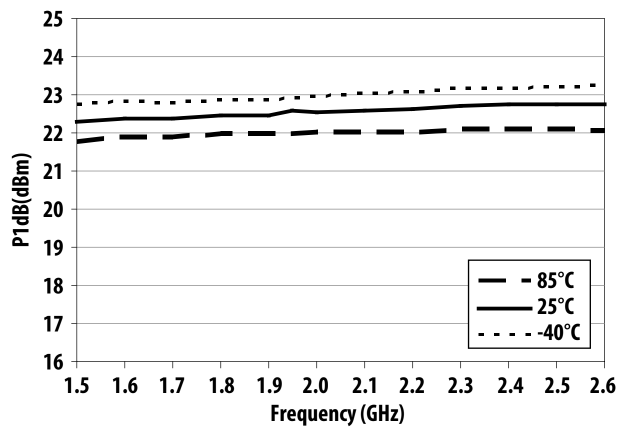


Figure 25. P1dB over Frequency and Temperature

Typical Performance (1.5GHz – 2.6GHz)

TA = +25°C, Vdd = 5V, Input Signal = CW. Application Test Circuit is shown in Figure 30 and Table 3.

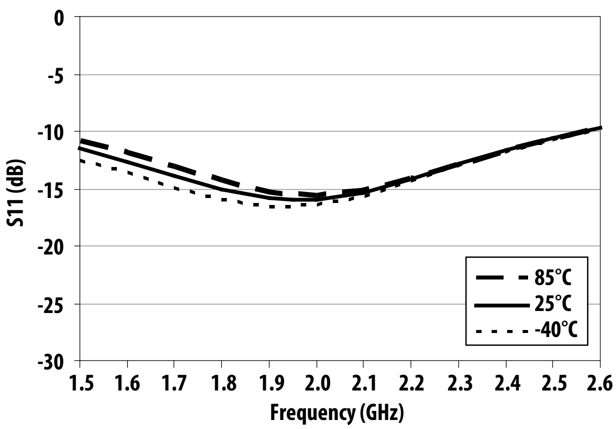


Figure 26. S11 over Frequency and Temperature

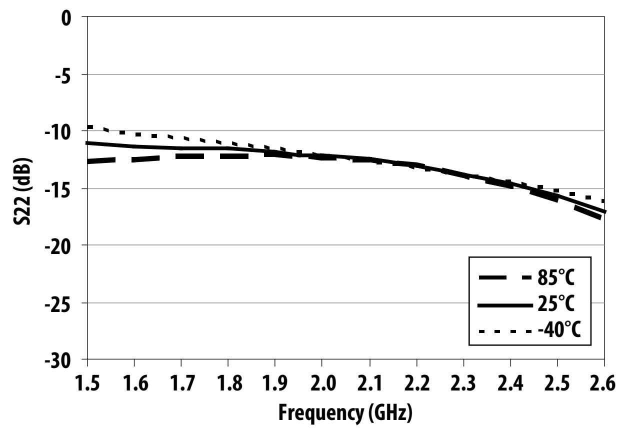


Figure 27. S22 over Frequency and Temperature

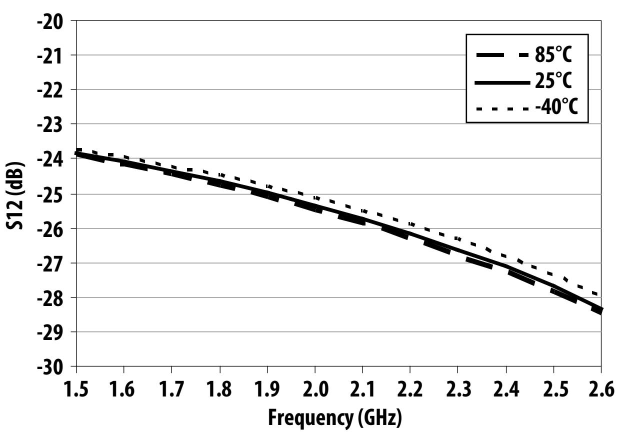


Figure 28. S12 over Frequency and Temperature

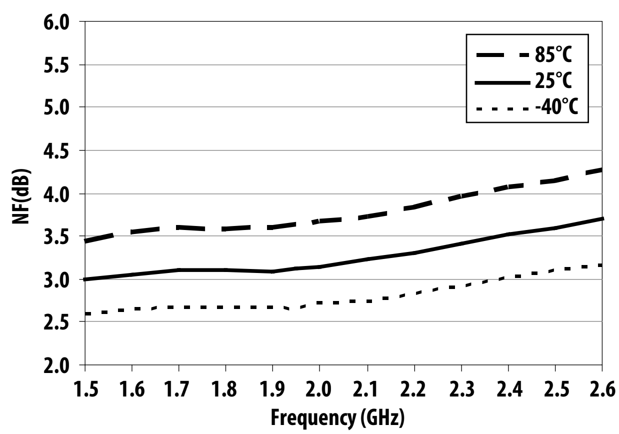


Figure 29. Noise Figure over Frequency and Temperature

Application Schematic Components Table and Demo Board

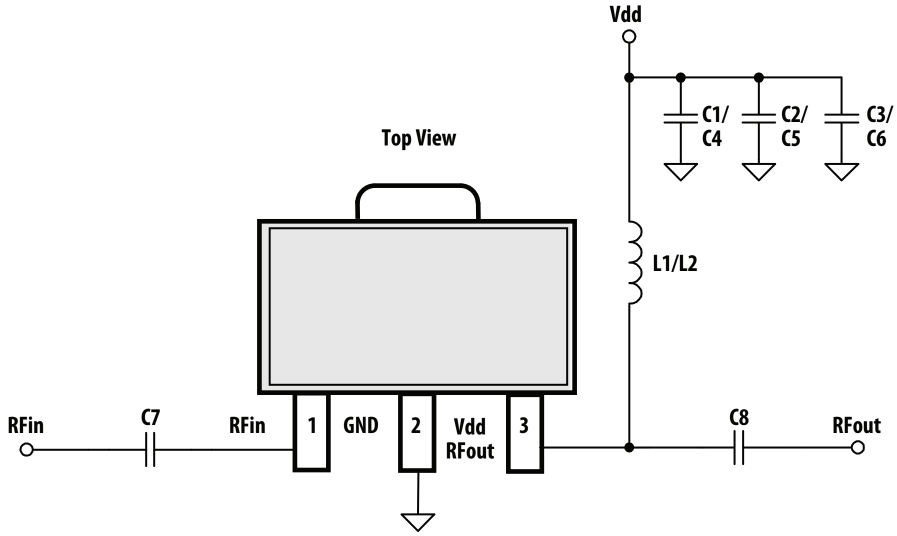
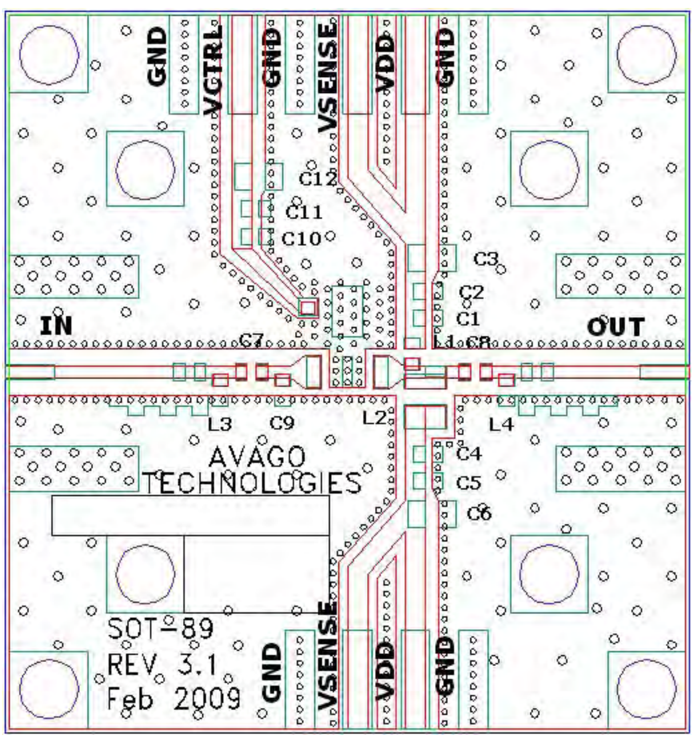


Figure 30. Application Schematic



– Recommended PCB material is 10 mils Rogers RO4350, with FR4 backing for mechanical strength.
– Suggested component values may vary according to layout and PCB material.

Figure 31. Demo board Layout

Demo board Part List

Table 1. 40 MHz – 2 GHz Application Schematic Components

Circuit Symbol	Size	Value	Part Number	Description
L2	0805	820nH	LLQ2012-series (Toko)	Wire Wound Chip Inductor
C4	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor
C5	0402	0.1uF	GRM155R71C104KA88D (Murata)	Ceramic Chip Capacitor
C6	0805	2.2uF	GRM21BR61E225KA12L (Murata)	Ceramic Chip Capacitor
C7	0402	0.1uF	GRM155R71C104KA88D (Murata)	Ceramic Chip Capacitor
C8	0402	0.1uF	GRM155R71C104KA88D (Murata)	Ceramic Chip Capacitor

Table 2. 0.2 GHz – 3 GHz Application Schematic Components

Circuit Symbol	Size	Value	Part Number	Description
L1	0402	100nH	LL1005-FHLR10J (Toko)	MLC Inductor
C1	0402	10pF	GRM1555C1H100JZ01B (Murata)	Ceramic Chip Capacitor
C2	0402	0.1uF	GRM155R71C104KA88D (Murata)	Ceramic Chip Capacitor
C3	0805	2.2uF	GRM21BR61E225KA12L (Murata)	Ceramic Chip Capacitor
C7	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor
C8	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor

Table 3. 1.5 GHz – 2.6 GHz Application Schematic Components

Circuit Symbol	Size	Value	Part Number	Description
L1	0402	5.6nH	LL1005-FHL5N6S (Toko)	MLC Inductor
C1	0402	100pF	GRM1555C1H101JZ01B (Murata)	Ceramic Chip Capacitor
C2	0402	0.1uF	GRM155R71C104KA88D (Murata)	Ceramic Chip Capacitor
C3	0805	2.2uF	GRM21BR61E225KA12L (Murata)	Ceramic Chip Capacitor
C7	0402	20pF	GRM1555C1H200JZ01B (Murata)	Ceramic Chip Capacitor
C8	0402	20pF	GRM1555C1H200JZ01B (Murata)	Ceramic Chip Capacitor

Test Circuit for S-Parameter and Noise Parameter

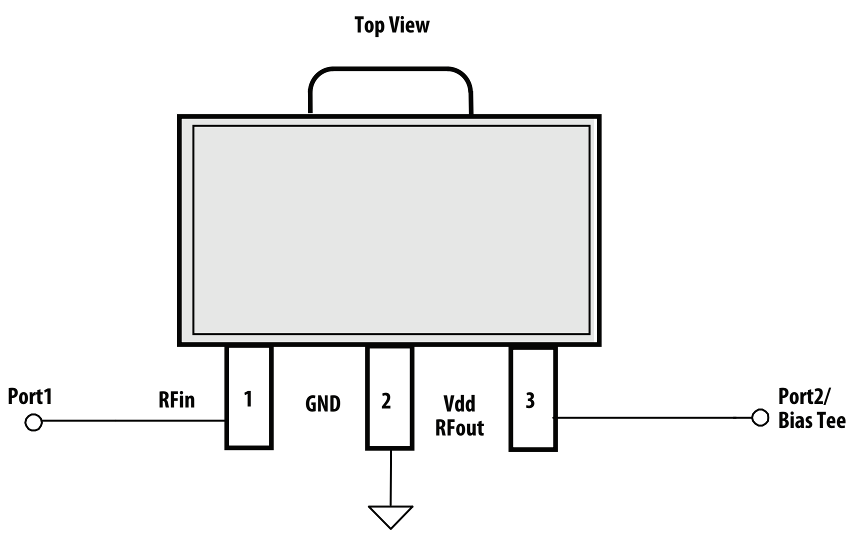


Figure 32. S-parameter and Noise parameter test circuit

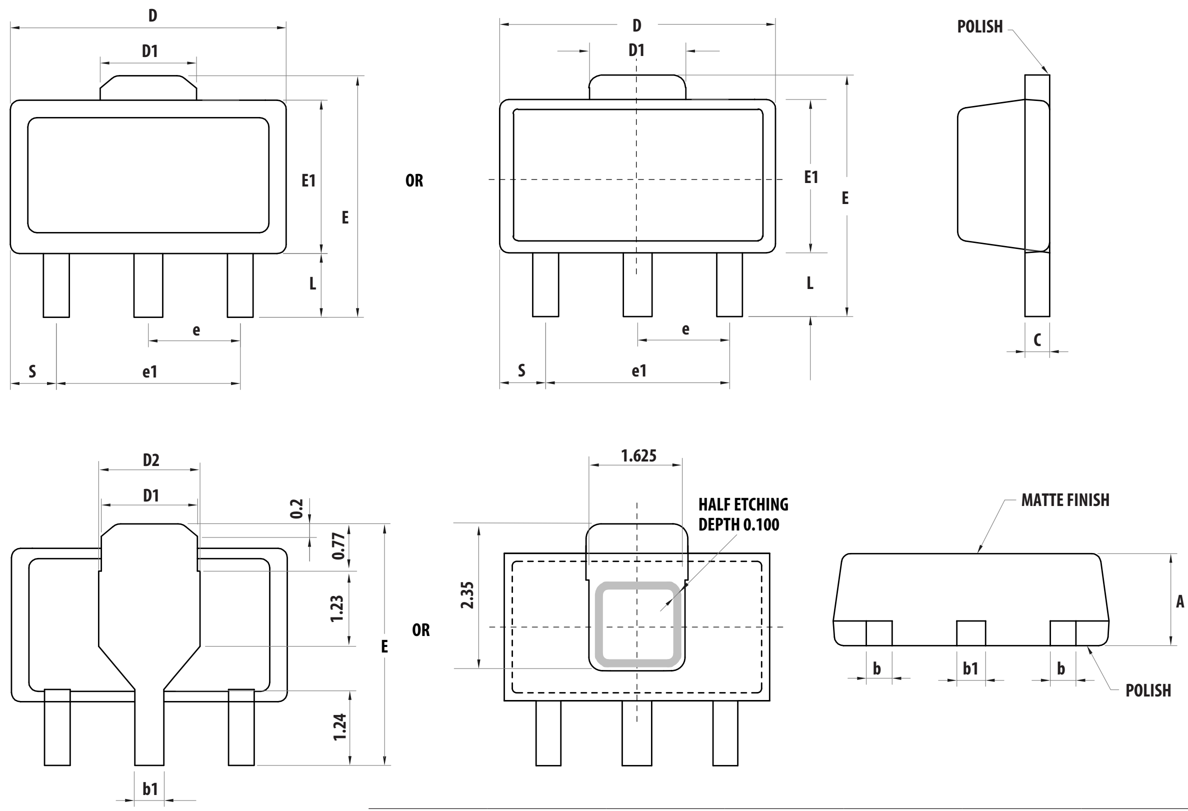
Typical S-Parameter (Vdd=5V, T=25°C, 50 ohm)

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.04	-12.99	-32.00	15.06	168.04	-20.92	5.28	-16.84	-127.51
0.1	-14.08	-27.40	14.79	169.90	-20.96	-2.48	-19.24	-154.22
0.2	-14.01	-38.85	14.76	165.35	-21.03	-8.75	-19.58	-162.15
0.3	-13.91	-53.66	14.74	159.56	-21.12	-14.11	-19.26	-164.02
0.4	-13.77	-68.63	14.73	153.53	-21.22	-19.09	-18.74	-163.03
0.5	-13.35	-83.56	14.73	147.37	-21.33	-23.96	-18.11	-160.98
0.6	-13.00	-97.71	14.73	141.14	-21.47	-28.71	-17.39	-160.35
0.7	-12.72	-111.41	14.73	134.86	-21.62	-33.44	-16.68	-161.36
0.8	-12.52	-124.63	14.74	128.51	-21.80	-38.09	-16.06	-163.41
0.9	-12.39	-137.62	14.76	122.08	-22.00	-42.67	-15.52	-166.34
1	-12.34	-150.05	14.78	115.62	-22.22	-47.13	-15.24	-169.82
1.1	-12.41	-161.87	14.82	109.17	-22.44	-51.53	-15.28	-173.97
1.2	-12.54	-175.41	14.84	102.50	-22.70	-55.82	-14.89	-179.03
1.3	-12.69	170.65	14.85	95.82	-22.99	-60.06	-14.57	175.40
1.4	-12.82	156.26	14.87	89.03	-23.31	-64.12	-14.31	169.62
1.5	-12.93	141.66	14.88	82.19	-23.64	-68.01	-14.12	163.81
1.6	-13.01	126.78	14.89	75.26	-23.99	-71.72	-14.00	157.96
1.7	-13.03	111.68	14.90	68.25	-24.35	-75.22	-13.93	152.01
1.8	-13.01	96.50	14.90	61.16	-24.71	-78.44	-13.94	146.11
1.9	-12.95	81.20	14.90	53.95	-25.07	-81.61	-14.00	140.34
2	-12.88	65.77	14.90	46.65	-25.43	-84.49	-14.15	134.63
2.1	-12.81	50.14	14.89	39.20	-25.77	-87.34	-14.40	129.04
2.2	-12.70	34.17	14.87	31.61	-26.12	-90.10	-14.76	123.74
2.3	-12.58	17.76	14.83	23.90	-26.47	-92.75	-15.29	118.58
2.4	-12.41	0.95	14.78	16.00	-26.81	-95.33	-16.00	113.77
2.5	-12.16	-16.14	14.71	7.96	-27.17	-98.00	-16.96	109.37
2.6	-11.80	-33.20	14.61	-0.24	-27.55	-100.74	-18.30	105.50
2.7	-11.33	-49.82	14.49	-8.55	-28.00	-103.33	-20.25	102.35
2.8	-10.76	-65.59	14.34	-17.05	-28.53	-105.61	-23.31	101.97
2.9	-10.13	-80.17	14.15	-25.68	-29.14	-107.36	-28.97	113.12
3	-9.48	-93.20	13.93	-34.41	-29.83	-107.91	-32.62	-162.21
4	-4.21	-168.28	7.93	-120.56	-27.04	-106.92	-5.05	172.01
5	-3.59	147.25	0.81	-166.87	-26.54	-152.31	-5.03	119.44
6	-3.85	96.49	-4.08	149.56	-27.32	163.02	-5.99	64.27
7	-2.69	44.14	-9.83	107.31	-29.75	120.51	-4.59	18.14
8	-1.77	16.03	-14.96	78.14	-31.67	91.43	-3.79	-4.64
9	-1.75	-9.43	-17.88	50.07	-31.40	63.78	-4.06	-28.88
10	-1.78	-50.02	-20.61	13.00	-31.03	27.56	-3.96	-68.59
11	-1.13	-83.66	-24.77	-17.84	-32.33	-2.54	-2.84	-99.28
12	-0.68	-93.53	-27.85	-31.54	-32.97	-16.55	-2.41	-112.27
13	-0.60	-96.96	-28.26	-42.20	-31.56	-29.12	-3.06	-124.68
14	-0.75	-111.43	-27.18	-66.26	-29.27	-55.40	-5.12	-151.90
15	-0.78	-137.85	-27.02	-107.10	-28.39	-98.30	-10.11	172.41
16	-0.60	-158.35	-29.80	-158.40	-30.72	-150.20	-13.09	-114.20
17	-0.46	-169.66	-36.11	159.22	-36.78	166.86	-4.23	-127.84
18	-0.46	-177.82	-41.41	126.91	-42.05	133.28	-2.40	-147.29
19	-0.56	173.41	-43.20	81.20	-44.00	83.71	-2.16	-162.89
20	-0.76	158.69	-40.61	50.84	-41.28	51.14	-2.26	-173.39

Typical Noise Parameters (Vdd=5V, T=25°C, 50 ohm)

Freq (GHz)	Fmin (dB)	Γ_{opt} Mag	Γ_{opt} Ang	Rn/Z0
0.4	3.04	0.203	13.20	0.522
0.9	2.80	0.205	14.50	0.466
1.0	2.87	0.208	16.30	0.468
1.7	2.82	0.211	19.80	0.496
1.85	2.81	0.214	20.80	0.512
2.0	2.83	0.217	26.10	0.526
2.5	3.05	0.280	51.60	0.59
3.0	3.84	0.356	95.30	0.596
3.5	4.27	0.468	142.00	0.362
4.0	5.18	0.537	174.50	0.234
4.5	5.20	0.522	-163.90	0.29
5.0	6.16	0.534	-142.24	0.618

SOT89 Package Dimensions

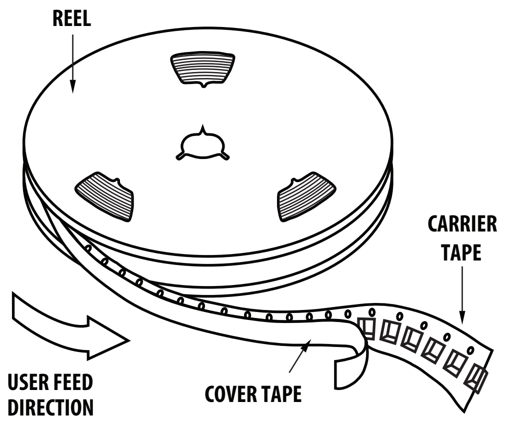


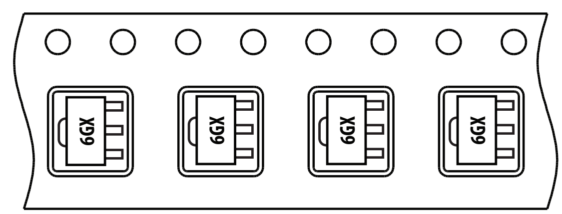
	Dimensions in mm			Dimensions in inches		
Symbols	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
A	1.40	1.50	1.60	0.055	0.059	0.063
L	0.89	1.04	1.20	0.0350	0.041	0.047
b	0.36	0.42	0.48	0.014	0.016	0.018
b1	0.41	0.47	0.53	0.016	0.018	0.030
C	0.38	0.40	0.43	0.014	0.015	0.017
D	4.40	4.50	4.60	0.173	0.177	0.181
D1	1.40	1.60	1.75	0.055	0.062	0.069
D2	1.45	1.65	1.80	0.055	0.062	0.069
E	3.94	-	4.25	0.155	-	0.167
E1	2.40	2.50	2.60	0.094	0.098	0.102
e1	2.90	3.00	3.10	0.114	0.118	0.122
S	0.65	0.75	0.85	0.026	0.030	0.034
e	1.40	1.50	1.60	0.054	0.059	0.063

Part Number Ordering Information

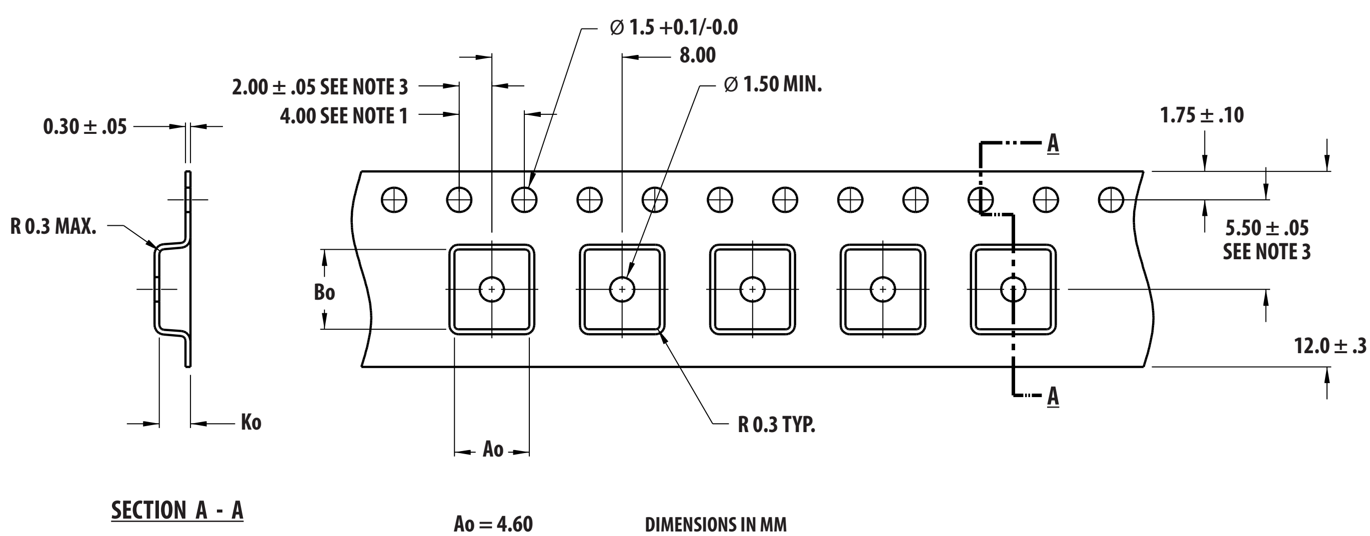
Part Number	No. of Devices	Container
MGA-30689-BLKG	100	7” Tape/Reel
MGA-30689-TR1G	3000	13” Tape/Reel

Device Orientation





Tape Dimensions

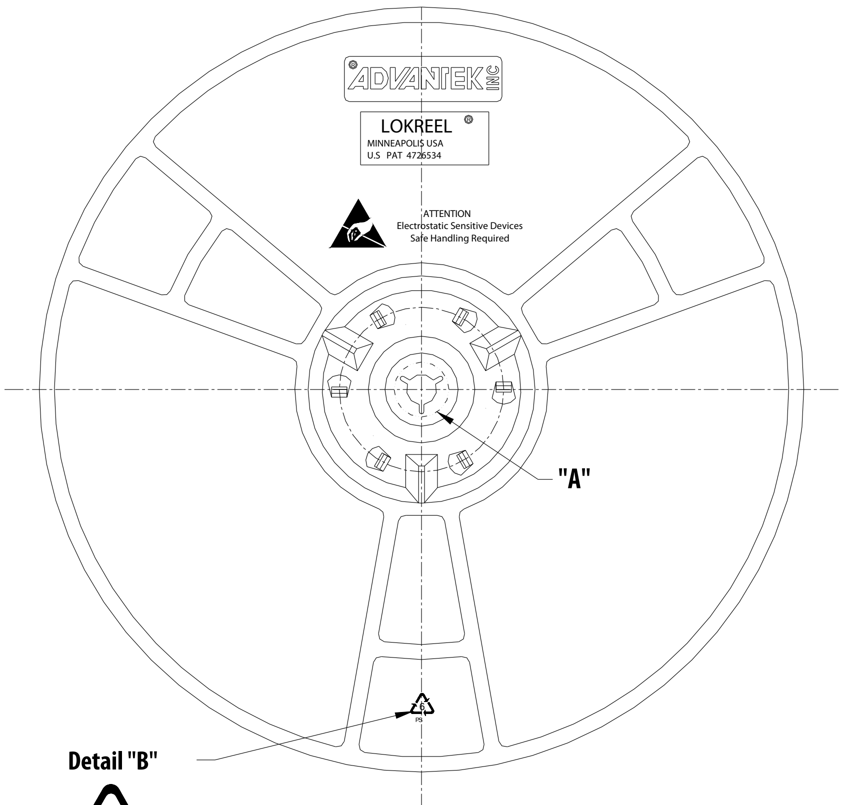


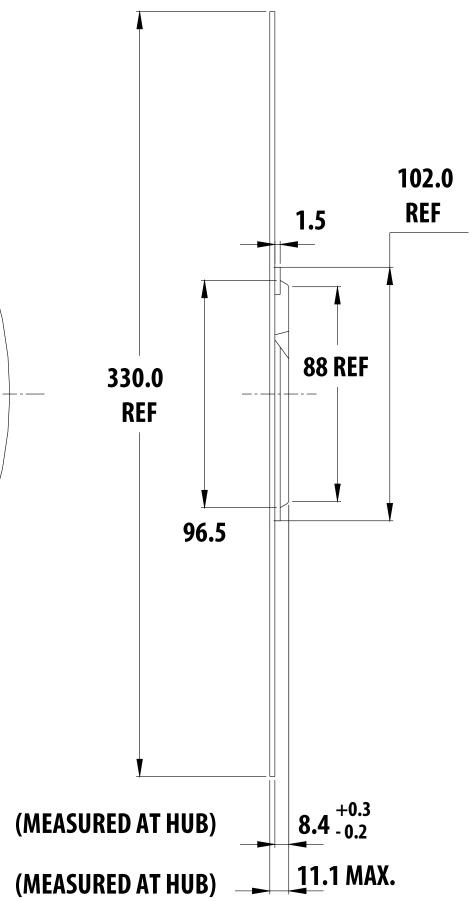
Ao = 4.60
Bo = 4.90
Ko = 1.90

DIMENSIONS IN MM

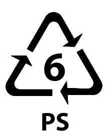
NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Reel Dimensions – 13” Reel

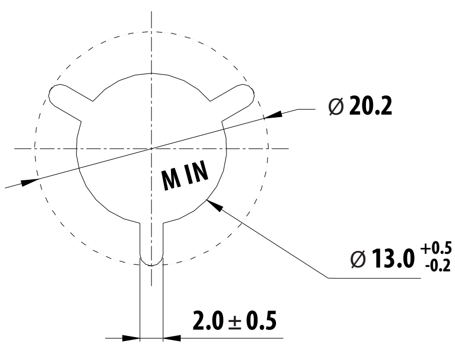




Detail "B"



Detail "A"



Dimensions in mm

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1876EN - November 11, 2013

MGA-31589

0.5 W High Gain Driver Amplifier

Data Sheet

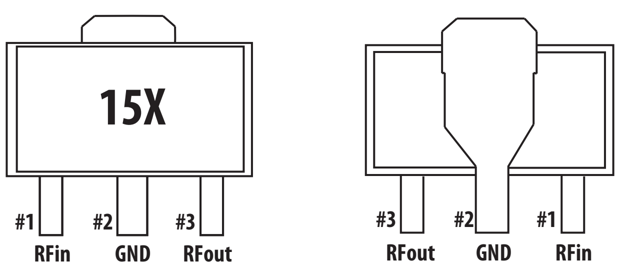
Description

Avago Technologies' MGA-31589 is a 0.5 W, high Gain, high performance Driver Amplifier MMIC, housed in a standard SOT-89 plastic package. The device required simple matching components to achieve optimum performance within specific 100 to 200 MHz bandwidth.

MGA-31589 is especially ideal for wireless infrastructure applications that operate within the 450 MHz to 1.5 GHz frequency range. With high IP3 and low noise figure, the MGA-31589 may be utilized as a driver amplifier in the transmit chain and as second or third stage LNA in the receive chain. For optimum performance at higher frequency from 1.5 GHz to 3.0 GHz, MGA-31689 is recommended.

MGA-31589's high gain and high linearity features are achieved through the use of Avago Technologies' proprietary 0.25 μm GaAs Enhancement-mode pHEMT process.

Pin connections and Package Marking



Top View   Bottom View

Note:
Top View: Package marking provides orientation and identification
"15" = Device Code
"X" = Date Code character indentifies month of manufacturing

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 150 V
ESD Human Body Model = 650 V
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Features

- ROHS compliant
- Halogen free
- High linearity at low DC bias power [1]
- High Gain
- Low noise figure
- High OIP3
- Advanced enhancement mode PHEMT Technology
- Excellent uniformity in product specification
- SOT-89 standard package

Specifications

At 0.9 GHz, Vdd = 5 V, Idd = 146 mA (typical) at 25° C

- OIP3 = 45.3 dBm
- Noise Figure = 1.9 dB
- Gain = 20.4 dB
- P1dB = 27.2 dBm
- IRL = 14.0 dB, ORL = 11.6 dB

Note:
1. The MGA-31589 has a superior LFOM of 16. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

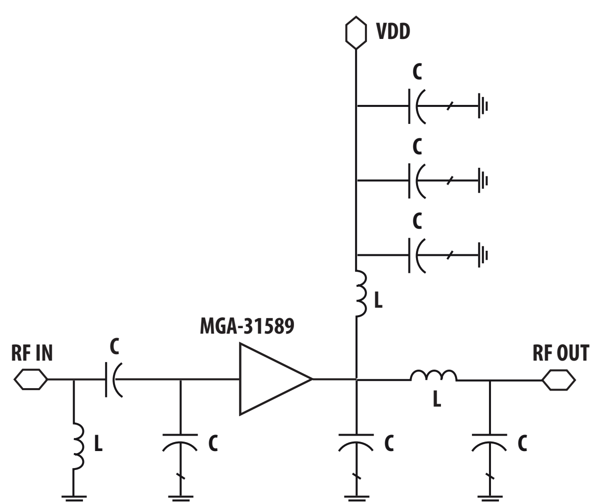


Figure 1. Simplified Schematic diagram

MGA-31589 Absolute Maximum Rating [1]

Symbol	Parameter	Units	Absolute Max.
$V_{dd, max}$	Drain Voltage, RF output to ground	V	5.5
P_d	Power Dissipation (2)	mW	1050
P_{in}	CW RF Input Power	dBm	17
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance

Thermal Resistance [3] (V_{dd} = 5.0 V, I_{dd} = 146 mA, T_c = 85° C), θ_{jc} = 44° C/W

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Source lead temperature is 25° C. Derate 22.7 mW/° C for T_L>103.8° C.
3. Thermal resistance measured using 150° C Infra-Red Microscopy Technique.

MGA-31589 Electrical Specification [1]

T_C = 25° C, Z_o = 50 Ω, V_{dd} = 5 V, unless specified.

Symbol	Parameter and Test Condition	Frequency (MHz)	Units	Min.	Typ.	Max.
I_{ds}	Quiescent Current	NA	mA	115	146	175
NF	Noise Figure	700	dB		2.35	
		900			1.92	2.8
Gain	Gain	700	dB		20.5	
		900		19.3	20.4	22.0
OIP3	Output Third Order Intercept Point	700 [2]	dBm		45.2	
		900 [2]		40.0	45.3	
P1dB	Output Power at 1 dB Gain Compression	700	dBm		26.4	
		900		26.3	27.2	
PAE	Power Added Efficiency at P1dB	700	%		43.6	
		900			45.0	
IRL	Input Return Loss	700	dB		20.0	
		900			14.0	
ORL	Output Return Loss	700	dB		10.4	
		900			11.6	
ISOL	Isolation	700	dB		28.0	
		900			27.5	

Note :
1. Measurements obtained from a test circuit described in Figure 27.
2. OIP3 test condition: F1 - F2 = 1.0 MHz, with input power of -8 dBm per tone measured at worst case side band.

MGA-31589 Consistency Distribution Chart [1,2]

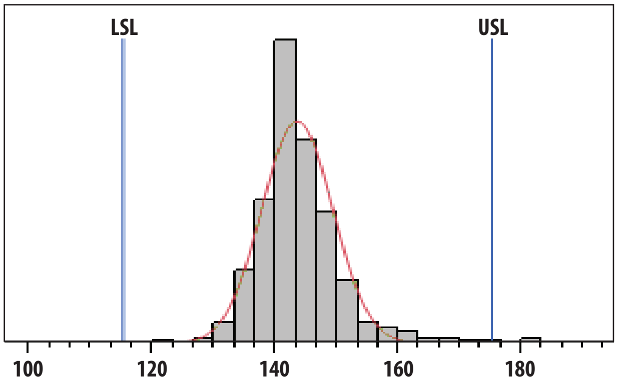


Figure 2. Idd at Vdd = 5 V, LSL = 115 mA , Nominal = 146 mA, USL = 175 mA

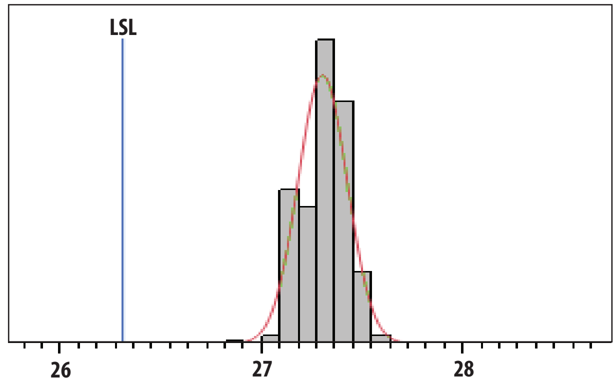


Figure 3. OP1dB at 900 MHz, Vdd = 5 V, LSL= 26.3 dBm, Nominal = 27.2 dBm

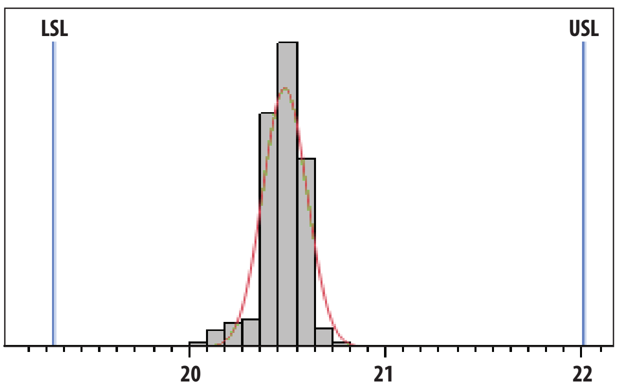


Figure 4. Gain at 900 MHz, Vdd = 5 V, LSL = 19.3 dB, Nominal = 20.4 dB, USL = 22.0 dB

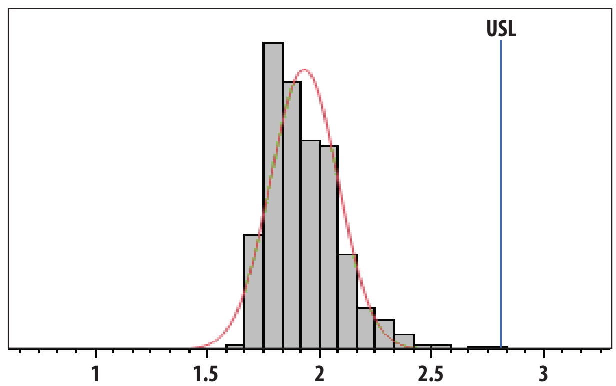


Figure 5. NF at 900 MHz, Vdd = 5 V, Nominal = 1.92 dB, USL = 2.8 dB

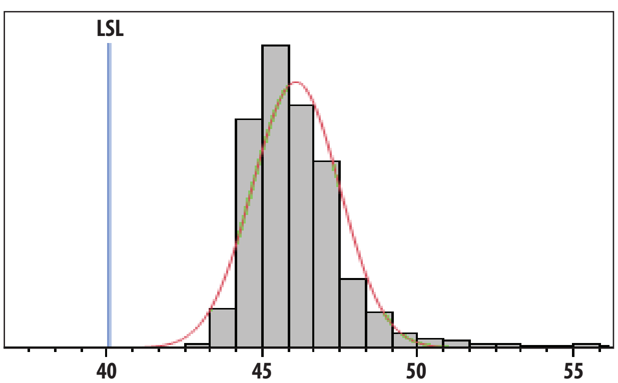


Figure 6. OIP3 at 900 MHz, Vdd = 5 V, LSL = 40.0 dBm, Nominal = 45.3 dBm

Notes:

1. Data sample size is 2500 samples taken from 5 wafers and 3 different wafer lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
2. Measurements are made on production test board which represents a trade off between nominal Gain, NF, OIP3, and OP1dB. Circuit losses have been de-embedded from actual measurements.

MGA-31589 Application Circuit Data for 700 MHz

$T_A = 25° C, V_{dd} = 5 V, I_{dd} = 146 mA$

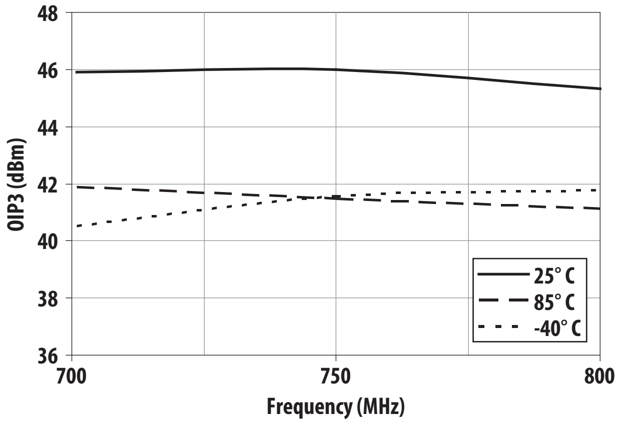


Figure 7. Over Temperature OIP3 vs Frequency

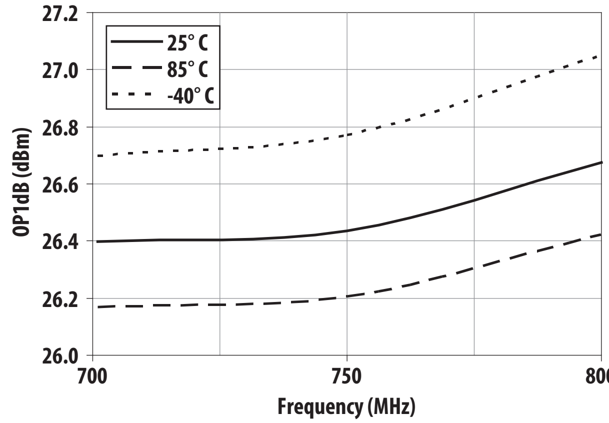


Figure 8. Over Temperature OP1dB vs Frequency

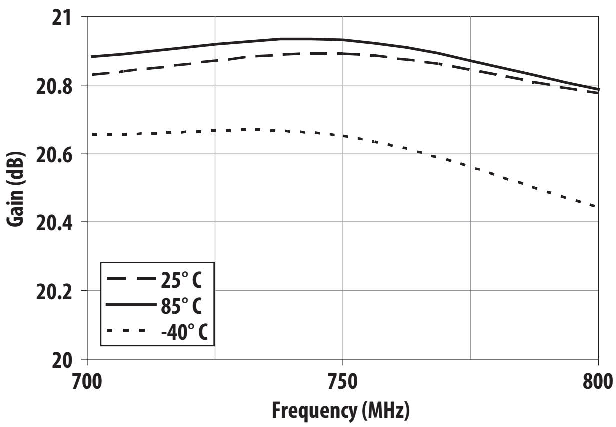


Figure 9. Over Temperature Gain vs Frequency

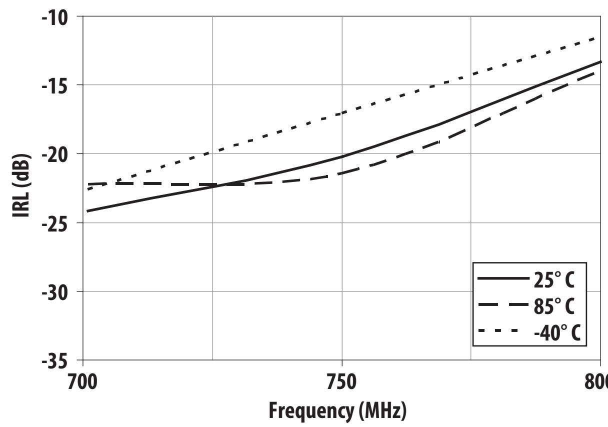


Figure 10. Over Temperature IRL vs Frequency

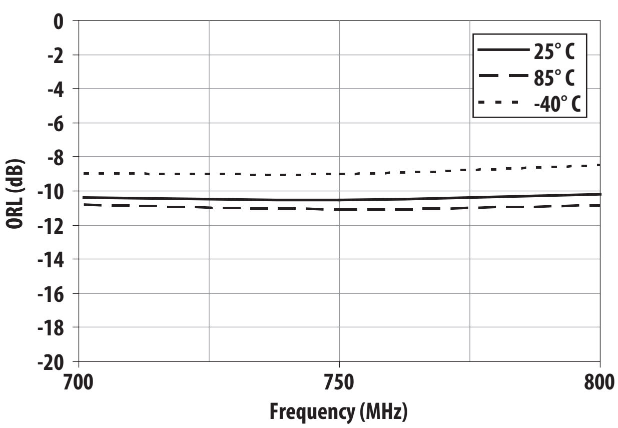


Figure 11. Over Temperature ORL vs Frequency

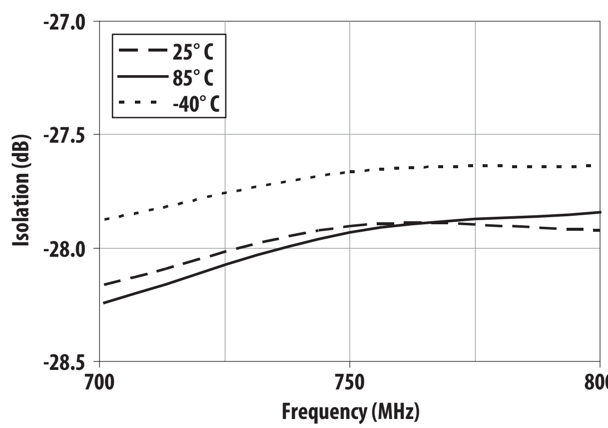


Figure 12. Over Temperature Isolation vs Frequency

MGA31589 Application Circuit Data for 700 MHz (continued)

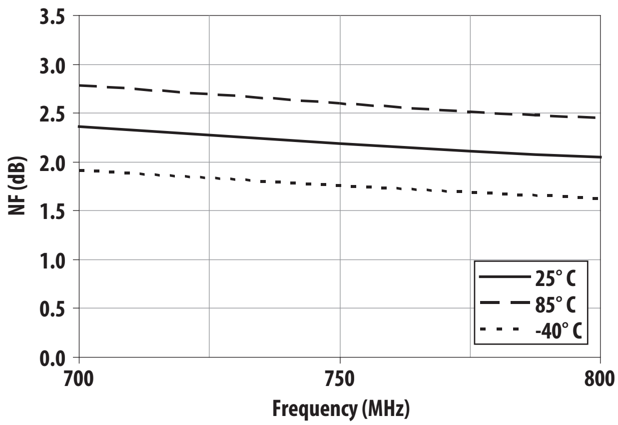


Figure 13. Over Temperature Noise Figure vs Frequency

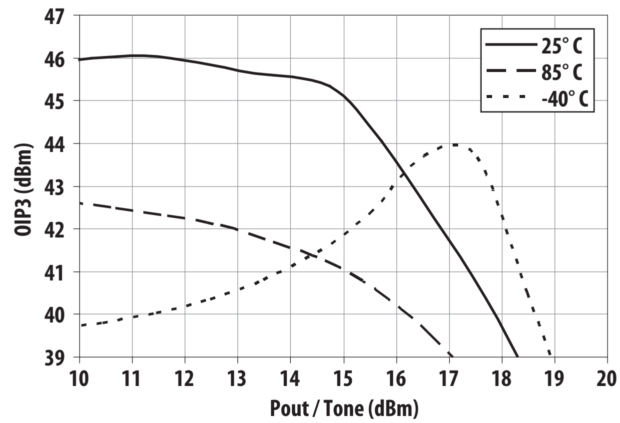


Figure 14. Over Temperature OIP3 at 700 MHz vs Pout

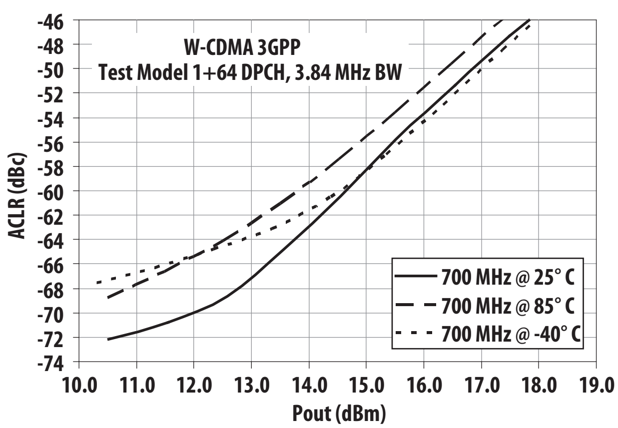


Figure 15. Over Temperature ACLR vs Pout at 700 MHz

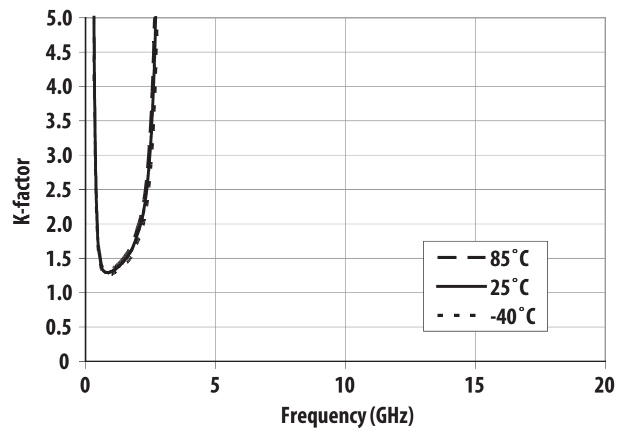


Figure 16. Over Temperature K-factor vs Frequency

MGA-31589 Application Circuit Data for 900 MHz

T_A = 25° C, V_{dd} = 5 V, I_{dd} = 146 mA

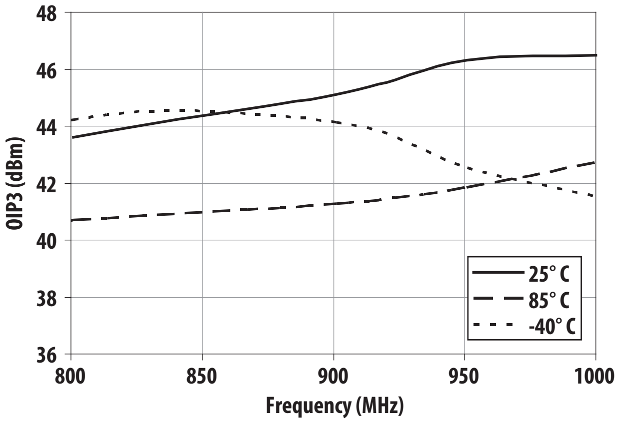


Figure 17. Over Temperature OIP3 vs Frequency

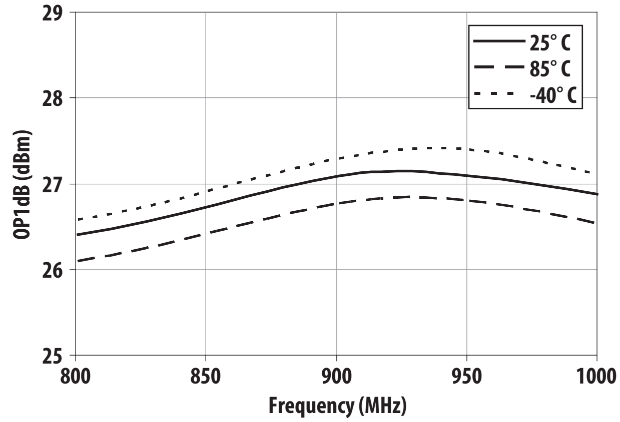


Figure 18. Over Temperature OP1dB vs Frequency

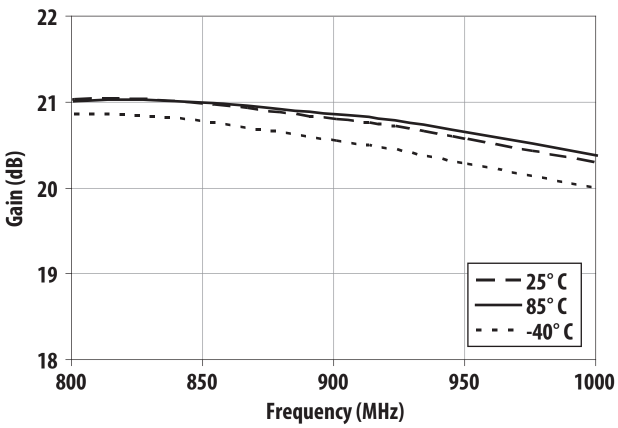


Figure 19. Over Temperature Gain vs Frequency

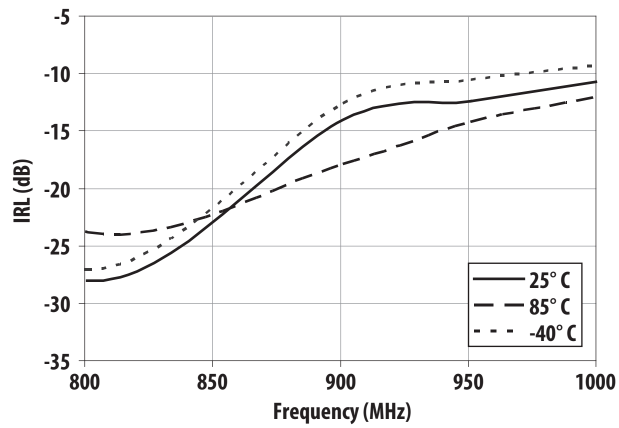


Figure 20. Over Temperature IRL vs Frequency

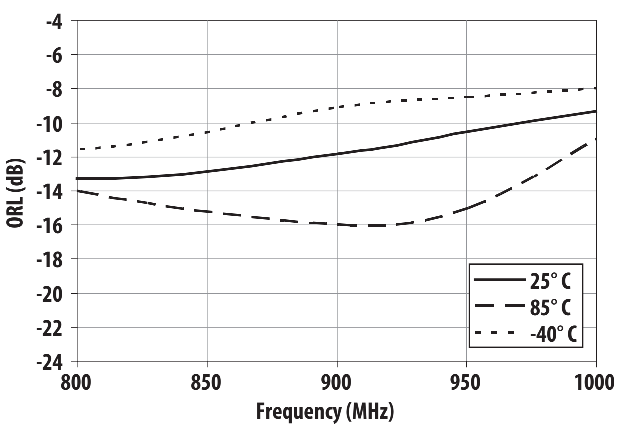


Figure 21. Over Temperature ORL vs Frequency

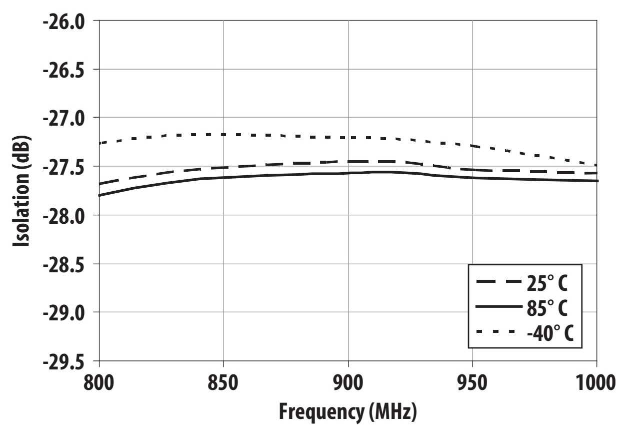


Figure 22. Over Temperature Isolation vs Frequency

MGA-31589 Application Circuit Data for 900 MHz (continued)

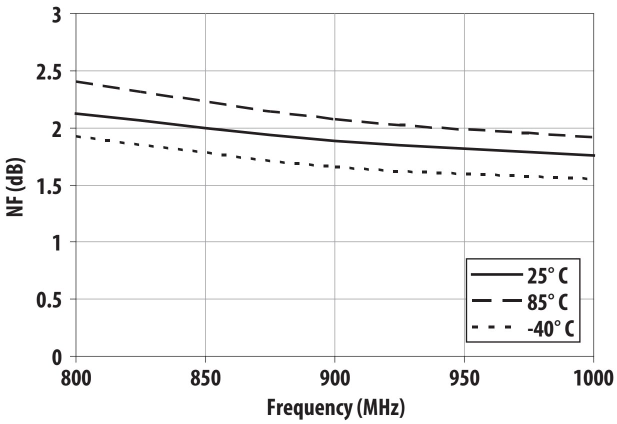


Figure 23. Over Temperature Noise Figure vs Frequency

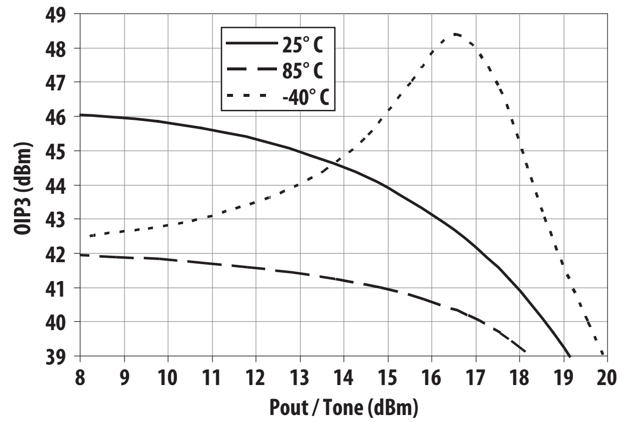


Figure 24. Over Temperature OIP3 vs Pout at 900 MHz

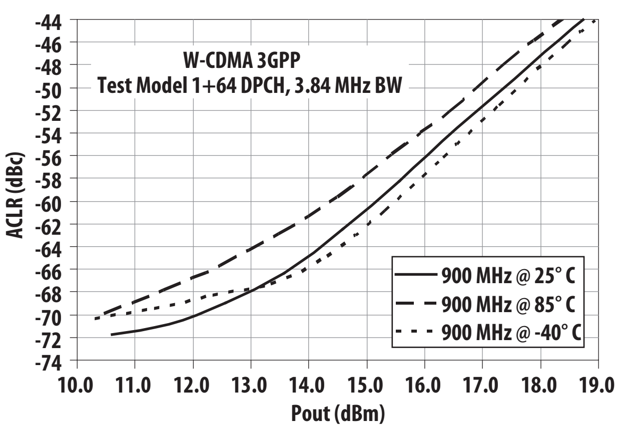


Figure 25. Over Temperature ACLR vs Pout at 900 MHz

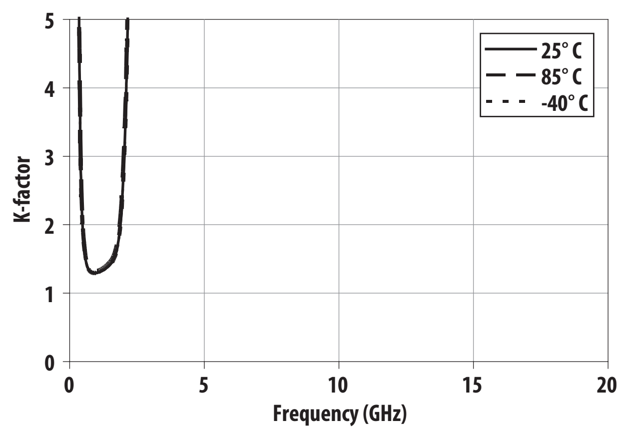


Figure 26. Over Temperature K-factor vs Frequency

Application Circuit Description and Layout

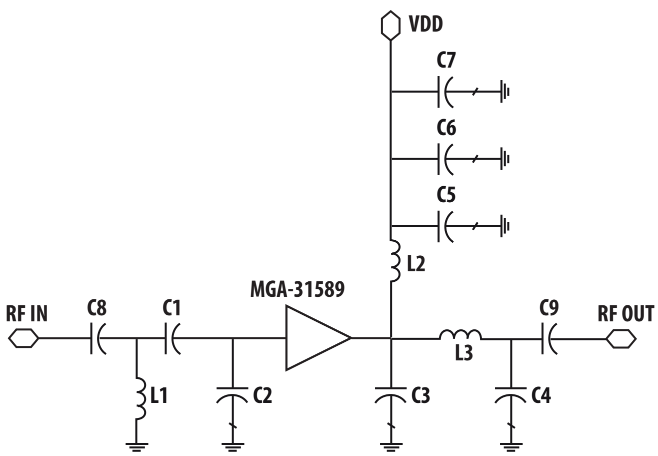


Figure 27. Circuit diagram

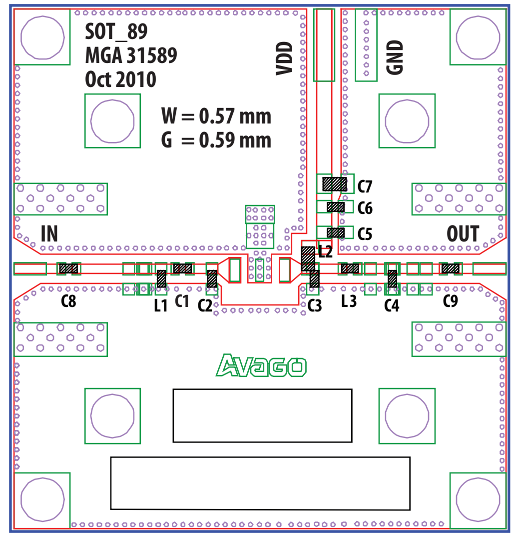


Figure 28. Demo board

Bill of Materials

Circuit Symbol	Size	Description For 700 – 800 MHz Value	Part Number	Manufacturer	Description For 800 – 1000 MHz Value	Part Number	Manufacturer
C1	0402	6.8 pF	CM05CH6R8C50AH	Kyocera	5.6 pF	CM05CH5R6C50AH	Kyocera
C2	0402	3.3 pF	CM05CH3R3C50AH	Kyocera	5.1 pF	CM05CH5R1C50AH	Kyocera
C3	0402	1.2 pF	CM05CH1R2C50AH	Kyocera	3.9 pF	CM05CH3R9C50AH	Kyocera
C4	0402	3.6 pF	CM05CH3R6C50AH	Kyocera	3.0 pF	GJM1555C1H3R0BB01D	Murata
C5	0402	100 pF	GRM1555C1H101JA01B	Murata	100 pF	GRM1555C1H101JA01B	Murata
C6	0402	0.1 µF	GRM155R71C104KA88D	Murata	0.1 µF	GRM155R71C104KA88D	Murata
C7	0805	2.2 µF	GRM21BR61A225KA01L	Murata	2.2 µF	GRM21BR61A225KA01L	Murata
C8*	0402	100 pF	GRM1555C1H101JA01B	Murata	100 pF	GRM1555C1H101JA01B	Murata
C9*	0402	100 pF	GRM1555C1H101JA01B	Murata	100 pF	GRM1555C1H101JA01B	Murata
L1	0402	5.6 nH	MLK1005S5N6DT000	TDK	5.6 nH	LLP1005-FH5N6C	Toko
L2	0603	22 nH	0603CS-22NXJLW	CoilCraft	22 nH	0603CS-22NXJLW	CoilCraft
L3	0402	2.7 nH	LLP1005-FH2N7C	Toko	4.3 nH	HK10054N3S-T	TaiyoYuden

Note: * as blocking capacitor, not required in actual application circuit.

For best performance, MGA-31589 requires only simple input and output matching network. The C3, C4, and L3 act as the output tuning circuitry for matching and OIP3 optimization. Bandpass network C1,C2, and L1 forms the input matching network. To bias MGA-31589, a +5 V supply (Vdd) is connected to the output pin thru a RF choke, L2 (which isolates the inband signal from the DC supply). The low frequency bypass capacitors C6 and C7 help to eliminate low frequency signals from power supply. Blocking capacitors are required for its input (C8) and output (C9), to isolate the supply voltage from succeeding circuits. The recommended output tuning is for achieving wideband best OIP3, while meeting typical specifications for other parameters.

MGA31589 Typical Scattering Parameter [1]

$T_A = 25°\ C, V_{dd} = 5.0\ V, I_{dd} = 146\ mA, Z_o = 50\ \Omega$

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)	k
0.1	-1.77	-176.55	19.58	136.19	-34.90	8.42	-3.27	-170.20	0.972
0.2	-1.67	177.54	16.85	145.31	-35.04	7.22	-3.22	-177.59	1.244
0.3	-1.72	173.67	16.41	149.08	-34.65	10.46	-2.82	179.75	1.275
0.4	-1.77	170.76	16.37	147.43	-34.05	11.21	-2.29	174.84	1.212
0.5	-1.83	168.30	16.34	143.00	-33.53	9.91	-2.07	169.34	1.177
0.6	-1.87	165.91	16.23	138.05	-33.16	8.33	-2.02	164.14	1.166
0.7	-1.90	163.53	16.08	133.00	-32.88	6.93	-2.06	159.35	1.168
0.8	-1.94	161.13	15.93	127.98	-32.61	5.62	-2.14	154.89	1.176
0.9	-1.98	158.73	15.76	123.03	-32.38	4.31	-2.25	150.65	1.189
1.0	-2.05	155.91	15.71	117.78	-32.03	2.68	-2.42	146.01	1.201
1.5	-2.30	143.20	15.13	94.05	-30.80	-5.20	-3.26	126.15	1.269
2.0	-2.58	131.24	14.79	71.01	-29.78	-15.44	-4.42	106.91	1.339
2.5	-2.97	119.80	14.64	46.54	-29.03	-29.02	-6.37	85.09	1.432
3.0	-3.38	109.13	14.52	20.10	-28.80	-45.16	-9.78	59.67	1.563
3.5	-3.66	99.38	14.28	-8.36	-29.30	-62.45	-17.08	28.50	1.750
4.0	-3.67	89.65	13.76	-38.65	-30.76	-78.63	-23.37	-158.95	2.051
4.5	-3.35	78.37	12.79	-70.05	-33.36	-87.86	-11.25	161.18	2.557
5.0	-2.72	69.55	11.22	-99.35	-35.92	-78.23	-7.01	133.77	2.926
5.5	-2.25	54.25	9.39	-127.96	-35.02	-63.36	-4.96	106.20	2.228
6.0	-1.90	37.98	7.35	-154.25	-32.62	-63.92	-3.73	81.48	1.420
6.5	-1.66	22.07	5.23	-178.40	-30.75	-73.57	-2.92	59.47	0.964
7.0	-1.49	6.75	3.14	158.99	-29.45	-86.55	-2.40	39.44	0.726
7.5	-1.37	-8.46	1.07	137.02	-28.55	-101.24	-2.10	20.23	0.634
8.0	-1.31	-23.53	-1.12	115.64	-28.08	-116.73	-1.99	1.07	0.763
8.5	-1.24	-38.62	-3.42	94.86	-27.89	-132.58	-1.99	-18.26	1.040
9.0	-1.15	-52.86	-5.90	75.16	-28.05	-148.05	-2.00	-37.13	1.491
9.5	-1.04	-65.05	-8.51	57.37	-28.46	-162.13	-1.93	-54.51	2.003
10.0	-0.93	-74.79	-11.10	41.67	-28.88	-174.70	-1.75	-69.74	2.471
10.5	-0.88	-83.14	-13.57	27.46	-29.23	173.83	-1.51	-82.60	2.966
11.0	-0.87	-91.24	-15.94	14.15	-29.46	162.64	-1.26	-93.38	3.480
11.5	-0.87	-99.83	-18.27	1.08	-29.63	151.89	-1.08	-102.57	4.186
12.0	-0.89	-108.98	-20.69	-12.23	-29.72	140.81	-0.99	-110.85	5.464
12.5	-0.90	-118.43	-23.36	-26.45	-29.77	128.66	-1.07	-119.52	8.527
13.0	-0.90	-127.25	-26.67	-42.33	-30.04	114.68	-1.36	-130.22	16.497
13.5	-0.79	-134.85	-31.56	-55.65	-30.86	102.56	-1.82	-144.24	36.982
14.0	-0.66	-142.23	-37.35	-61.23	-31.33	93.78	-2.25	-161.00	76.824
14.5	-0.64	-149.26	-47.45	-58.90	-31.61	84.09	-2.33	-176.91	255.376
15.0	-0.66	-156.32	-48.66	73.73	-31.91	75.57	-2.04	171.92	284.336
15.5	-0.71	-163.50	-40.13	79.58	-31.96	69.43	-1.64	166.22	96.597
16.0	-0.79	-170.94	-35.71	75.52	-31.36	64.76	-1.27	164.25	47.911
16.5	-0.85	-178.86	-32.13	66.97	-29.97	58.14	-0.97	163.32	23.387
17.0	-0.94	171.97	-29.15	54.52	-28.27	47.58	-0.83	160.50	13.048
17.5	-1.05	162.04	-26.61	39.34	-26.63	33.70	-1.09	152.54	11.264
18.0	-1.18	151.96	-24.66	20.98	-25.34	16.84	-2.03	137.49	14.322
18.5	-1.35	142.56	-23.66	1.12	-24.79	-1.31	-3.78	116.75	20.654
19.0	-1.50	134.05	-23.71	-15.16	-25.17	-15.72	-5.58	99.74	29.409
19.5	-1.72	127.31	-23.25	-26.68	-24.89	-25.23	-4.69	87.70	27.596
20.0	-1.98	122.16	-24.07	-36.24	-25.77	-32.73	-6.17	75.97	43.126

MGA-31589 Typical Noise Parameters [1]

$T_A = 25° C$, $V_{dd} = 5.0 V$, $I_{dd} = 146 mA$, $Z_o = 50 \Omega$

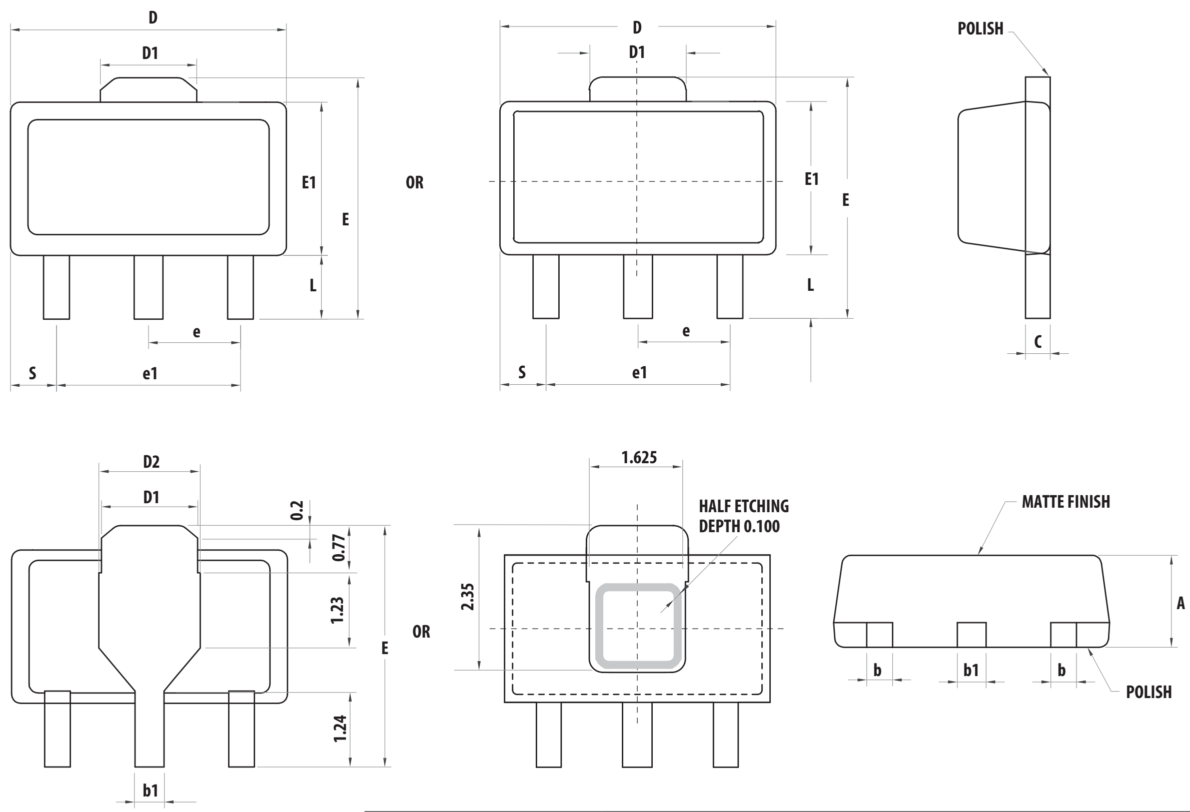
Freq (GHz)	F_{min} (dB)	Γ_{opt} Mag	Γ_{opt} Ang	R_n/Z_0	Ga (dB)
0.5	1.80	0.59	-163.70	0.08	22.27
0.8	1.75	0.59	-157.40	0.07	21.69
0.9	1.54	0.59	-158.60	0.06	21.39
1.0	1.53	0.59	-151.30	0.07	21.11
1.5	1.34	0.58	-143.30	0.09	19.79
2.0	1.23	0.57	-131.00	0.13	18.67
2.5	1.15	0.56	-119.80	0.19	17.84
3.0	1.30	0.54	-109.00	0.23	17.13
3.5	1.48	0.53	-99.50	0.34	16.60
4.0	1.93	0.52	-91.50	0.54	16.16
4.5	2.64	0.51	-78.50	0.81	15.76
5.0	3.68	0.50	-58.60	1.29	15.03
5.5	5.06	0.49	-22.80	1.98	13.26
6.0	6.70	0.48	-5.40	2.68	11.93

Note:
1. Measurements are made using 10 mils Rogers RO4350 TRL Board.

Part Number Ordering Information

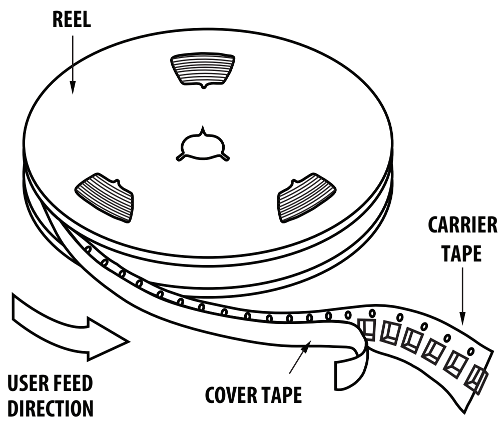
Part Number	No. of Devices	Container
MGA-31589-BLKG	100	7” Tape/Reel
MGA-31589-TR1G	3000	13” Tape/Reel

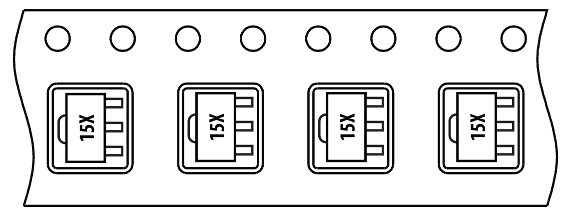
SOT89 Package Dimensions



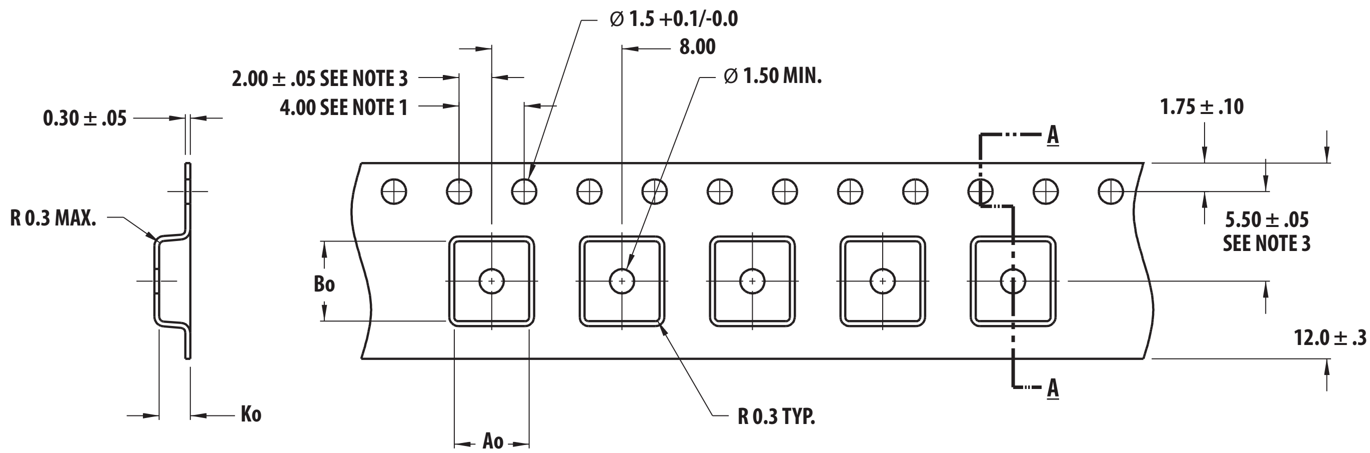
	Dimensions in mm			Dimensions in inches		
Symbols	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	1.40	1.50	1.60	0.055	0.059	0.063
L	0.89	1.04	1.20	0.0350	0.041	0.047
b	0.36	0.42	0.48	0.014	0.016	0.018
b1	0.41	0.47	0.53	0.016	0.018	0.030
C	0.38	0.40	0.43	0.014	0.015	0.017
D	4.40	4.50	4.60	0.173	0.177	0.181
D1	1.40	1.60	1.75	0.055	0.062	0.069
D2	1.45	1.65	1.80	0.055	0.062	0.069
E	3.94	-	4.25	0.155	-	0.167
E1	2.40	2.50	2.60	0.094	0.098	0.102
e1	2.90	3.00	3.10	0.114	0.118	0.122
S	0.65	0.75	0.85	0.026	0.030	0.034
e	1.40	1.50	1.60	0.054	0.059	0.063

Device Orientation





Tape Dimensions



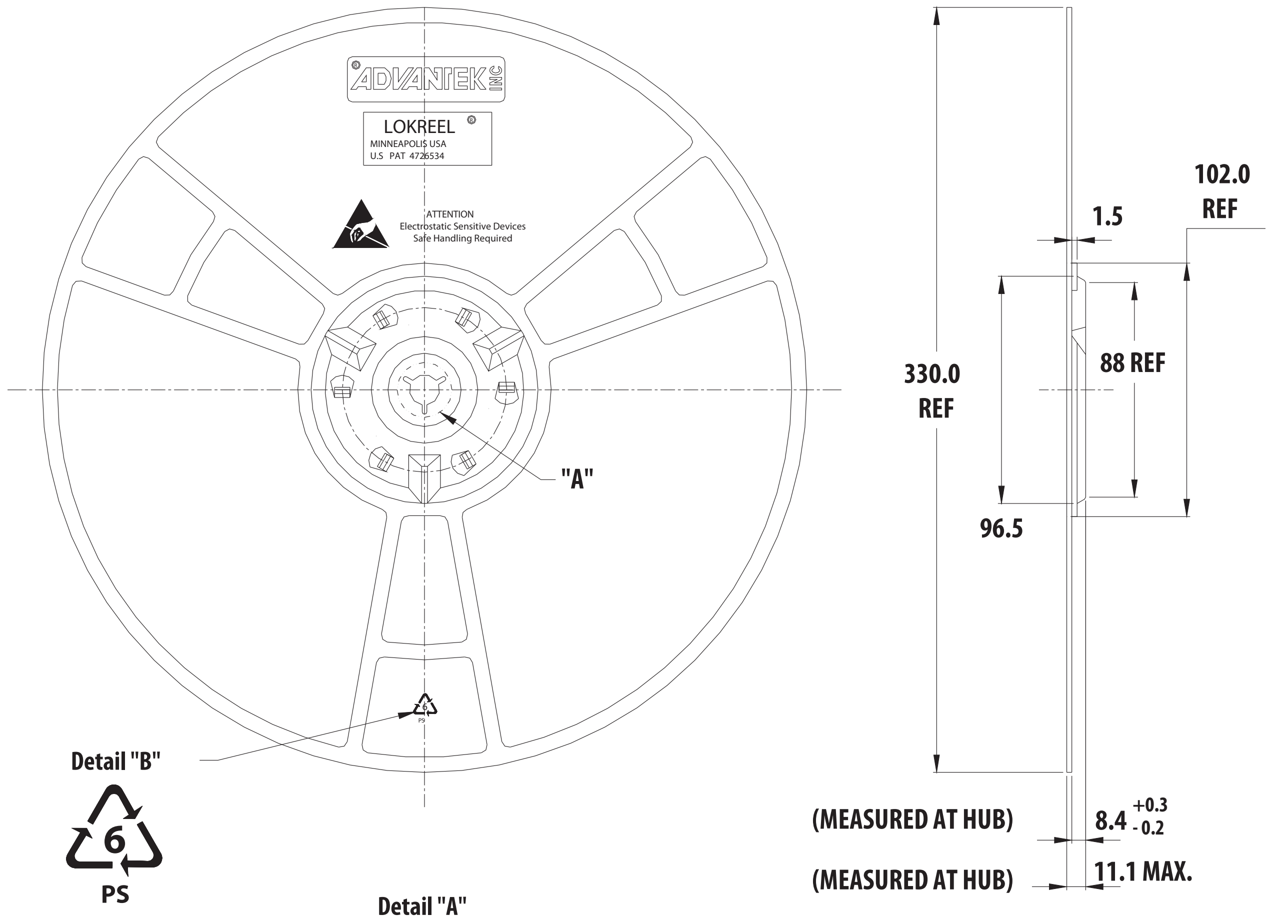
SECTION A - A

Ao = 4.60
Bo = 4.90
Ko = 1.90

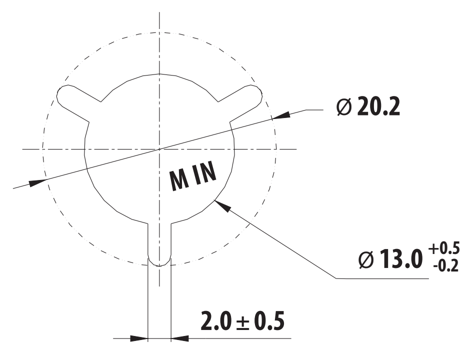
DIMENSIONS IN MM

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Reel Dimensions – 13" Reel



Detail "A"



Dimensions in mm

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-2744EN - November 11, 2013

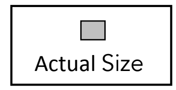
Programmable Crystal Oscillator

CMOS, LVDS, LVPECL Output

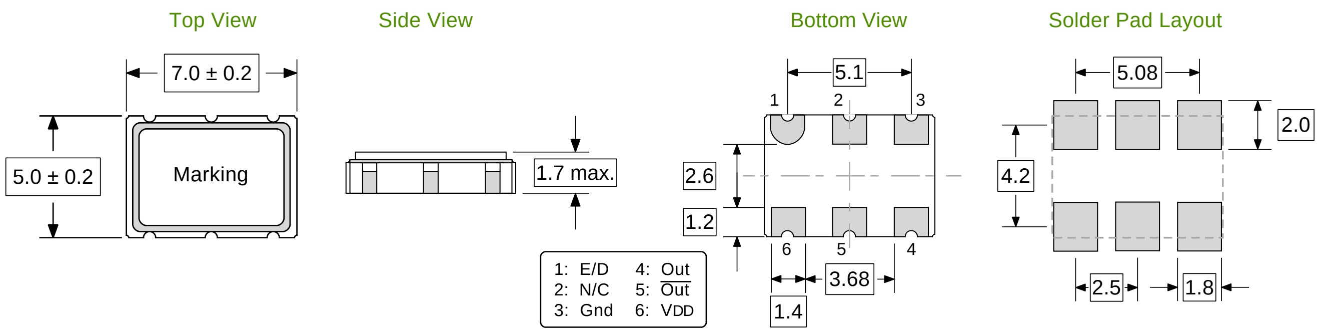
5.0 x 7.0 x 1.7mm Ceramic (6 pad) SMD
10MHz ~ 1.5GHz

Features

- Operational Voltage: 2.5, 3.3V ±5%
- 0.6pS Jitter (max.)
- Voltage Controlled
- Enable/Disable function
- CMOS, LVDS, LVPECL Output
- **RoHS Compliant Product**



Outlines & Dimensions (mm)



Electrical Specifications

Waveform Output	HCMOS	LVDS	LVPECL
Frequency	10MHz to 250MHz	10MHz to 1.5GHz	
Mode of Oscillation	Fundamental		
Supply Voltage	2.5V, 3.3V		
Frequency Stability vs. Temp. Range	±50ppm		
Input Current	40mA	30mA	70mA
Rise/Fall Time	4nS	600pS	
Phase Jitter	0.6pS (max.)		
Duty Cycle	45/55%		
Start-up Time	10mS (Max.)		
Enable/Disable Input Voltage	$V_{IH} \geq 0.7_{DD}$ or No Connect, $V_{IL} \leq 0.3V_{DD}$ or Ground		
Output Load	15pF	100Ω	50Ω
Aging/year	±3.0ppm (Max.)		
Operating Temp. Range	0 ~ +70°C		
Storage Temp. Range	-40 ~ +125°C		

Numbering Guide

Example: O75P2-622.0000M3T2MAE

Series	Frequency	Supply Voltage	Tri-state	Freq. Stability	Oper. Temp.	Waveform
O75P2	**xxx.xxxxM** = MHz xxx.xxxxG = GHz	2 = 2.5V **3** = 3.3V	T1 = Pin 1 **T2** = Pin 2 N = No Connect	L = ±25ppm **M** = ±50ppm N = ±100ppm	**A** = -40 ~ +85°C B = -20 ~ +70°C C = 0 ~ +70°C	C = HCMOS D = LVDS **E** = LVPECL

o75p2 series r2.0
Specifications subject to change without notice.

Ultra Linear Low Noise

Monolithic Amplifier

PGA-103+

50Ω 0.05 to 4 GHz

The Big Deal

- Ultra High IP3
- Broadband High Dynamic Range
- May be used as a replacement for RFMD SPF-5189Z[a,b]

SOT-89 PACKAGE

Product Overview

PGA-103+ (RoHS compliant) is an advanced wideband amplifier fabricated using E-PHEMT technology and offers extremely high dynamic range over a broad frequency range and with low noise figure. In addition, the PGA-103+ has good input and output return loss over a broad frequency range without the need for external matching components and has demonstrated excellent reliability. Lead finish is SnAgNi. It has repeatable performance from lot to lot and is enclosed in a SOT-89 package for very good thermal performance.

Key Features

Feature	Advantages
Broad Band: 0.05 to 4.0 GHz	Broadband covering primary wireless communications bands: Cellular, PCS, LTE, WiMAX
Ultra High IP3 Versus DC power Consumption: 45 dBm typical at 2 GHz at +5.0V Supply Voltage and only 97mA	The PGA-103+ provides excellent IP3 performance relative to device size and power consumption. The combination of the design and E-PHEMT Structure provides enhanced linearity over a broad frequency range as evidence in the IP3 being typically 20 dB above the P 1dB point. This feature makes this amplifier ideal for use in: • Driver amplifiers for complex waveform up converter paths • Drivers in linearized transmit systems • Secondary amplifiers in ultra High Dynamic range receivers
Low Noise Figure: 0.6 dB up to 1.0 GHz	A unique feature of the PGA-103+ which separates this design from all competitors is the low noise figure performance in combination with the high dynamic range.

Notes:
a. Suitability for model replacement within a particular system must be determined by and is solely the responsibility of the customer based on, among other things, electrical performance criteria, stimulus conditions, application, compatibility with other components and environmental conditions and stresses.
b. The RFMD SPF-5189Z part number is used for identification and comparison purposes only.

Ultra Linear Low Noise

Monolithic Amplifier

0.05-4 GHz

Product Features
- 5V/3V operation
- High IP3, 45 dBm typ. at 2 GHz, Vd=5V
- Low Noise Figure, 0.6 at 1 GHz; 0.9 dB at 2 GHz
- Gain, 11.0 dB typ. at 2 GHz
- P1dB 22.5 dBm typ. at 2 GHz at Vd=5V
- Protected under US Patent 8,803,612

PGA-103+

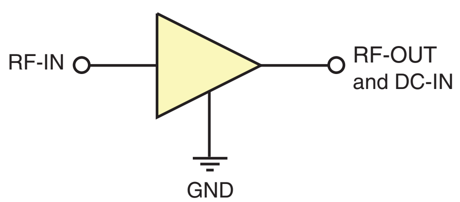
CASE STYLE: DF782

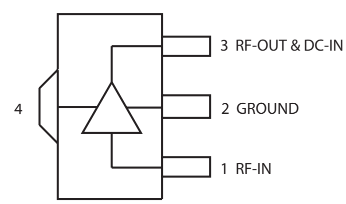
+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Typical Applications
- Base station infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- LTE

General Description
PGA-103+ (RoHS compliant) is an advanced wideband amplifier fabricated using E-PHEMT technology and offers extremely high dynamic range over a broad frequency range and with low noise figure. In addition, the PGA-103+ has good input and output return loss over a broad frequency range without the need for external matching components. Lead finish is SnAgNi. It has repeatable performance from lot to lot and is enclosed in a SOT-89 package for very good thermal performance.

simplified schematic and pin description





Function	Pin Number	Description
RF IN	1	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.
RF-OUT and DC-IN	3	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in “Recommended Application Circuit”, Fig. 2
GND	2,4	Connections to ground. Use via holes as shown in “Suggested Layout for PCB Design” to reduce ground path inductance for best performance.

Notes:
a. Suitability for model replacement within a particular system must be determined by and is solely the responsibility of the customer based on, among other things, electrical performance criteria, stimulus conditions, application, compatibility with other components and environmental conditions and stresses.
b. The RFMD SPF-5189Z part number is used for identification and comparison purposes only.

Electrical Specifications[1] at 25°C, 50Ω, unless noted

Parameter	Condition (GHz)	Vd=5V			Vd=3V	
		Min.	Typ.	Max.	Typ.	Units
Frequency Range		0.05		4.0		GHz
Gain	0.05	—	26.5	—	25.9	dB
	0.4	—	22.1	—	21.6	
	1.0	14.7	16.2	18.0	15.8	
	2.0	—	11.0	—	10.6	
	3.0	—	8.1	—	7.7	
	4.0	—	6.2	—	5.9	
Noise Figure	0.05		0.5		0.5	dB
	0.4		0.5		0.5	
	1.0		0.6		0.6	
	2.0		0.9		0.9	
	3.0		1.2		1.2	
	4.0		1.5		1.4	
Input Return Loss	0.05	—	6.7	—	6.1	dB
	0.4	—	11.3	—	10.4	
	1.0	10.0	13.0	—	12.0	
	2.0	—	12.8	—	13.0	
	3.0	—	13.7	—	13.0	
	4.0	—	15.0	—	14.2	
Output Return Loss	0.05	—	14.1	—	13.8	dB
	0.4	—	23.8	—	25.5	
	1.0	10.0	21.8	—	30.6	
	2.0	—	20.6	—	26.4	
	3.0	—	17.2	—	20.8	
	4.0	—	16.0	—	19.2	
Reverse Isolation	1.0		21.2		20.5	dB
Output Power @1 dB compression[2]	0.05		20.0		15.4	dBm
	0.4		21.5		18.2	
	1.0		22.5		18.7	
	2.0		22.5		19.3	
	3.0		22.9		20.0	
	4.0		23.2		20.7	
Output IP3	0.05	—	36.7	—	32.4	dBm
	0.4	—	39.0	—	34.1	
	1.0	—	41.9	—	34.5	
	2.0	40.0	44.6	—	35.6	
	3.0	—	44.3	—	35.6	
	4.0	—	45.4	—	35.3	
Device Operating Voltage		4.8	5.0	5.2	3.0	V
Device Operating Current			97	120	60	mA
Device Current Variation vs. Temperature			-178		-54	μA/°C
Device Current Variation vs Voltage			0.014		0.018	mA/mV
Thermal Resistance, junction-to-ground lead			36		36	°C/W

(1) Measured on Mini-Circuits Characterization test board TB-313. See Characterization Test Circuit (Fig. 1)
(2) Current increases at P1dB

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Operating Current at 5.0V	200 mA
Power Dissipation at 5.0V	1W
Input Power (CW)	+21 dBm (50 to 2000 MHz) +26 dBm (2000 to 4000 MHz)
DC Voltage on Pin 3	6V

Note:
Permanent damage may occur if any of these limits are exceeded.
Electrical maximum ratings are not intended for continuous normal operation.

Characterization Test Circuit

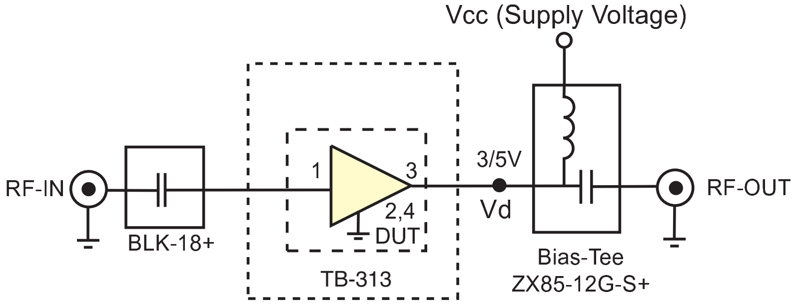
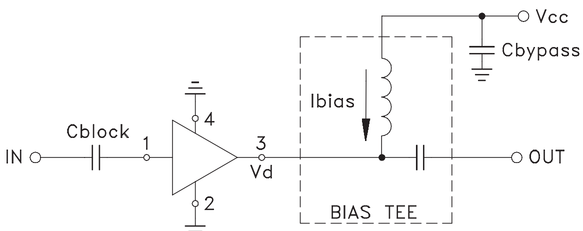


Fig 1. Block Diagram of Test Circuit used for characterization. (DUT tested on Mini-Circuits Characterization test board TB-313) Gain, Return loss, Output power at 1dB compression (P1 dB) , output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.

Recommended Application Circuit



Cblock=0.001μF, Bias-Tee=TCBT-14+, Cbypass=0.1μF

Fig 2a. Evaluation board TB-678-103+ includes case, connectors and components soldered to PCB

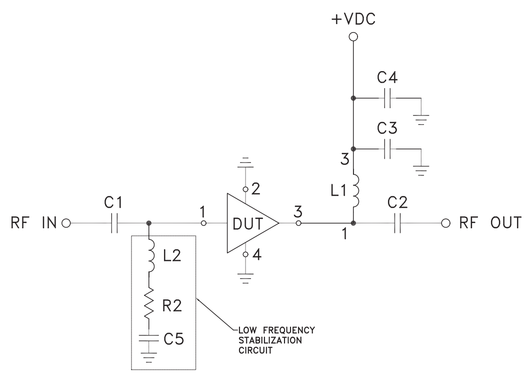
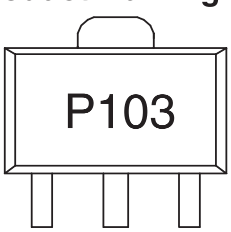


Fig 2b. Evaluation board TB-761-103+ unconditionally stable (see note AN-60-064)

SEQ	Manufacturer P/N / Value	Size
A1	PGA-103+	—
C1, C2	.01 uF	0805
C3	0.33 uF	1206
C4	10 uF	1206
C5	330 pF	0603
L1	TCCH-80+	—
L2	620 nH	.115X.110
R2	150 Ohm	0603

Product Marking



Additional Detailed Technical Information

additional information is available on our dash board. To access this information click here

Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DF782 (SOT 89) *Plastic package, exposed paddle lead finish: tin-silver over nickel*
Tape & Reel **Standard quantities available on reel**	F55 *7" reels with 20, 50, 100, 200, 500 or 1K devices*
Suggested Layout for PCB Design	PL-313
Evaluation Board	TB-678-103+ TB-761-103+ (see Application Note AN-60-064)
Environmental Ratings	ENV08T1

ESD Rating

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

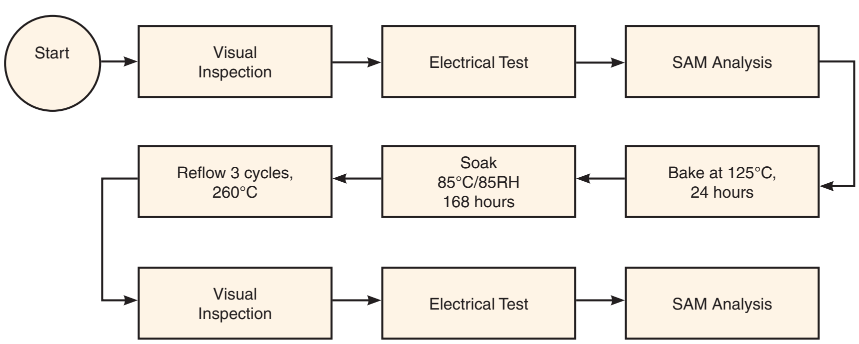
Machine Model (MM): Class M1(25V) in accordance with ANSI/ESD STM5.2-1999

Attention
Observe precautions for handling electrostatic sensitive devices

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



Notes
A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp

- ***Low-Loss RF Filter for Mobile Systems***
- ***Low Amplitude Ripple***
- ***No Matching Network Required for Operating at 50Ω***
- ***Ultra Miniature Ceramic DCC6C SMD Package***
- ***Complies with Directive 2002/95/EC (RoHS Compliant)***

SF5914

ABSOLUTE MAXIMUM RATING (T_A=25°C)			
Parameter		Rating	Unit
Input Power Level	P_{in}	+10	dBm
DC Voltage	V_{DC}	0	V
Operating Temperature Range	T_A	-30 ~ +85	°C
Storage Temperature Range	T_{stg}	-45 ~ +85	°C

ELECTRONIC CHARACTERISTICS						
Parameter		Sym	Minimum	Typical	Maximum	Unit
Nominal Frequency (at 25°C) (Center frequency between 3dB point)		f_C	NS	866.00	NS	MHz
Insertion Loss	851.00 … 869.00 MHz	IL	-	2.0	3.5	dB
3dB Bandwidth		BW_3	-	-	-	MHz
Amplitude Ripple (p-p)	851.00 … 869.00 MHz	$\Delta\alpha$	-	0.8	1.5	dB
Input VSWR	851.00 … 869.00 MHz	-	-	1.5	2.0	-
Output VSWR	851.00 … 869.00 MHz	-	-	1.5	2.0	-
Absolute Attenuation	DC … 809.00 MHz	α_{rel}	50	-	-	dB
	809.00 … 827.00 MHz	α_{rel}	45	-	-	dB
	827.00 … 839.00 MHz	α_{rel}	20	35	-	dB
Frequency Aging	Absolute Value during the First Year	$\|fA\|$	-	-	10	ppm/yr
DC Insulation Resistance Between any Two Pins		-	1.0	-	-	MΩ
Input / Output Impedance (nominal)		-	-	50	-	Ω

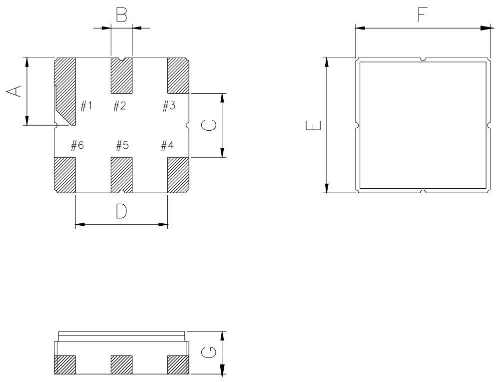
NS = Not Specified

Notes:

1. The frequency f_C is defined as the midpoint between the 3dB frequencies.
2. Unless noted otherwise, all measurements are made with the filter installed in the specified test fixture that is connected to a 50Ω test system with VSWR ≤ 1.2:1. The test fixture L and C are adjusted for minimum insertion loss at the filter center frequency, f_C. Note that insertion loss, bandwidth, and passband shape are dependent on the impedance matching component values and quality.
3. Unless noted otherwise, specifications apply over the entire specified operating temperature range.
4. The specifications of this device are based on the test circuit shown above and subject to change or obsolescence without notice.
5. All equipment designs utilizing this product must be approved by the appropriate government agency prior to manufacture or sale.
6. Our liability is only assumed for the Surface Acoustic Wave (SAW) component(s) per se, not for applications, processes and circuits implemented within components or assemblies.
7. For questions on technology, prices and delivery please contact our sales offices or e-mail sales@vanlong.com.

Phone: +86 (10) 5820 3910 Fax: +86 (10) 5820 3915 Email: sales@vanlong.com Web: http://www.vanlong.com

PACKAGE DIMENSIONS (DCC6C)



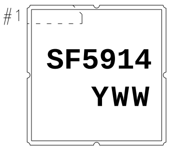
Electrical Connections

Terminals	Connection
2	Input
5	Output
1,3,4,6	Case Ground

Package Dimensions

Dimensions	Nom (mm)	Dimensions	Nom (mm)
A	1.5	E	3.0
B	0.6	F	3.0
C	1.5	G	1.1
D	1.8		

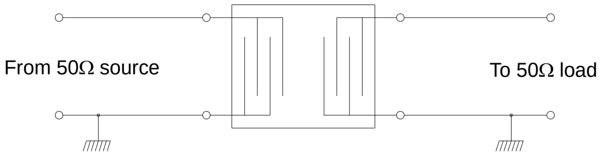
MARKING



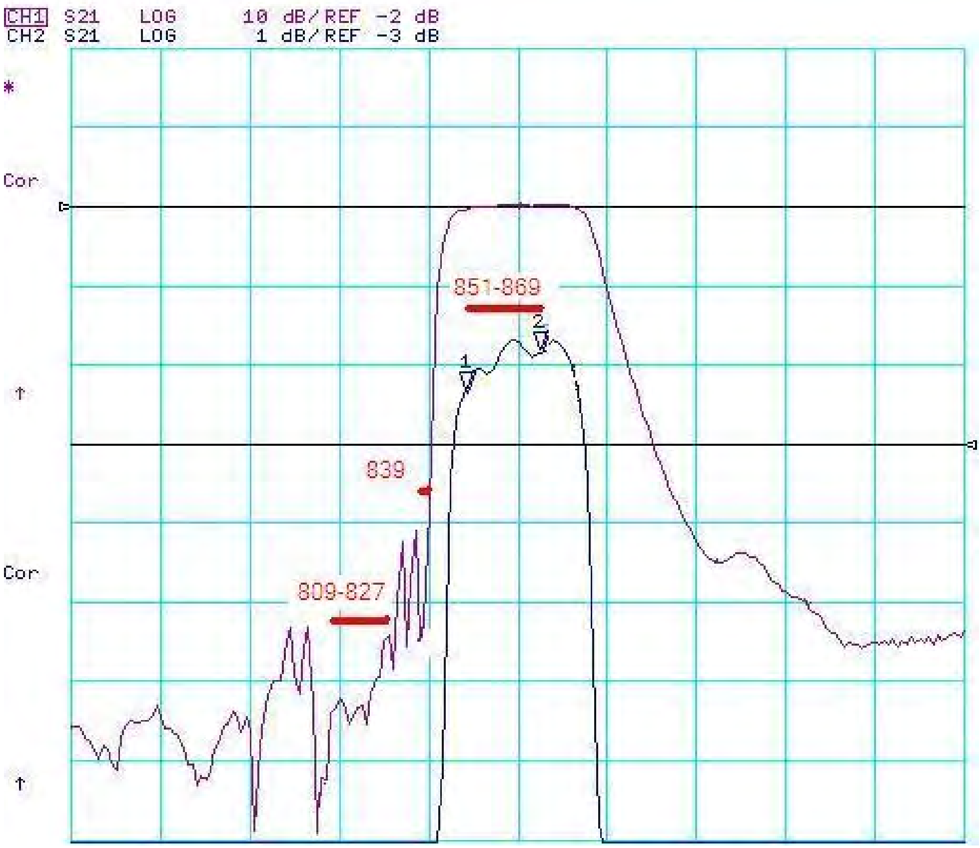
Laser or ink marking

1. SF5914 - Part Code
2. Date Code:
   Y : Last digit of year
   WW : Week No.

TEST CIRCUIT



TYPICAL FREQUENCY RESPONSE

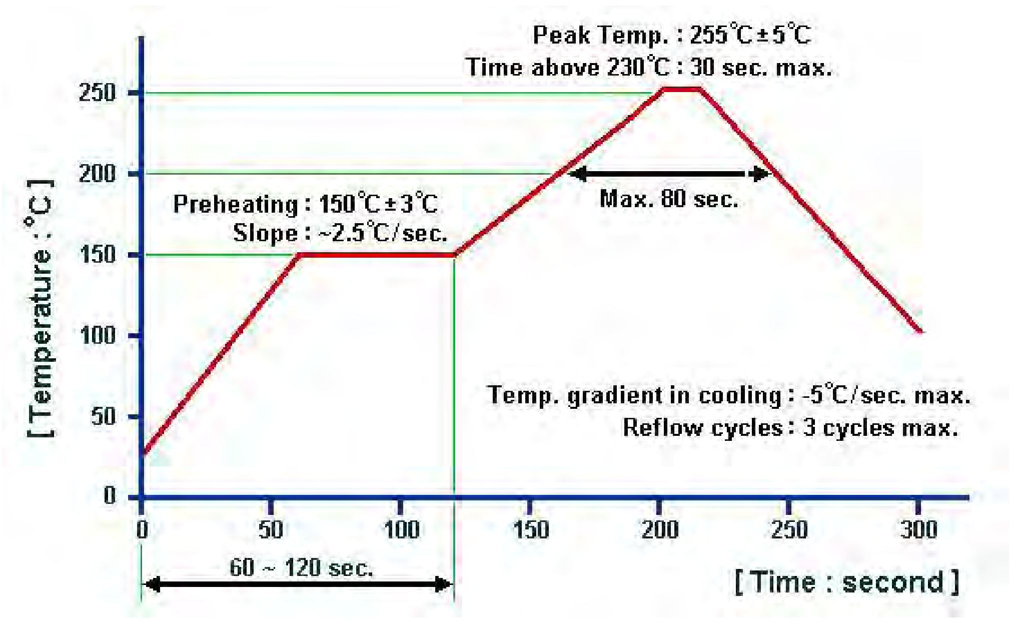


Phone: +86 (10) 5820 3910 Fax: +86 (10) 5820 3915 Email: sales@vanlong.com Web: http://www.vanlong.com

 April 09, 2010

ENVIRONMENTAL CHARACTERISTICS		
Item	Condition of Test	Requirements
Random Drop	The Filter shall be measured after 3 times random drops from the height of 1.0M on concrete floor.	No visible damage and the measured values shall meet the Electronic Characteristics
Vibration	The Filter shall be measured after being applied vibration of amplitude of 1.5mm with 10 to 55Hz bands of vibration frequency to each of 3 perpendicular directions for 1 hour.	
Lead Pulling Test	Weight along with the direction of lead without any shock 1.0 Kg.	
Lead bending Test	Lead shall be subject to withstand against 90 bending at its stem. This operation shall be done toward both directions.	
Resistance to Soldering Heat	Lead terminals are immersed up to 1.5mm from the Filter's body in solder bath of 270°C ± 10°C for 10 ± 1 seconds, and then the Filter shall be measured after being placed in natural condition for 2 hour.	
Solderability	Lead terminals are immersed in resin for 5 seconds and then immersed in soldering bath of 270°C ± 10°C for 2 ± 0.5 seconds.	
High Temperature	After being placed in a chamber with +85°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Low Temperature	After being placed in a chamber with -40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Humidity	After being placed in a chamber with 90 to 95% R.H. at +40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Heat Shock	After being kept at room temperature, the Filter shall be placed at temperature of -40°C for 30 minutes, then the Filter shall be immediately placed at temperature of 85°C, after 30 minutes at temperature of 85°C, the Filter shall be returned to -40°C again. After 5 times above cycles, the Filter shall be returned to room temperature, after 2 hour in natural condition, the Filter shall be measured.	

REFLOW SOLDERING TEMPERATURE PROFILE



DATA SHEET

SKY16602-632LF: Low-Threshold PIN Diode Limiter 0.2 to 4.0 GHz

Applications

- Cellular infrastructure
- WLAN, WiMAX
- Receiver LNA protection
- Test instruments

Features

- Optimized for 0.2 to 4.0 GHz operation
- Low limiting threshold (+5 dBm typical)
- Low insertion loss
- Low distortion
- Integrated PIN limiter and Schottky diodes, and DC blocks
- MLP (2-pin, 2.3 x 2.3 mm) Pb-free package, (MSL1, 260°C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

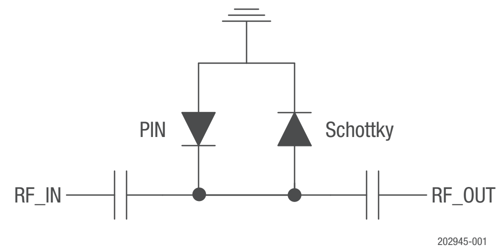


Figure 1. SKY16602-632LF Block Diagram

Description

The SKY16602-632LF is a fully integrated PIN diode low-threshold limiter module in a surface-mount package. It is designed for use as a passive receiver protector in wireless or other RF systems for frequencies up to 4 GHz. It features a low limiting threshold, low-insertion loss, and low distortion in a single Micro Lead-frame Package (MLP).

The SKY16602-632LF module is comprised of a PIN limiter diode, a Schottky diode, and 2 DC blocking caps at the RF ports in a 2-lead MLP. The small package design reduces printed circuit board area. The module can be tuned using external surface mount technology (SMT) components for optimal narrow band performance over the 0.2 to 4.0 GHz operating range.

The module can operate over the temperature range of –40°C to +85°C.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

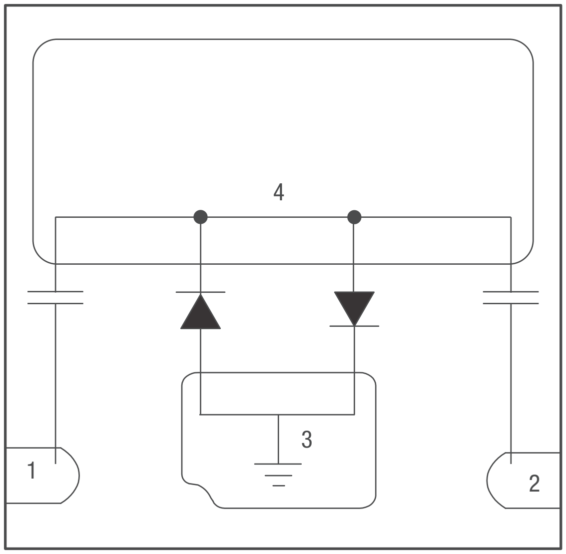


Figure 2. SKY16602-632LF Pinout (Top View)

Table 1. SKY16602-632LF Signal Descriptions

Pin	Name	Description
1	RF_IN	RF input, AC coupled.
2	RF_OUT	RF output, AC coupled.
3	GND	Must be connected to chassis ground
4	PAD	Exposed pad **(must be isolated from ground)**

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY16602-632LF are provided in Table 2. Electrical specifications for the un-tuned limiter module are provided in Table 3, and typical performance characteristics are illustrated in Figures 4 and 5. Electrical specifications for the 2.45 GHz tuned limiter module are provided in Table 4, and typical performance characteristics are illustrated in Figures 6 and 7.

Figures 8 and 9 show the power derating curves for the limiter. In Figure 8, the temperature is referenced to the bottom of the QFN package. The power derating curve with the temperature referenced to the bottom of the printed circuit board is shown in Figure 9.

Table 2. SKY16602-632LF Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Unit
RF input power (CW) at T_{CASE} = 85°C	P_{IN}		12	W
RF input power (1 μs pulse, 10% duty cycle) at T_{CASE} = 85°C	P_{IN}		120	W
CW power dissipation at T_{CASE} = 85°C	P_{DIS}		0.4	W
Storage temperature	T_{STG}	–65	150	°C
Operating temperature	T_{OP}	–40	85	°C
Electrostatic discharge:	ESD			
Charged-Device Model (CDM), Class 4			1000	V
Human Body Model (HBM), Class 1B			250	V
Machine Model (MM), Class A			150	V

[1] Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: *Although these devices are designed to be as robust as possible, electrostatic discharge (ESD) can damage them. These devices must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be employed at all times.*

Table 3. SKY16602-632LF Electrical Specifications (Untuned Circuit, Reference Figure 1)
(T_{OP} = 25°C, Z_O = 50 Ω, as Measured in Skyworks Evaluation Board Optimized for Operation at 0.2 to 4.0 GHz, Unless Otherwise Noted)

Parameter	Symbol	Condition	Frequency	Min.	Typ.	Max.	Units
Reverse voltage	V_R					20	V
Forward current	I_F					50	mA
Insertion loss	I_L	P_{IN} = 0 dBm	0.90 GHz		0.3	0.5	dB
Return loss	R_L	P_{IN} = 0 dBm	0.90 GHz		14		dB
Threshold level	T_L	P1dB	0.90 GHz	5.3	6.0	6.7	dBm
Saturated CW input power[1]	P_{IN_CW}		0.90 GHz		30		dBm
Flat leakage power[2]	F_L	P_{IN} = +10 dBm	0.90 GHz		6		dBm
Recovery time[3]	t_R		0.90 GHz		5		ns
Thermal resistance	θ_{JC}	Junction-to-case			114		°C/W

[1] Saturated CW input power is defined as the point where the diode series resistance does not change with the rectified current. As the input power increases past this point, output power will increase until the diode reaches its max power limit.

[2] Flat leakage power is defined as the power level after the limiter has fully turned on and the output pulse reaches a constant level.

[3] Recovery time represents the transition time from the high-loss to low-loss state following the removal of high-power input. RF pulse modulation: 1 μs pulse width and 0.1% duty factor.

Theory of Operation

A limiter prevents overload by allowing RF signals that are below a certain threshold to pass through, but larger signals exceeding the threshold are increasingly attenuated. The SKY16602-632LF has a lower threshold level over a traditional self-bias limiter circuit with an inductor for a ground return. It accomplishes this by adding a basic PIN limiter diode (Pin 1) in parallel to a Schottky diode (Pin 2). The low turn on voltage of the Schottky diode reduces the threshold level while the PIN limiter diode protects the Schottky diode at higher power levels. Therefore, for maximum RF power handling, the RF input signal is required to be connected to Pin 1. The two internal DC input/output capacitors provide DC blocking needed for most applications.

Tuned Circuit

The module may be RF tuned for optional RF match and insertion loss centered at a target frequency within its normal band of operation. This is done with the use of external surface mount components. The schematic diagram in Figure 3 shows the SKY16602-632LF limiter with a shunt connected capacitor and inductor tuned for 2.45 GHz. The bill of materials for the 2.45 GHz tuned circuit is shown in Table 4. Electrical specifications for the 2.45 GHz tuned limiter module are provided in Table 5.

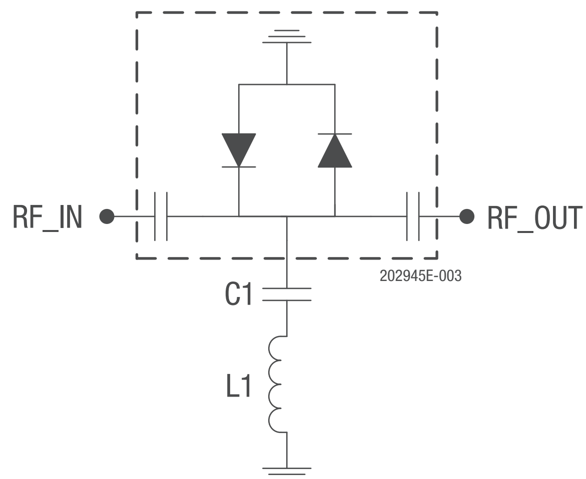


Figure 3. SKY16602-632LF Schematic with External Tuning Networks Optimized for 2.45 GHz

Table 4. Evaluation Board Bill of Materials for EN33-D946-001 (2.45 GHz Tuned Circuit)

Component	Value	Size	Manufacturer	Mfg. Part Number	Characteristics
C1	15 pF	0402	Murata	GRM1555C1H150J	C0G, 50 V
L1	2.2 nH	0402	Taiyo Uden	HK10052N2S	300 mA, R = 0.13 Ω

Table 5. SKY16602-632LF Electrical Specifications (Tuned to 2.45 GHz Operation, Reference Figure 3)
(T_{OP} = 25°C, Z_O = 50 Ω, as Measured in Skyworks Evaluation Board Optimized for Operation at 2.45 GHz, Unless Otherwise Noted)

Parameter	Symbol	Condition	Frequency	Min.	Typ.	Max.	Units
Insertion loss	I_L	P_{IN}= 0 dBm	2.45 GHz		0.5		dB
Return loss	R_L	P_{IN}= 0 dBm	2.45 GHz		25		dB
Threshold level	T_L	P1dB	2.45 GHz		5		dBm
Saturated CW input power[1]	P_{IN_CW}		2.45 GHz		23		dBm
Flat leakage power[2]	F_L	P_{IN} = +10 dBm	2.45 GHz		4		dBm
Input third order intercept	IIP3	P_{IN} = –10 dBm/tone, spacing = 10 MHz	2.45 GHz		21		dBm
Recovery time[3]	t_R		2.45 GHz		5		ns
Thermal resistance	θ_{JC}	Junction to case			114		°C/W

1 Saturated CW input power is defined as the point where the diode series resistance does not change with the rectified current. As the input power increases past this point, output power will increase until the diode reaches its max power limit.

2 Flat leakage power is defined as the power level after the limiter has fully turned on and the output pulse reaches a constant level.

3 Recovery time represents the transition time from the high-loss to low-loss state following the removal of high-power input. RF pulse modulation: 1 μs pulse width and 0.1% duty factor.

Typical Performance Characteristics

(TOP=25 °C, Characteristic Impedance = 50 Ω)

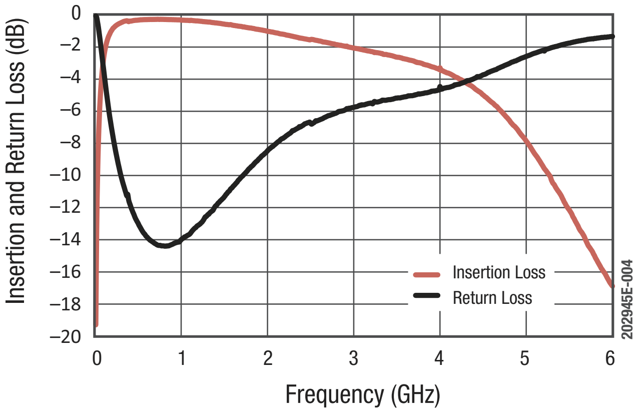


Figure 4. Small Signal Performance without External Tuning

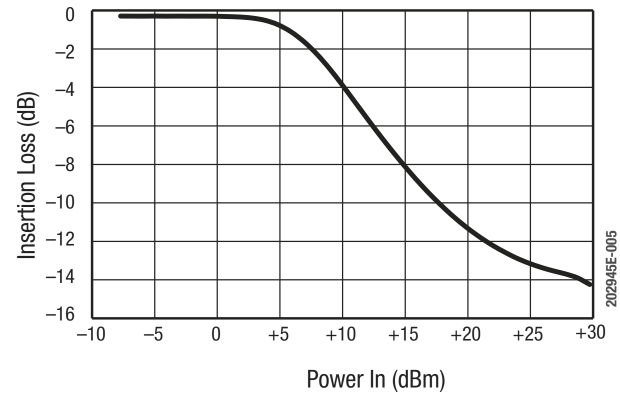


Figure 5. Insertion Loss vs CW Input Power at 0.90 GHz without External Tuning

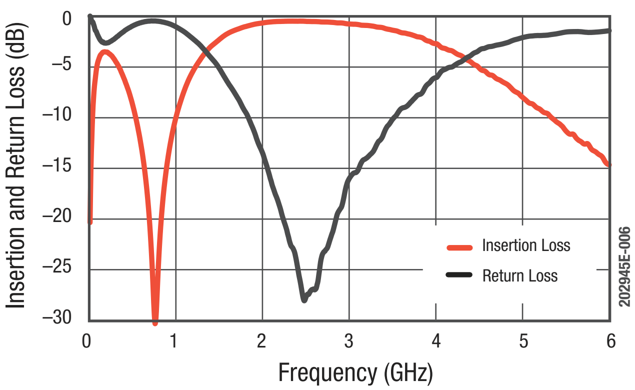


Figure 6. Small Signal Performance with External Tuning Networks Optimized for 2.45 GHz

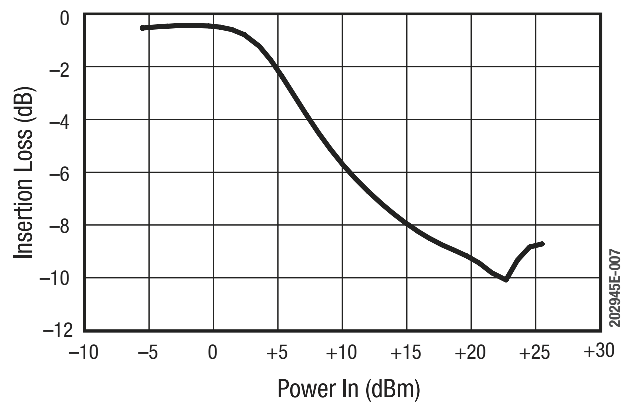


Figure 7. Insertion Loss vs CW Input Power at 2.45 GHz (Tuned Circuit)

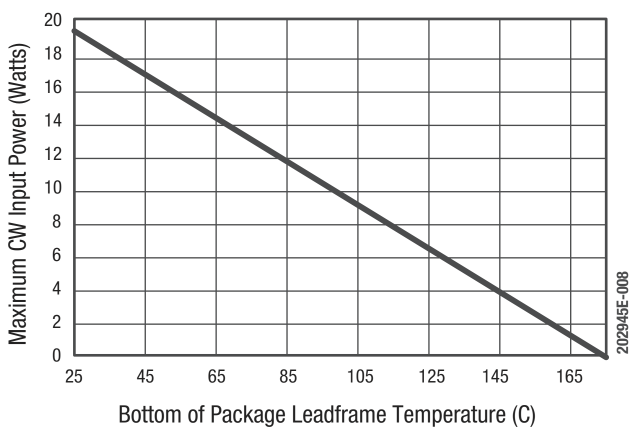


Figure 8. Power Derating Curve (Insertion Loss = 0.3 dB) vs Temperature on Bottom of Package Leadframe

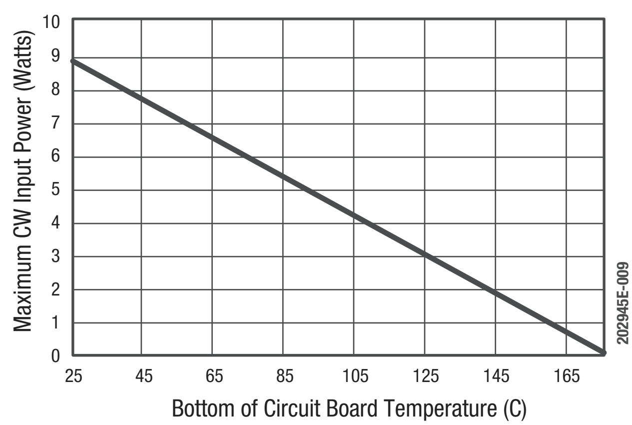


Figure 9. Power Derating Curve (Insertion Loss = 0.3 dB) vs Temperature on Bottom of EVB Circuit Board

Evaluation Board Description

The SKY16602-632LF evaluation boards are used to test the performance of the limiter. Assembly drawings for the evaluation boards are shown in Figures 10 and 11. The evaluation board layer detail is provided in Figure 12.

Package Dimensions

The PCB layout footprint for the SKY16602-632LF is shown in Figure 13. Typical part markings are noted in Figure 14. Package dimensions are shown in Figure 15, and tape and reel dimensions are provided in Figure 16.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY16602-632LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, Solder Reflow Information, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

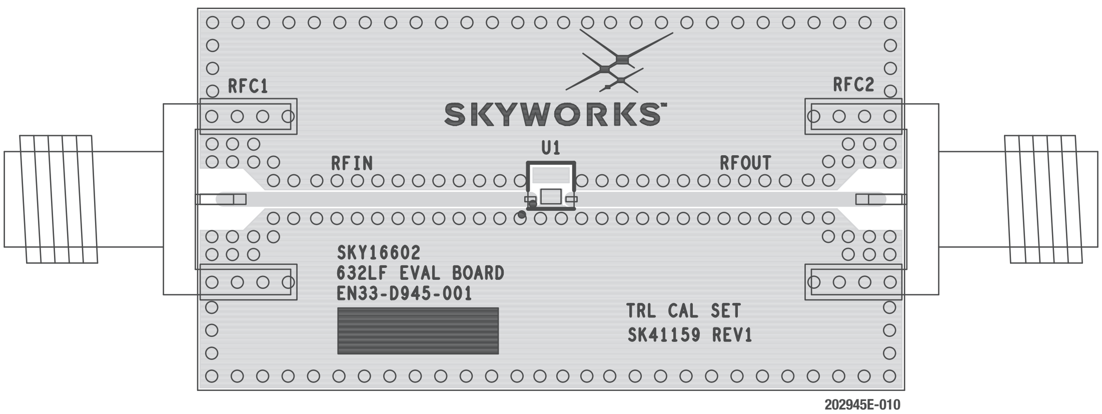


Figure 10. SKY16602-632LF Evaluation Board Assembly Diagram

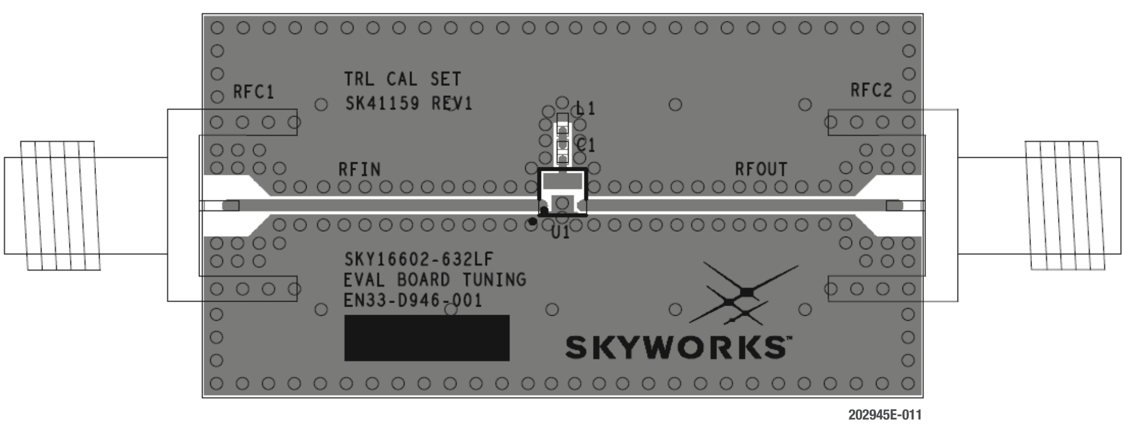
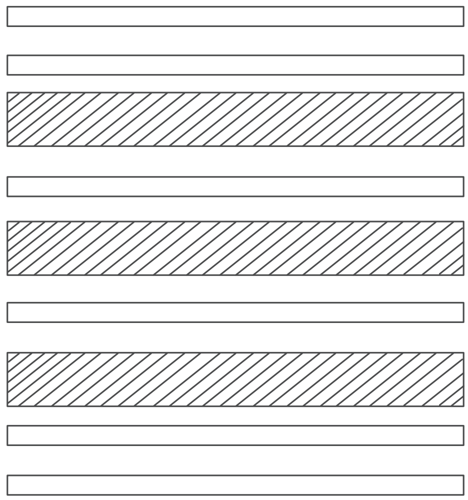


Figure 11. SKY16602-632LF Evaluation Board Assembly Diagram (Tuned Circuit)

Cross Section



Name	Thickness (in)	Material
Top Solder mask		
L1	(0.0028)	Cu foil
Laminate	0.012 ± 0.0006	Rogers RO4003C Core
L2	(0.0014)	Cu foil
Laminate	(Note 1)	FR4 Prepreg
L3	(0.0014)	Cu foil
Laminate	0.010 ± 0.0006	FR4 Core
L4	(0.0028)	Cu foil
Bottom Solder mask		

Note 1: Adjust this thickness to meet total thickness goal of 0.062 ± 0.005 inches.

202945E-012

Figure 12. Board Layer Detail Physical Characteristics

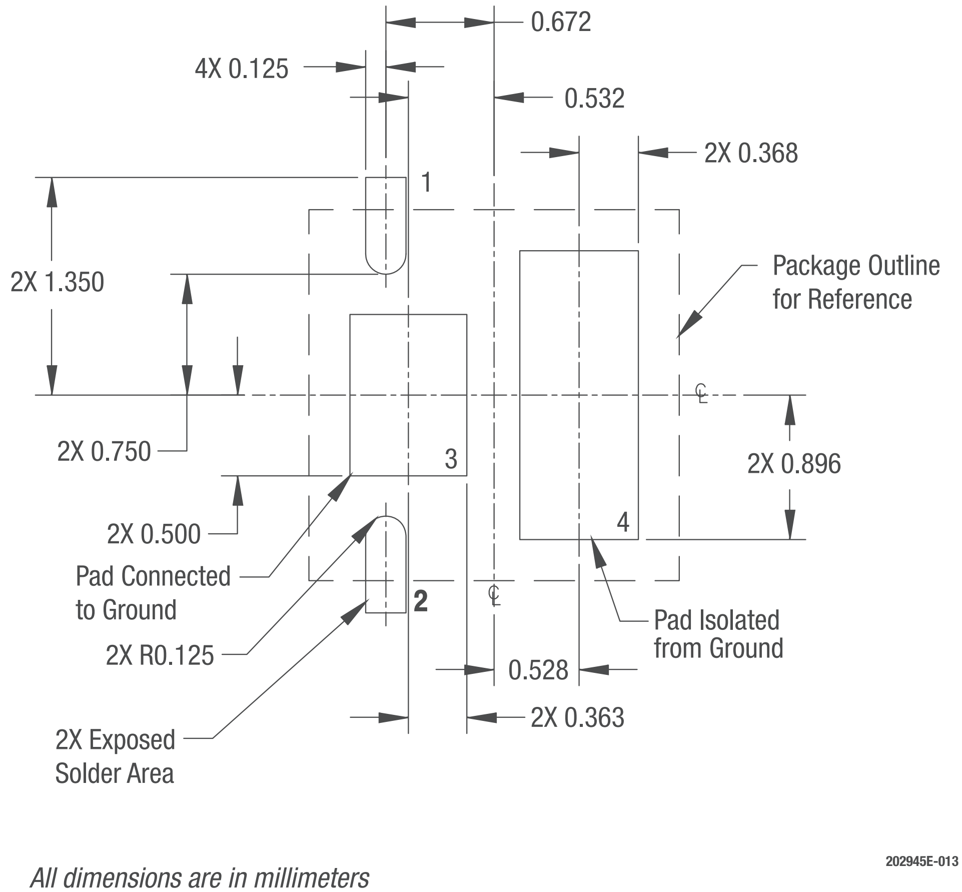


Figure 13. SKY16602-632LF PCB Layout Footprint

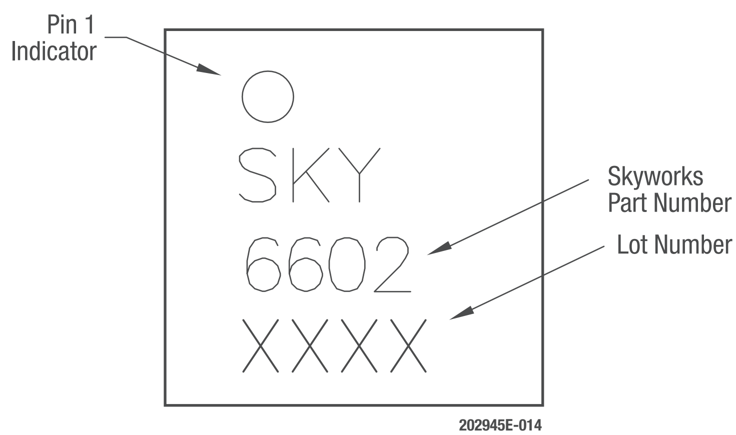
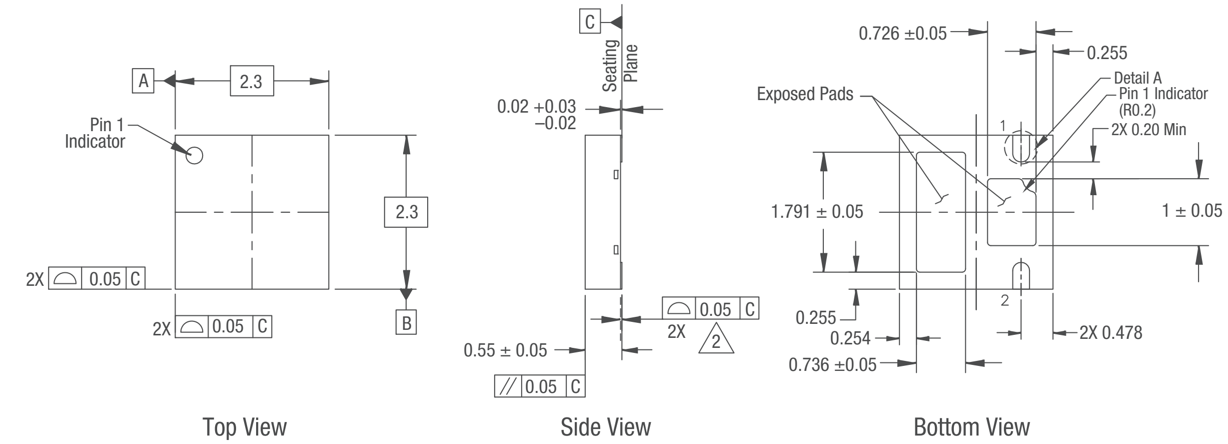
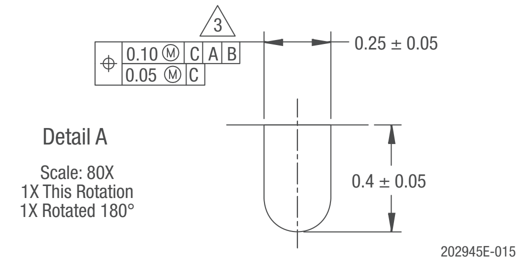


Figure 14. SKY16602-632LF Typical Part Markings

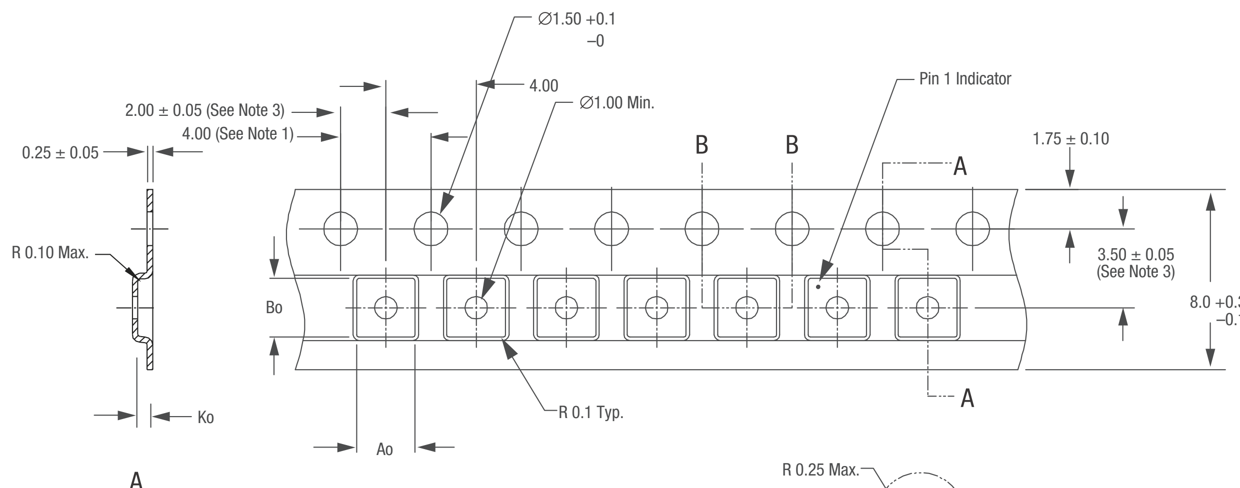




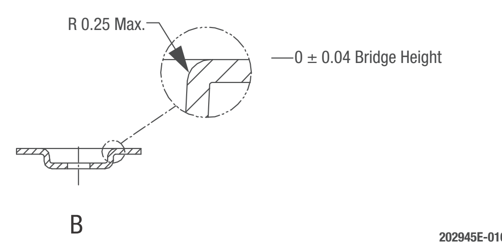
Notes:

1. *Dimensions and tolerances according to ASME Y14.5M-1994.*
2. *Coplanarity applies to the exposed heat sink slug as well as the terminals.*
3. *Dimension applies to metallized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that area.*
4. *Plating requirement per source control drawing (SCD) 2504.*
5. *All measurements are in millimeters.*

Figure 15. SKY16602-632LF Package Dimensions



Ao = 2.60 ± 0.05
Bo = 2.60 ± 0.05
Ko = 0.65 ± 0.05



Notes:

1. *10 sprocket hole pitch cumulative tolerance ±0.20 mm.*
2. *ESD surface resistivity shall be ≤ 1 x 10[10] Ohms/Square per EIA, JEDEC TNR specification.*
3. *Pocket position relative to sprocket hole measured as true position of pocket.*
4. *Ao and Bo are measured on a plane 0.30 mm above the bottom of the pocket.*
5. *Carrier tape: black conductive polycarbonate.*
6. *Cover tape material: transparent conductive material.*
7. *All measurements are in millimeters.*

Figure 16. SKY16602-632LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY16602-632LF: Low Threshold PIN Diode Limiter	SKY16602-632LF	SKY16602-632LF-EVB

Transko TA815BM

RoHS Compliant

- iDEN, RF-Tx SAW Filter
- Revision 1: January 2010

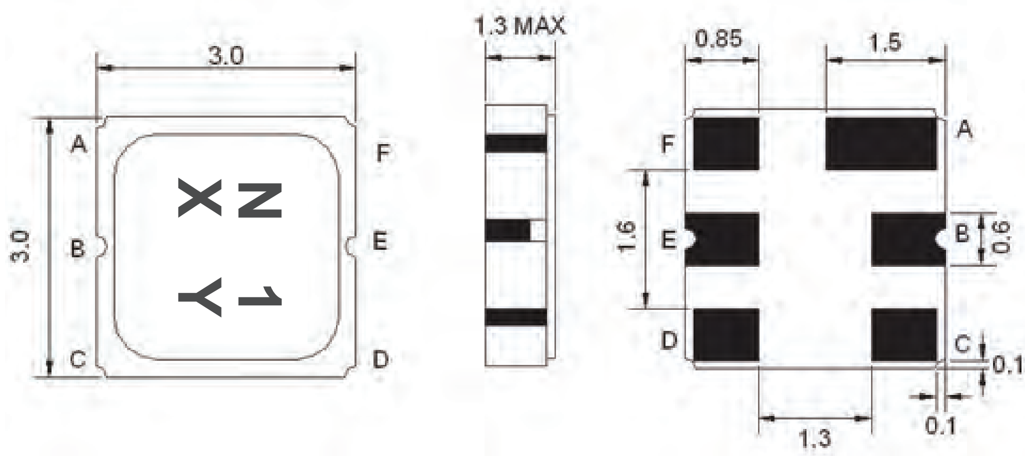
Electrical Characteristics

MAXIMUM RATING				
PARAMETERS DESCRIPTION	UNIT	MINIMUM	TYPICAL	MAXIMUM
Operating Temperature Range	°C	-40	-	+85
Storage Temperature Range	°C	-40	-	+85
Maximum DC Voltage	V	-	-	5
Maximum Input Power	dBm	-	-	20
Source Impedance (single ended)(1)	Ω	-	50	-
Load Impedance (single ended)(1)	Ω	-	50	-
Package type & size	M			
Length x Width	mm²	-	3.0 x 3.0	-
Height	mm	-	-	1.3

ELECTRICAL SPECIFICATION				
PARAMETERS DESCRIPTION	UNIT	MINIMUM	TYPICAL	MAXIMUM
Center Frequency (Fo)	MHz	-	815.5	-
Insertion Loss within 806 ~ 825 MHz	dB	-	2.4	3.5
Group delay ripple within 806 ~ 825 MHz	ns_{p-p}	-	15	30
Attenuation:				
851.0 ~ 866.0 MHz	dB	40	46	-
935.0 ~ 940.0 MHz	dB	35	40	-
960.65 ~ 979.65 MHz	dB	35	41	-
1115.30 ~ 1134.30 MHz	dB	37	42	-
1269.95 ~ 1288.95 MHz	dB	40	51	-
1612.0 ~ 1650.0 MHz	dB	35	43	-
1650.0 ~ 2600.0 MHz	dB	25	30	-
VSWR within 806 ~ 825 MHz	-	-	1.7	2.0

Notes: (1) No Matching Network (Ref. Testing Environment Circuit as shown below).

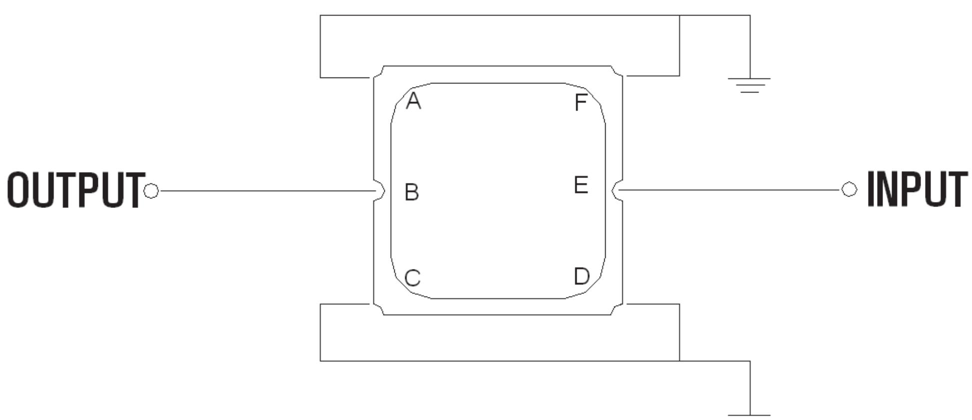
Package Dimensions



Marking Descriptions	
N	IDEN Application
1	Series Number
X	Date Code (Year)
Y	Date Code (Month)

Pin Description	
A, C, D, F	Ground
E	In
B	Out

Testing Environment

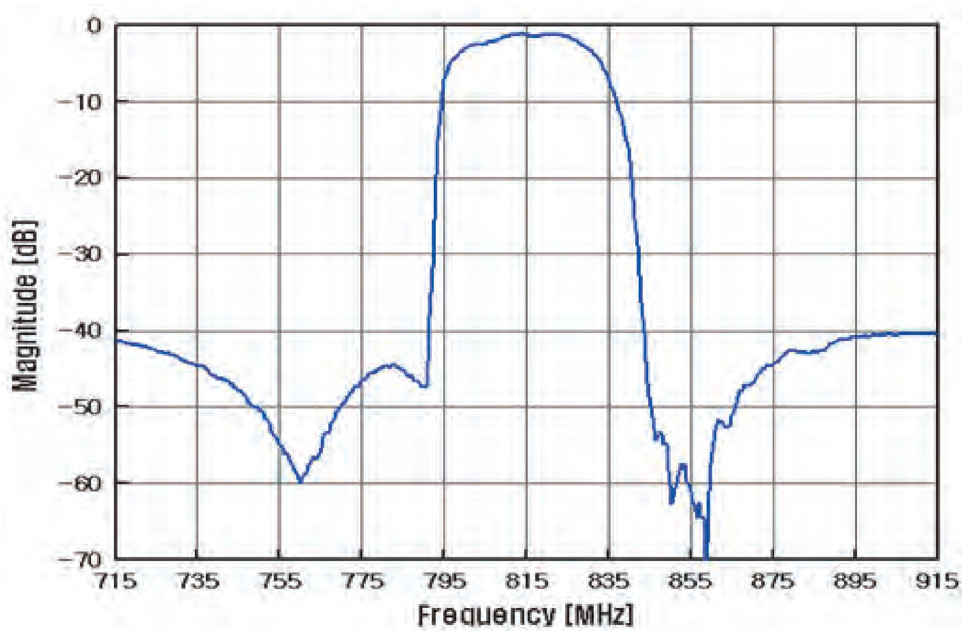


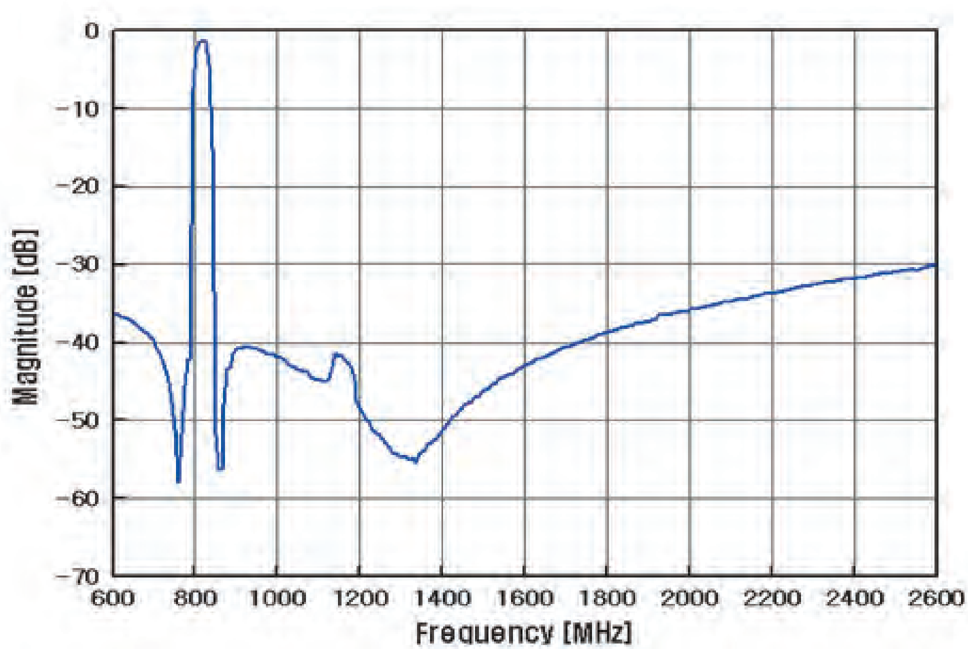
Source & Load Impedance: 50 Ω

Transko Electronics, Inc. 3981 E. Miraloma Ave., Anaheim CA 92806 USA
Tel: 714-528-8000 Fax: 714-528-8017 Website: www.transko.com E-mail: sales@transko.com

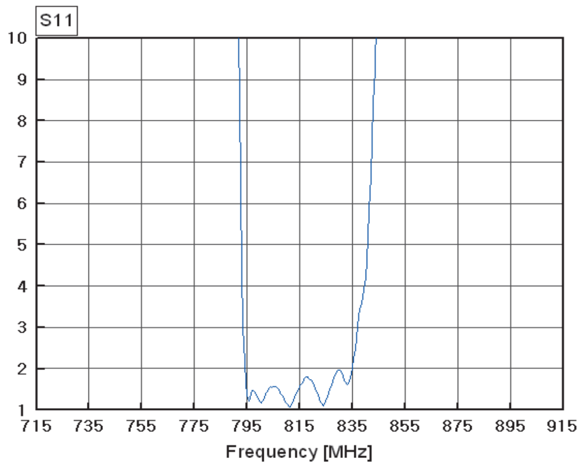
Frequency Characteristics

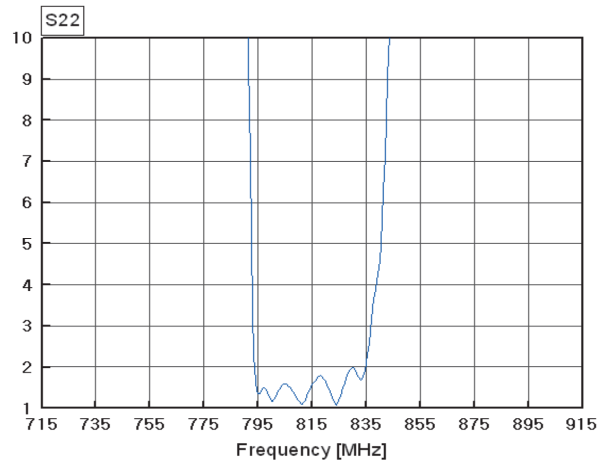
Frequency Response



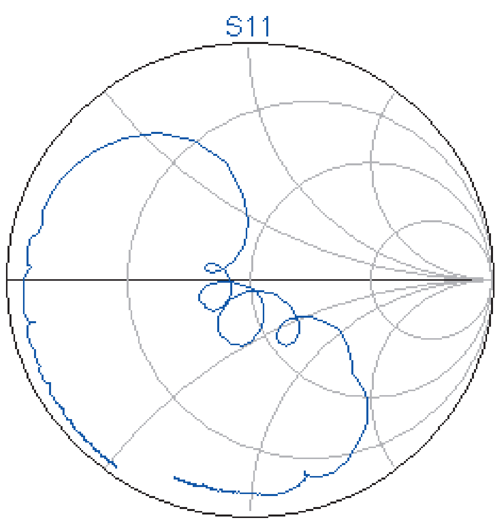


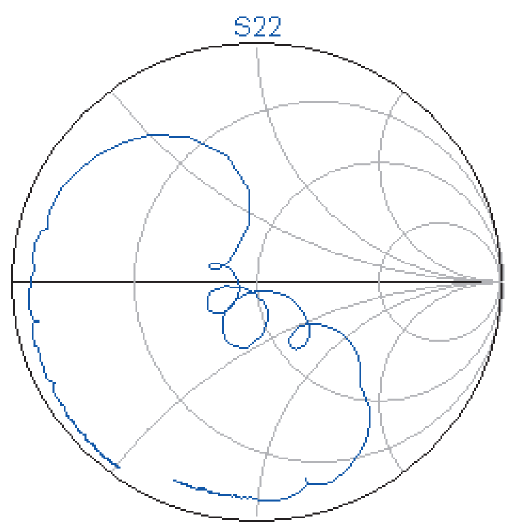
VSWR





Smith Chart





Applications

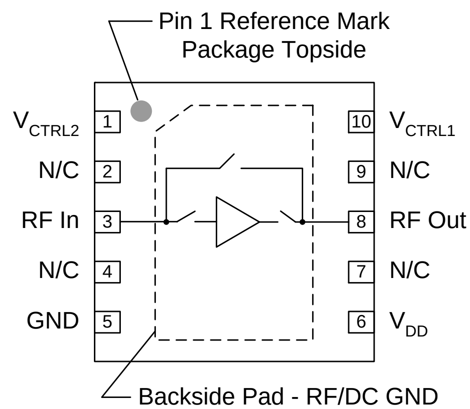
- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

10-pin 3 x 3 mm DFN Package

Product Features

- 500 – 2000 GHz Operational Bandwidth
- LNA with Integrated Bypass Mode
- Ability To Turn LNA and Bypass Mode OFF
- Ultra Low Noise, 0.42 dB at 900 MHz
- 19 dB Gain
- +36 dBm Output IP3
- +43 dBm Input IP3 in Bypass Mode
- Internally Matched
- Positive Supply Only, +3.3 to +5 V
- 3 x 3 mm 10-pin DFN Plastic Package

Functional Block Diagram



General Description

The TQL9042 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 900 MHz, the amplifier typically provides 19 dB gain, +36 dBm OIP3, and 0.42 dB noise figure while drawing 70 mA current from a +5 V supply. The component also provides high linearity in the bypass mode with +43 dBm IIP3.

The TQL9042 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The TQL9042 covers the 500 – 2000 MHz frequency band and is targeted for wireless infrastructure. The TQL9042 is packaged in a 3 x 3 mm and is pin compatible with the 1.5 – 2.7 GHz TQL9043 and 1.5 – 4.0 GHz TQL9044.

Pin Configuration

Pin No.	Label
1	V_{CTRL2}
2, 4, 7, 9	N/C
3	RFin
5	GND
6	V_{DD}
8	RFout
10	V_{CTRL1}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQL9042	500 – 2000 MHz Bypass LNA
TQL9042-PCB	Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
Drain Voltage (V_{DD})	+7 V
Input Power (CW)	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_{DD})	+3.3	+5.0	+5.25	V
Operating Temp. Range	−40		+105	°C
T_{ch} (for>10^6 hrs MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.=+25 °C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		2000	MHz
Test Frequency			900		MHz
Gain	Bypass OFF	17.5	19	20.5	dB
Input Return Loss	Bypass OFF		11		dB
Output Return Loss	Bypass OFF		20		dB
Noise Figure	Bypass OFF		0.42	0.8	dB
Output P1dB	Bypass OFF		+23		dBm
Output IP3	Bypass OFF, Pout=+5 dBm/tone, Δf=1 MHz	+30	+36		dBm
Insertion Loss	Bypass ON		1	1.9	dB
Return Loss	Bypass ON		13		dB
Input IP3	Bypass ON Pin=+6 dBm/tone, Δf=1 MHz		+43		dBm
Isolation	LNA OFF, Bypass OFF		-8.5		dB
Control Voltage, V_1, V_2 [(1)]	V_{IH}	2.4		V_{DD}	V
	V_{IL}	0		0.4	V
Current, I_d	Bypass OFF	40	70	110	mA
	Bypass ON		3	4.5	mA
Switching Speed [(2)]	Bypass to LNA Mode		483	900	ns
	LNA to Bypass Mode		400	800	ns
Thermal Resistance, θ_{jc}	Channel to case		100		°C/W

Notes:
1. The limits shown are true when using the external resistive divider values as shown on the Qorvo app board.
2. To achieve these fast switching speeds it is required to place a shunt 30K resistor at the RFout pin 8. Refer to pg. 6.

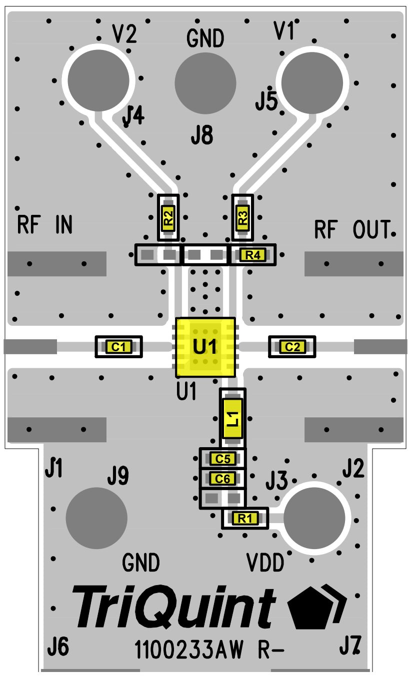
Control Truth Table

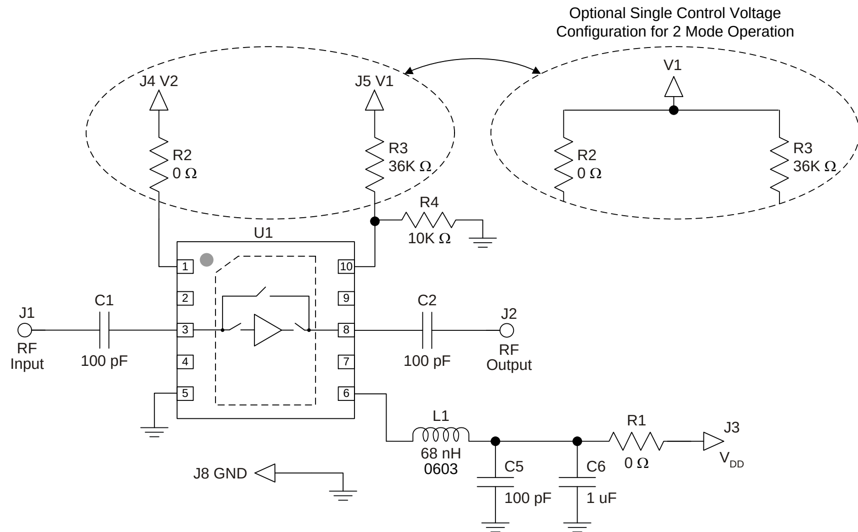
V_{CTRL2}	V_{CTRL1}	State
0	1	LNA OFF, Bypass OFF
1	1	LNA OFF, Bypass ON
0	0	LNA ON, Bypass OFF
1	0	Reserved (Do not use)

Control Voltage Limits (at device pins)

	State	Bias Condition
V_{CTRL1}	Low	≤ 0.1 V
	High	≥ 0.52 V
V_{CTRL2}	Low	≤ 0.4 V
	High	≥ 1.3 V

TQL9042-PCB Evaluation Board





See Evaluation Board PCB Information section for PCB material and stack-up.

C3 C4

Note:
If a TQL9042 application requires only two operational modes, LNA and bypass, the modes may be set using a single control voltage with the control lines tied together as shown above right. The corresponding truth table is shown below.

Control Truth Table – 2 Mode Operation

V_1	State
1	LNA OFF, Bypass ON
0	LNA ON, Bypass OFF

Bill of Material – TQL9042-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Bypass LNA	Qorvo	TQL9042
C1, C2, C3, C4, C5	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C6	1.0 uF	CAP, 0402, 10%, 10V, X5R	various	
R1, R2	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
R3	36K	RES, 0402, +/-5%, 1/10W	Various	
R4	10K	RES, 0402, +/-5%, 1/10W	Various	
L1	68 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-68NXJL

Power-up and Power-down Sequencing

		V_{DD}	V_{CTRL1} & V_{CTRL2}
LNA ON, Bypass OFF	Power-up	1st	2nd
	Power-down	1st	2nd
LNA OFF, Bypass ON	Power-up	1st	2nd
	Power-down	1st	2nd

Typical Performance (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D =70 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	700	800	900	1000	MHz
Gain	20.8	19.9	19.0	18.2	dB
Noise Figure	0.37	0.37	0.42	0.46	dB
Input Return Loss	9.6	10.2	10.8	11.4	dB
Output Return Loss	21.0	20.4	19.8	19.1	dB
Output P1dB	+23.1	+23.1	+23.1	+23.2	dBm
OIP3 (Pout/tone=+5 dBm, Δf = 1 MHz)	+35.3	+35.5	+36.0	+36.0	dBm

Typical Performance (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 3 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	700	800	900	1000	MHz
Insertion Loss	0.95	0.96	0.98	1.00	dB
Input Return Loss	12.5	12.6	12.7	12.6	dB
Output Return Loss	13.1	13.4	13.6	13.7	dB
Input IP3 (Pin/tone=+6 dBm, Δf = 1 MHz)	+41.2	+40.8	+43.0	+40.2	dBm

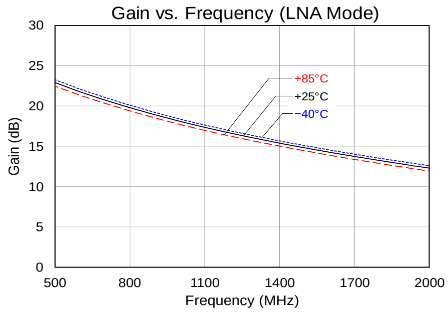
Typical Performance (LNA OFF, Bypass OFF Mode)

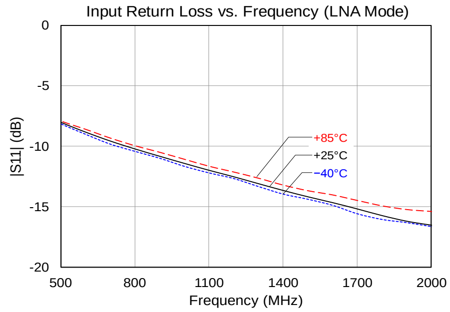
Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25 °C.

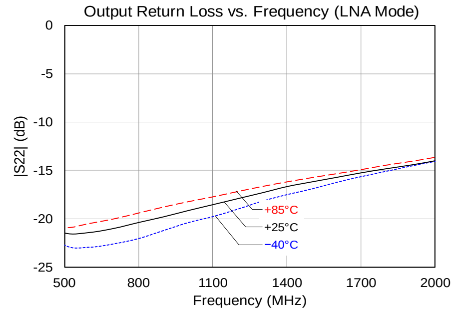
Parameter	Typical Value				Units
Frequency	700	800	900	1000	MHz
Isolation	6.6	7.4	8.2	8.8	dB

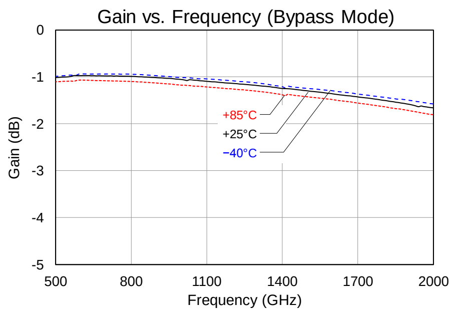
Performance Plots

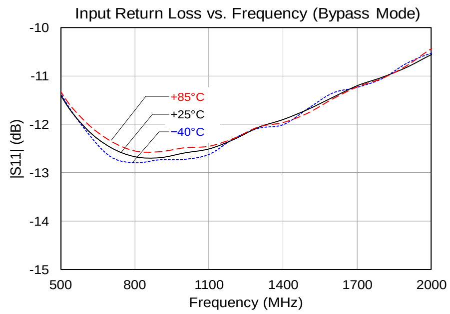
Test conditions unless otherwise noted: V_{DD} = +5 V, I_D =70 mA, Temp.=+25 °C

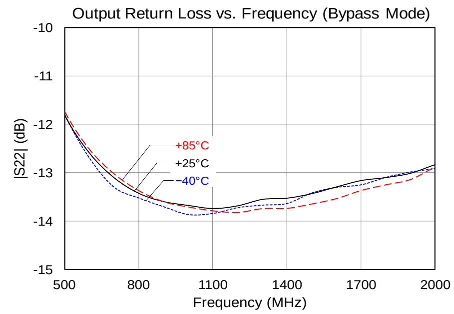


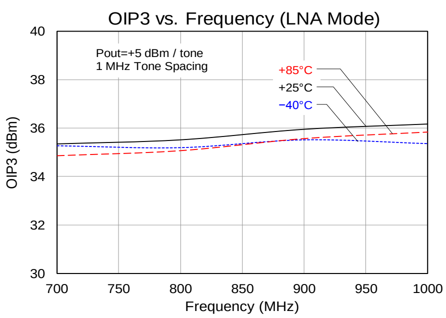


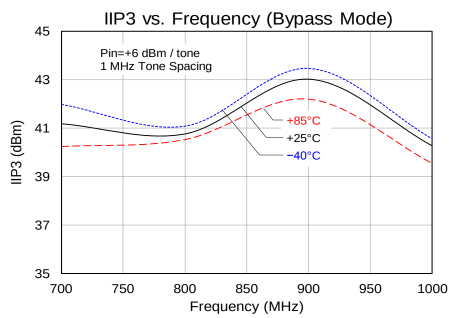


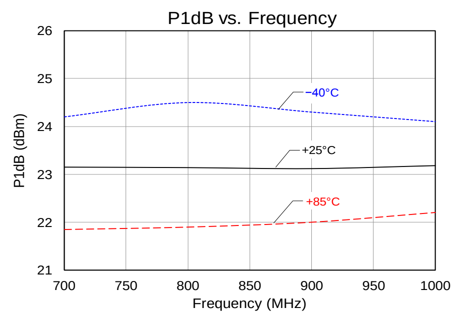


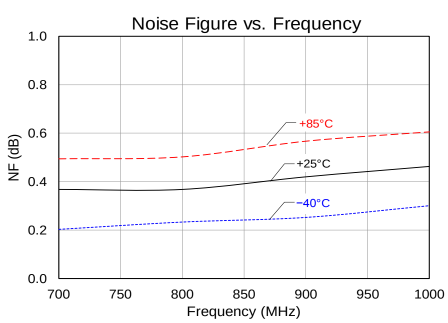


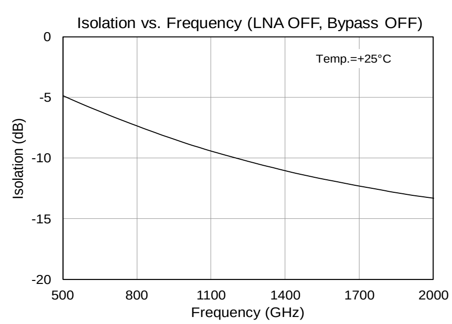




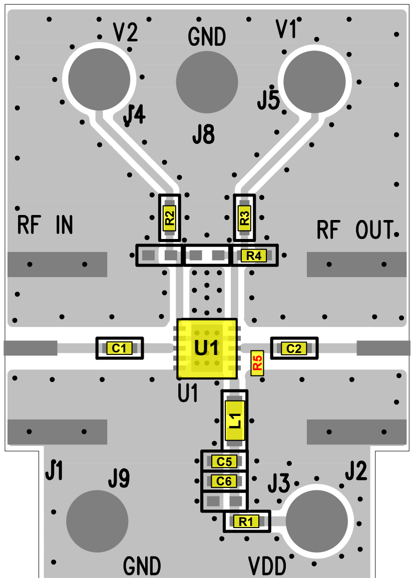


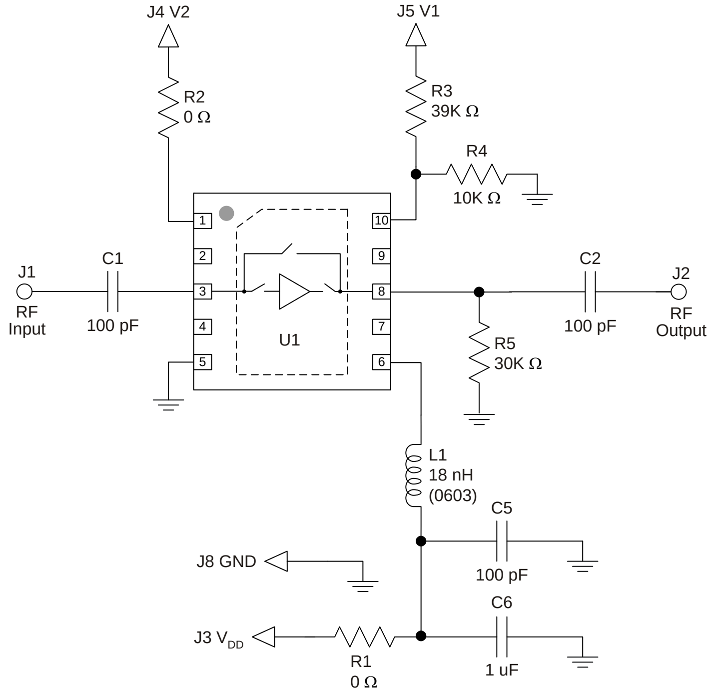






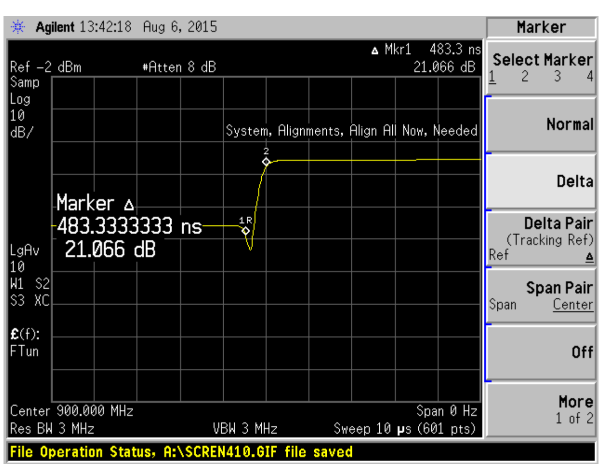
Switching Speed Application Note



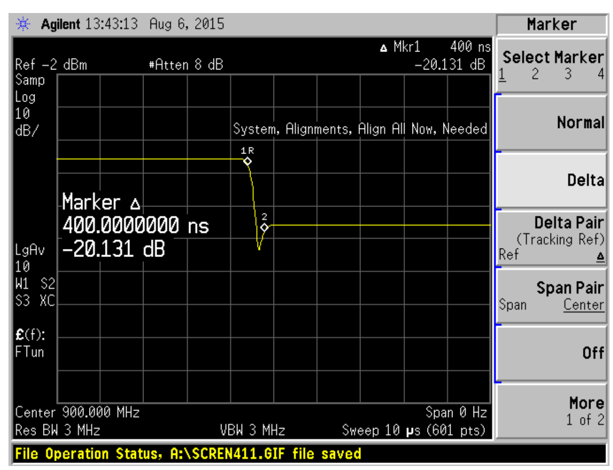


Transition	Value	Units
Bypass to LNA mode	483	ns
LNA to Bypass mode	400	ns

R5, valued 30K, is required to achieve the switching speeds listed above. The placement of R5 is shown on the Qorvo Evaluation Board above.

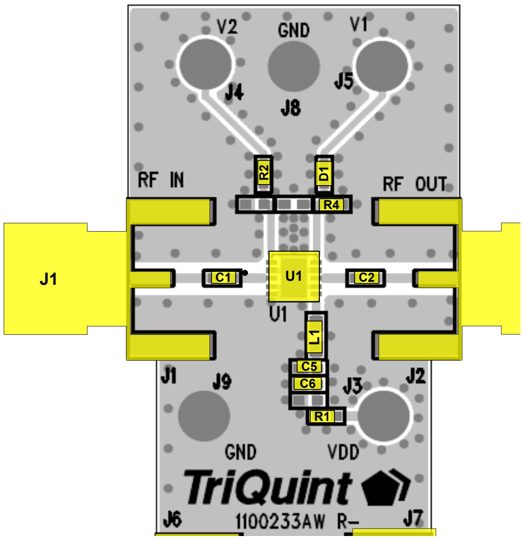


Bypass to LNA mode transition

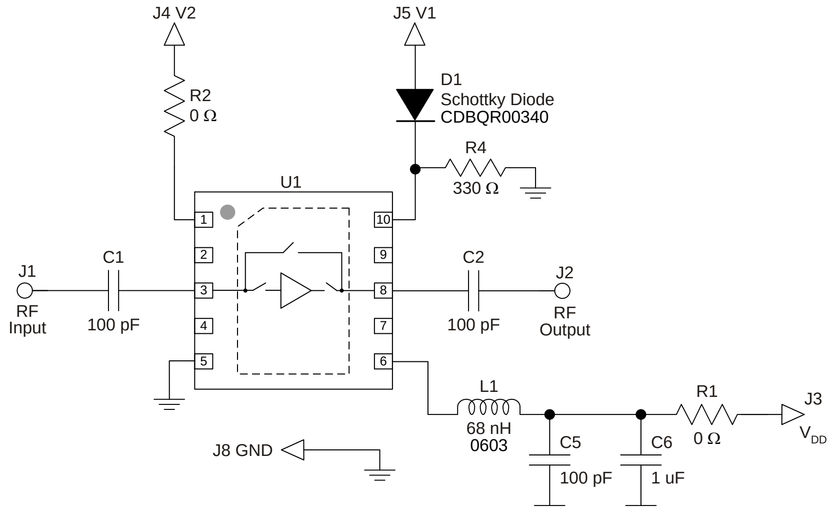


LNA to Bypass mode transition

TQL9042-PCB for 1.8V TTL Compatibility



See Evaluation Board PCB Information section for PCB material and stack-up.



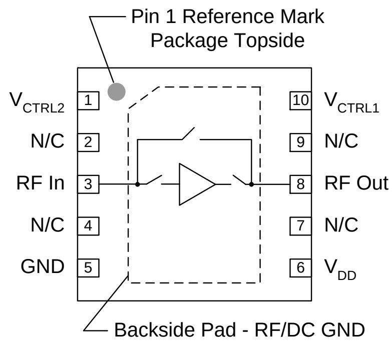
Note:
The control voltage limit for Vctrl1 shown in the table in the bottom right corner of pg. 2 cannot be met with a simple resistive divider network at pin 10 when using a 1.8V TTL logic level. A solution is to use a diode drop as shown above. This guarantees a voltage a pin 10 which is ≥0.52V.

Parameter	Conditions	Min		Max	Units
Control Voltage, V_1, V_2	V_{IH}	1.4		1.8	V
	V_{IL}	0		0.4	V

Bill of Material – TQL9042-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Bypass LNA	Qorvo	TQL9042
C1, C2, C3, C4, C5	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C6	1.0 uF	CAP, 0402, 10%, 10V, X5R	Various	
R1, R2	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
D1	n/a	Schottky Barrier Diode,	Comchip	CDBQR00340
R4	330 Ω	RES, 0402, +/-5%, 1/10W	Various	
L1	68 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-68NXJL

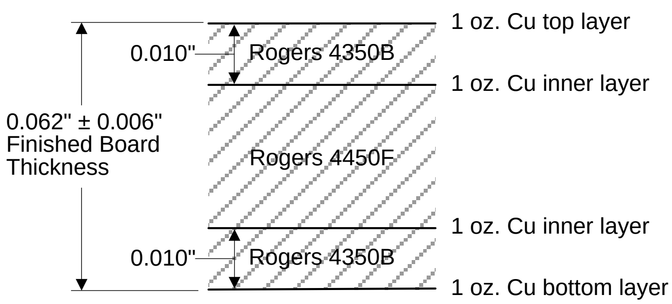
Pin Configuration and Description



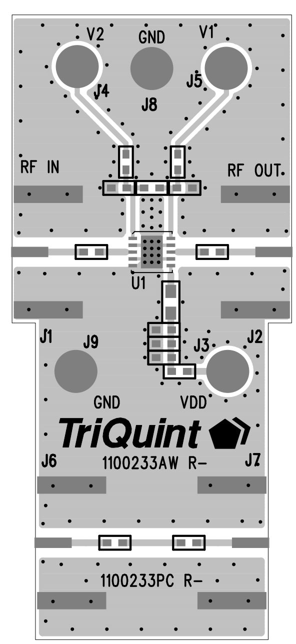
Pin No.	Label	Description
1	V_{CTRL2}	Control pin for bypass mode and LNA mode. Internal resistor divider. Refer to truth table.
2, 4, 7, 9	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
3	RFin	RF input pin. DC block required.
5	GND	RF/DC Ground pin.
6	V_{DD}	Supply voltage pin.
8	RFout	RF output pin. DC block required.
10	V_{CTRL1}	Control pin for bypass mode and LNA mode. Requires external resistor divider. Refer to truth table.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

Qorvo PCB 1100233 Material and Stack-up



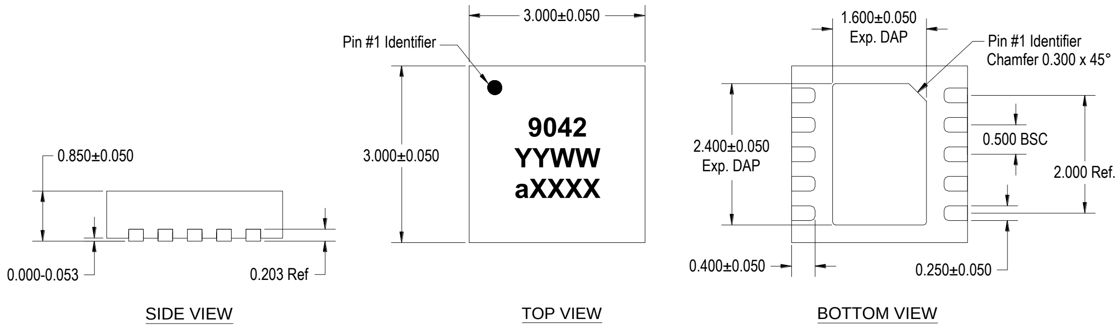
50 ohm line dimensions: width = .020”, spacing = .032”



Mechanical Information

Package Marking and Dimensions

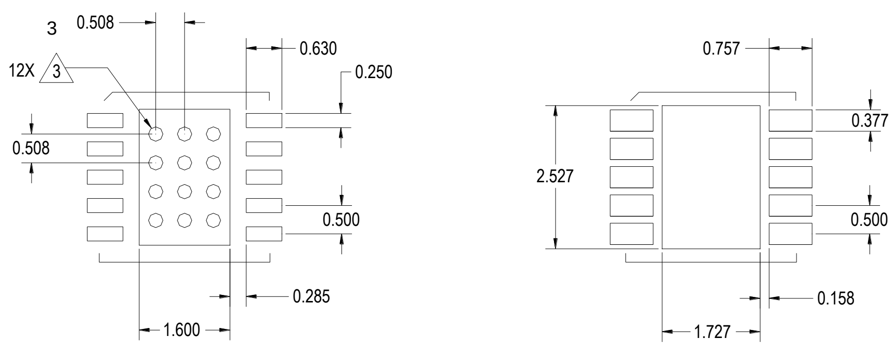
Marking: Part number – 9042
Year/Week – YYWW
Lot Code – aXXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥250V to 500V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.triquint.com **Tel: 877-800-8584**
Email: customer.support@qorvo.com

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

For technical questions and application information:

Email: sjcapplications.engineering@qorvo.com

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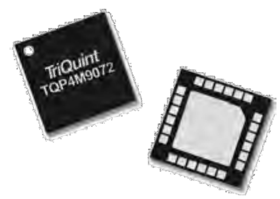
TQP4M9072

High Linearity 6-Bit, 31.5dB Digital Step Attenuator

Applications

- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- Test Equipments and Sensors
- IF and RF Applications
- General Purpose Wireless

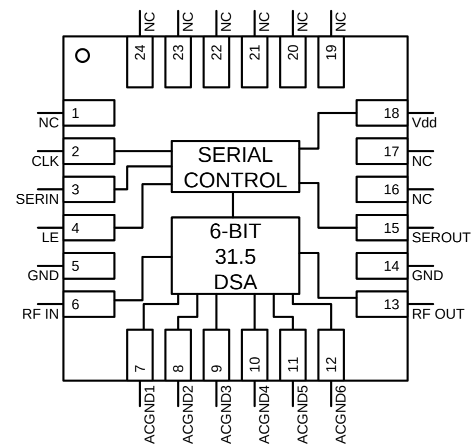


24-pin 4x4mm leadless QFN package

Product Features

- DC - 4 GHz
- 0.5 dB LSB Steps to 31.5 dB
- +57 dBm Input IP3
- 1.7 dB Insertion Loss @ 2.2 GHz
- Serial Control Interface
- No requirement for external bypass capacitors for operation above 700 MHz
- 50 Ω Impedance
- +5V Supply Voltage

Functional Block Diagram



General Description

The TQP4M9072 is a high linearity, low insertion loss, 6-bit, 31.5 dB Digital Step Attenuator (DSA) operating over the DC-4 GHz frequency range. The digital step attenuator uses a single positive 5V supply and has a serial periphery interface (SPI™) for changing attenuation states. This product maintains high attenuation accuracy over frequency and temperature. No external matching components are needed for the DSA. The product has an added feature of not requiring external AC ground capacitors for operation above 700 MHz.

The TQP4M9072 is available in a standard lead-free /green/RoHS-compliant 24-pin 4x4mm QFN package. The TQP4M9071 is also available from TriQuint as a footprint and pin compatible DSA equivalent with a parallel control interface

Pin Configuration

Pin #	Symbol
2	CLK
3	SERIN
4	LE
6	RF IN
13	RF OUT
15	SEROUT
18	Vdd
5, 14	GND
7, 8, 9, 10, 11, 12	ACGND1-ACGND6
Backside Paddle	Ground
All other pins are N/C	

Ordering Information

Part No.	Description
TQP4M9072	6-Bit, 31.5 dB DSA
TQP4M9072-PCB_ IF	40-500MHz Evaluation Board
TQP4M9072-PCB_RF	0.7-3.5GHz Evaluation Board

PCB includes USB control interface board, EVH.

Standard T/R size = 2500 pieces on a 13" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
Junction Temperature	150 °C
RF Input Power, 50Ω,T = 85ºC	+28 dBm
V_{dd}, Power Supply Voltage	+6.0 V
Digital Input Voltage	V_{dd} + 0.5V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	4.75	5	5.25	V
T (case)	-40		85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions: 25ºC, V_{dd} = +5V, 50Ω system, Mode 1, No external bypass capacitors used on pins 7-12.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range	See Note 1 and 2.	DC		4000	MHz
Insertion Loss	1.0 GHz		1.3		dB
	2.0 GHz		1.6		dB
	2.2 GHz		1.7	2.2	dB
	3.5 GHz		2.1		dB
Return Loss	All States		17		dB
Accuracy Error	0.04-2.7 GHz, All States, Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	0.7-2.7 GHz, All States, Mode 1 or Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	2.7-3.5 GHz, All States, Mode 1 or Mode 2	± (0.4 + 4% of Atten. Setting) Max			dB
Attenuation Step	To be monotonic (Step Attenuation ≥ 0)	0	0.5		dB
Input IP3	Input = +15dBm / tone, All States		+57		dBm
Input P0.1dB	All States, DC-4 GHz		+30		dBm
$Time_{rise / fall}$	10% / 90% RF		90		ns
$Time_{On}$, $Time_{Off}$	50% CTL to 10% / 90% RF		100		ns
Supply Voltage, Vdd			+5		V
Supply Current, Idd			2.0		mA

Notes:
1. In Mode 1 no external bypass capacitors are used and operating frequency is 0.7-4GHz. See page 8 for details.
2. In Mode 2 external bypass capacitors are used and operating frequency may be extended to 0.04-4GHz. See page 8 for details.

Serial Control Interface

The TQP4M9072 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SERIN) SPI™ input compatible. At power up, the serial control interface resets device attenuation state to 31.5dB. The 6-bit SERIN word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is disabled.

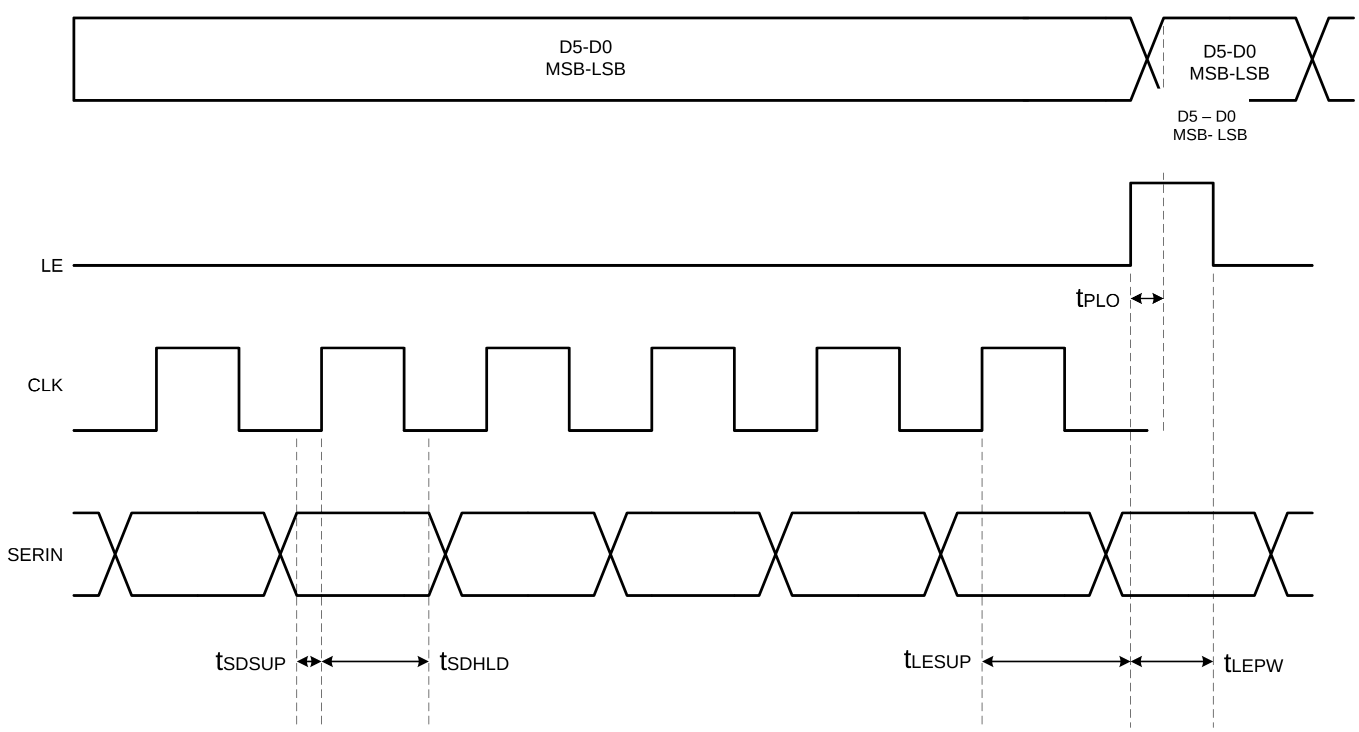
SERIN (MSB in First 6-Bit Word) Control Logic Truth Table

Test conditions: 25ºC, V_{dd} = +5V

6-Bit Control Word to DSA (LSB … MSB)						Attenuation State
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB
Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected						

Serial Control Interface Timing Diagram

CLK is disabled when LE is high



Serial Control Timing Characteristics

Test conditions: 25ºC, V_{dd} = +5V

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

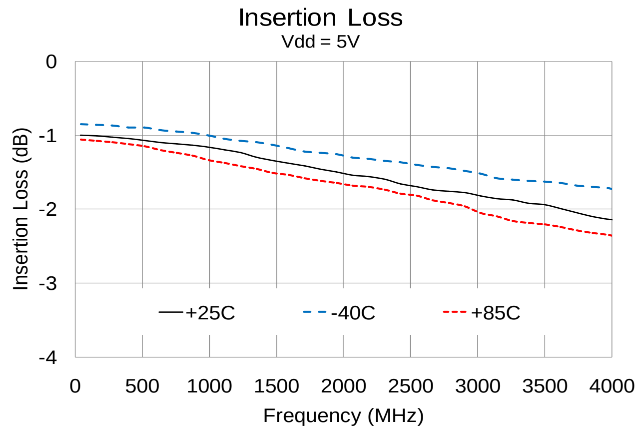
Serial Control DC Logic Characteristics

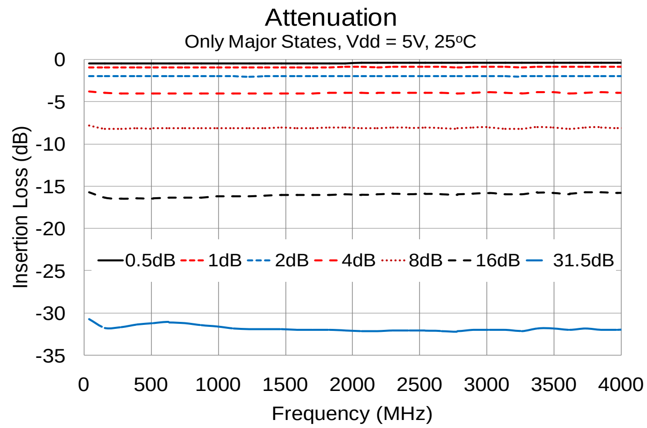
Test conditions: 25ºC, V_{dd} = +5V

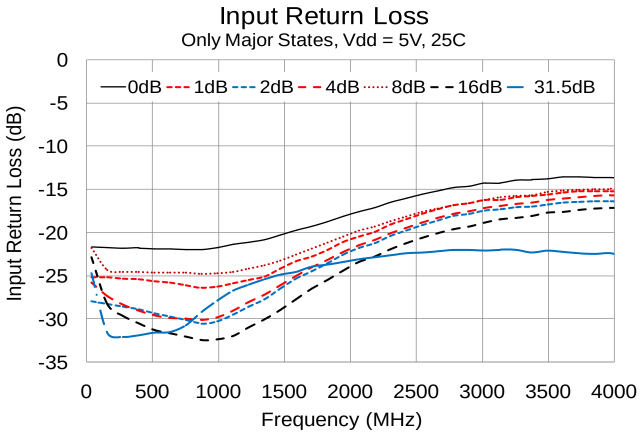
Parameter	Condition	Min	Max	Units
Input Low Voltage, V_{IL}		0	0.8	V
Input High Voltage, V_{IH}		2.4	Vdd	V
Output High Voltage, V_{OH}	On SEROUT	2.0	Vdd	V
Output Low Voltage, V_{OL}	On SEROUT	0	0.8	V
Input Current, I_{IH} / I_{IL}	On SERIN, LE and CLK	-10	+10	µA

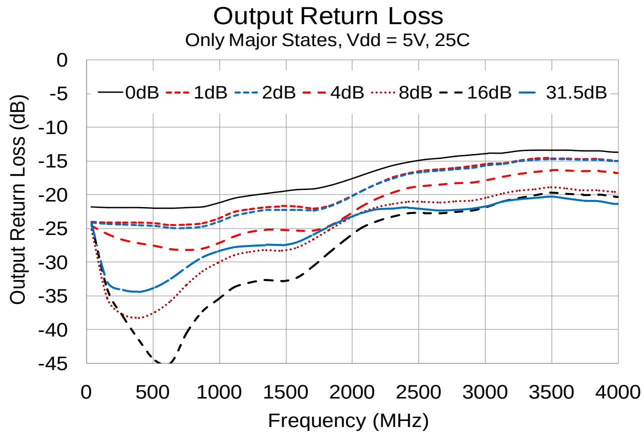
Typical Performance Data

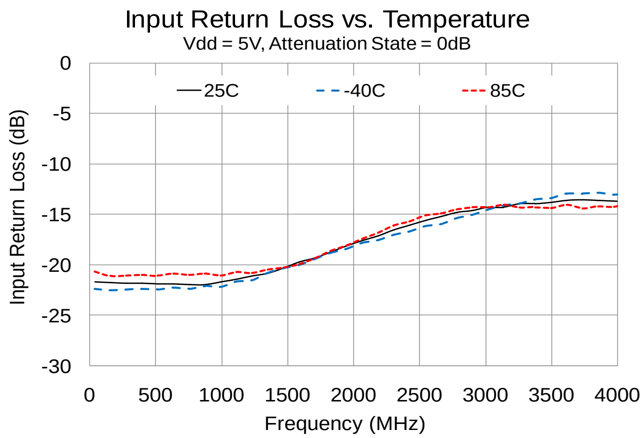
Performance plots data is measured using Bias Tee on RF ports in Mode 2 configuration. Mode 2 operation is required to obtain performance at frequencies lower than 0.7 GHz. For frequency range 0.7 - 4.0 GHz, data is identical in Mode 1 and Mode 2.

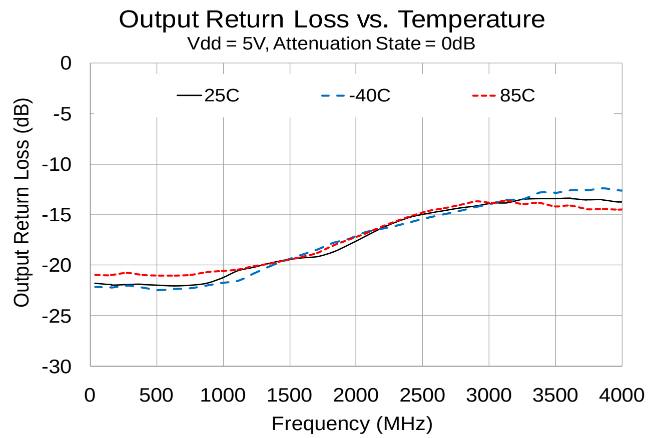




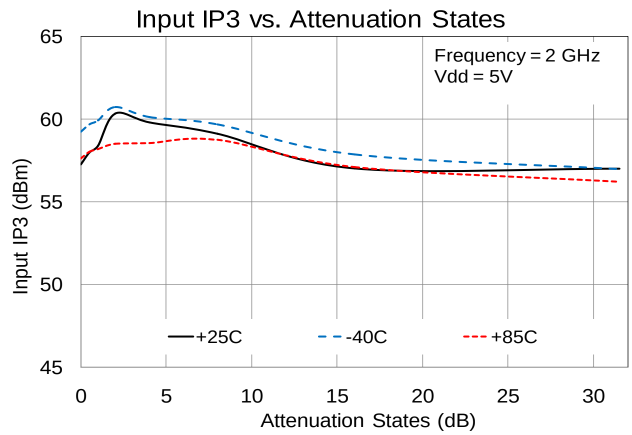


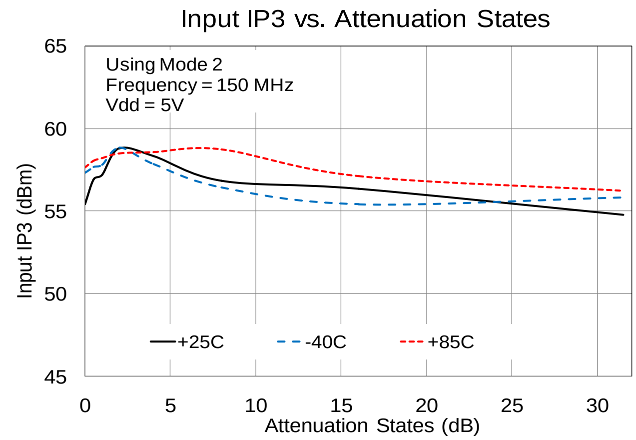


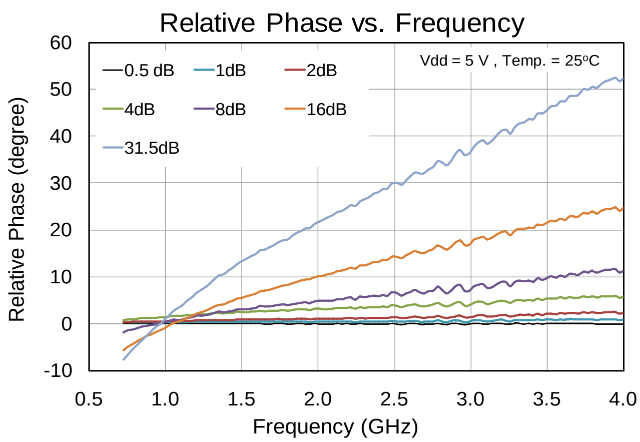


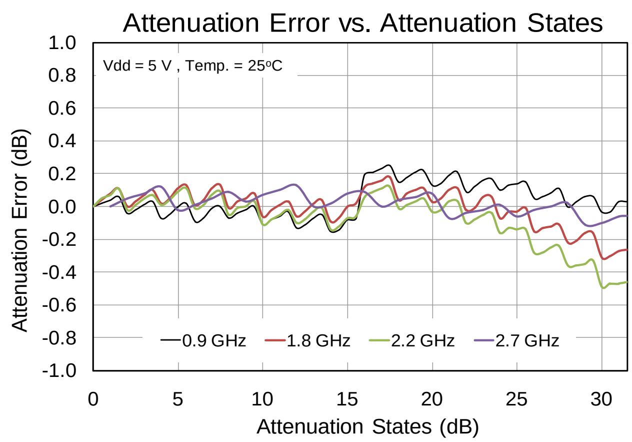


Typical Performance Data







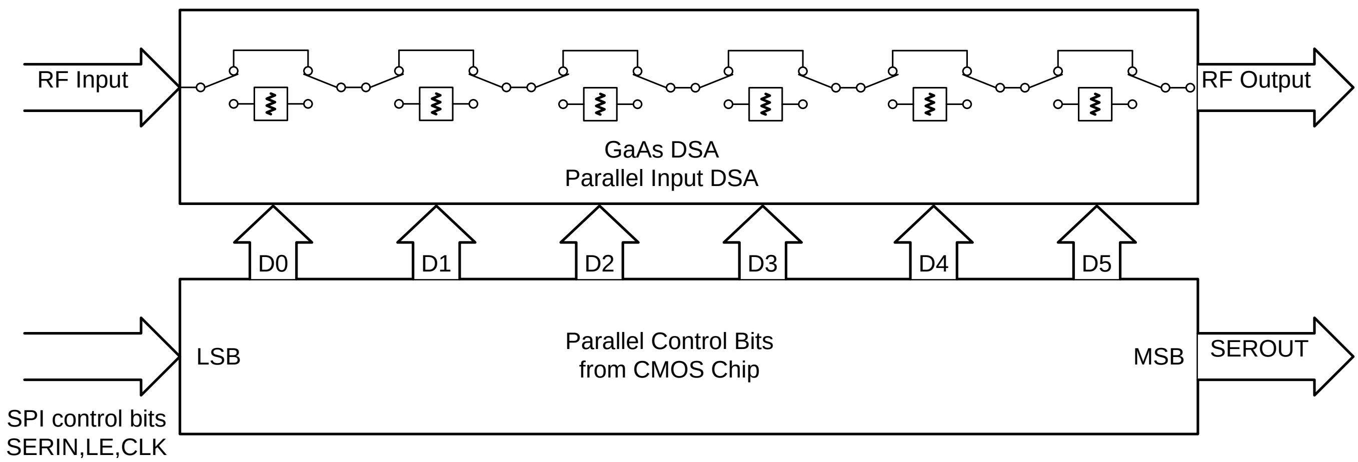


Detailed Device Description

The TQP4M9072 is a high linearity, low insertion loss, wideband, 6-bit, 31.5 dB digital step attenuator. The digital step attenuator uses a single 5V supply and has a CMOS SPI™ controller. This product maintains high attenuation accuracy over frequency and temperature. The product does not require any external bypass capacitors on AC ground pins for operation above 700 MHz. The DSA performance remains unchanged for frequency range 0.7 – 4 GHz in either Mode 1 or Mode 2. The operating frequency may be extended to low frequency range (0.04 – 0.7 GHz) with external bypass capacitors on AC ground pins (ACGND1-ACGND6).

Further assistance may be requested from TriQuint Applications Engineering, **sjcapplications.engineering@tqs.com**.

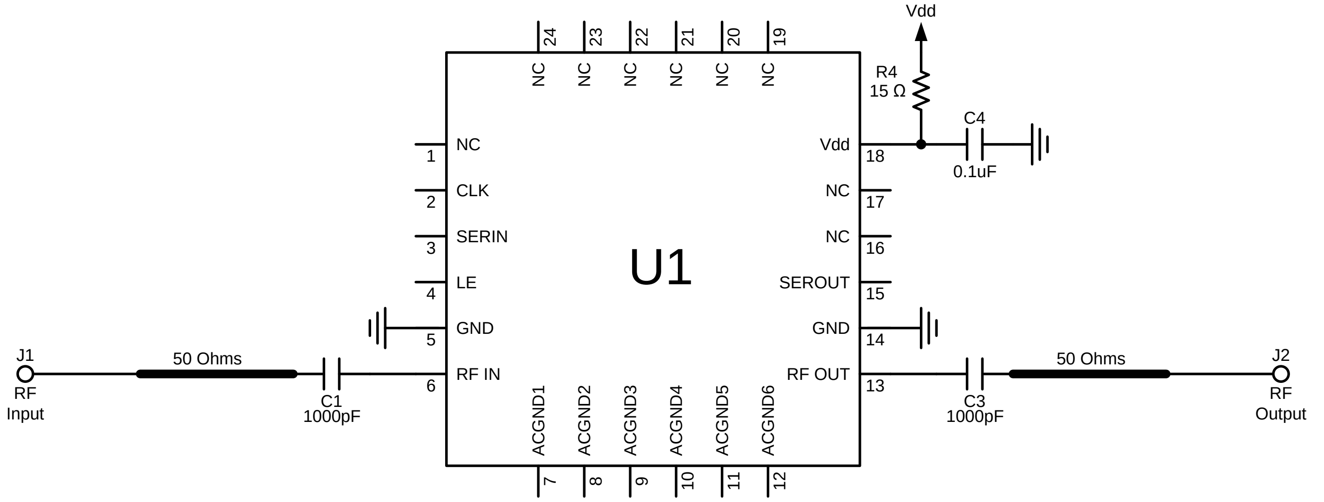
Functional Schematic Diagram



Detailed Device Description

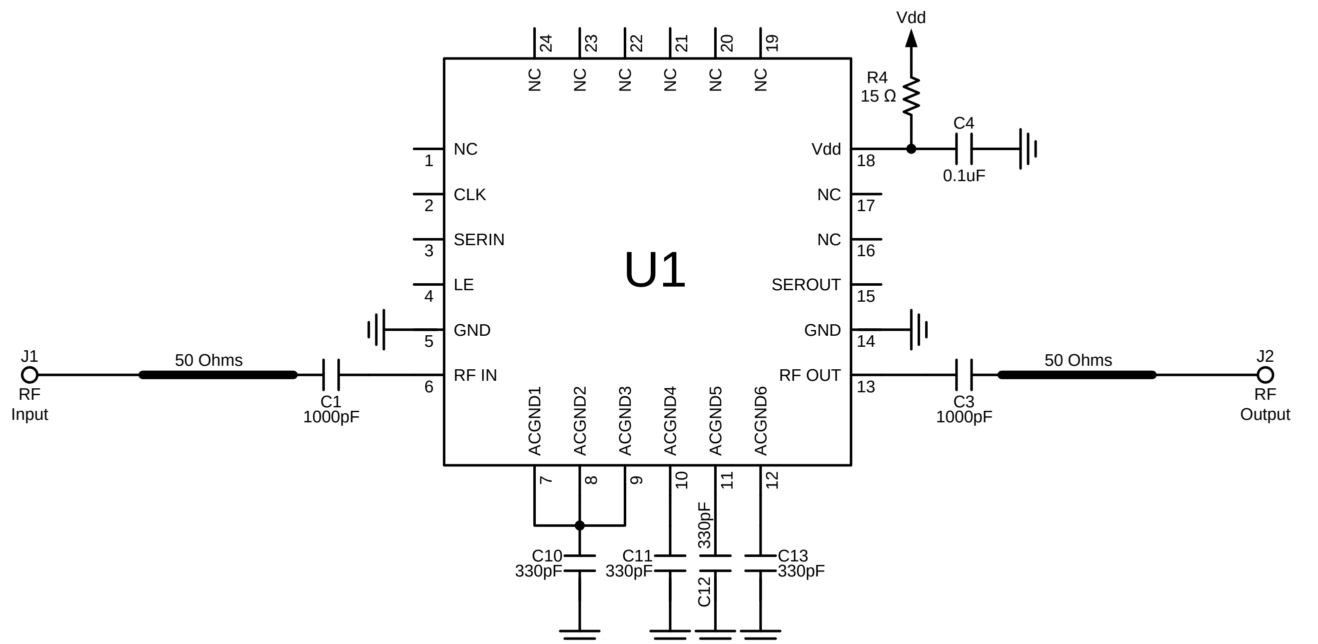
Mode 1: 0.7 - 4.0 GHz Operation (TQP4M9072-PCB_RF)

No external bypass capacitors required. There are 0.2 pF shunt capacitors (C5 and C7) next to RF connectors, on the application board, to resonate out the RF connector parasitic. These shunt capacitors are not required in the final application circuit.

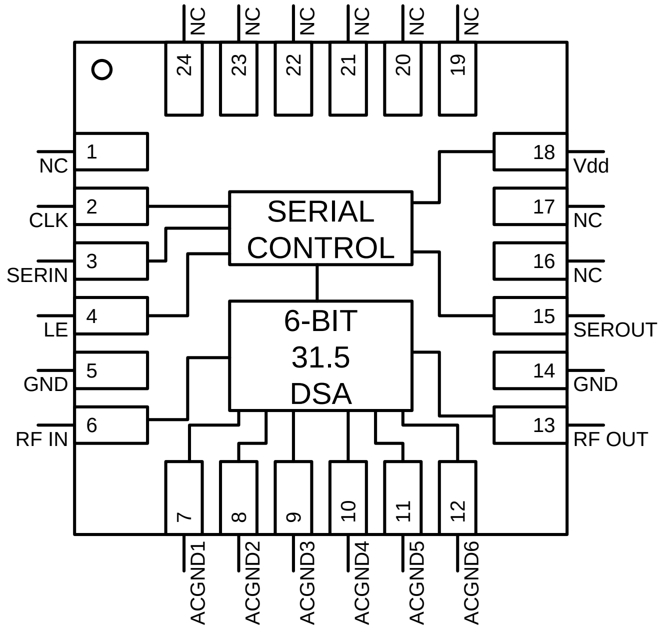


Mode 2: 0.04 - 4.0 GHz Operation (TQP4M9072-PCB_IF)

External bypass capacitors required on ACGND0 - ACGND5 pins. For improved operation below 0.1 GHz, blocking and bypass capacitors values can be increased to 10 nF. This circuit configuration can also be used for operation up to 4 GHz. The DSA performance remains unchanged for frequency range 0.7 - 4 GHz in either Mode 1 or Mode 2. There are 0.2 pF shunt capacitors (C5 and C7) next to RF connectors, on the application board, to resonate out the RF connector parasitic. These shunt capacitors are not required in the final application circuit.



Pin Description



Pin	Symbol	Description
2	CLK	Clock. This serial clock is used to clock in the serial data to the registers. The data is latched on the CLK rising edge. This input is a high impedance CMOS input.
3	SERIN	Serial Input Data. The 6-bit serial data is loaded MSB first. This input is a high impedance CMOS input.
4	LE	Latch Enable, When LE goes high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high, CLK is disabled
6	RF IN	RF Input, DC voltage present, blocking capacitor required. Can be used for Input or Output.
7	ACGND1	AC ground for extended low frequency operation option
8	ACGND2	AC ground for extended low frequency operation option
9	ACGND3	AC ground for extended low frequency operation option
10	ACGND4	AC ground for extended low frequency operation option
11	ACGND5	AC ground for extended low frequency operation option
12	ACGND6	AC ground for extended low frequency operation option
13	RF OUT	RF Output, DC voltage present, blocking capacitor required. Can be used for Input or Output.
15	SEROUT	Serial Output Data
18	V_{dd}	Supply Voltage. Bypass capacitor required close to the pin. Dropping resistor highly recommended ensuring compatibility with different power supplies.
5, 14	GND	These pins must be connected to RF/DC ground
1, 16, 17, 19, 20, 21, 22, 23, 24	N/C	These pins are not connected internally but can be grounded on the PCB
Backside Paddle	GND	Multiple vias should be employed for proper performance; see page 10 for suggested footprint

Applications Information

PC Board Layout

Top RF layer is .020" Rogers-4003, ϵ_r = 3.45, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .040", spacing = .020".

External DC blocking capacitors are required on RFin and RFout pins of the device. The supply voltage for the DSA is supplied externally through pin Vdd. Frequency bypassing for this pin is supplied by surface mount capacitor 0.1 uF (C4). This capacitor is placed close to the device pin in the board layout. To ensure application circuit is compatible with different standard power supplies, 15 Ω (R4) dropping resistor is highly recommended on Vdd supply line.

R1, R2 and R3 are used as termination for digital noise or any noise reflection on Serial Input, CLK and LE pins.

RF layout is critical for getting the best performance. RF trace impedance needs to be 50 ohm. For measuring the actual device performance on connectorized PC board, input losses due to RF traces need to be subtracted from the data measured through SMA connectors. The calibration microstrip line J6-J7 estimates the PCB insertion loss for removal from the evaluation board measured data. All data shown on the datasheet are de-embedded up to the device input/output pins.

The PC board is designed to test using USB control interface board, Evaluation Board Host (EVH). Each TQP4M9072 evaluation board is supplied with the EVH board, USB cable and EVH graphical user interface (EVH GUI) to change attenuation states. Manual for using EVH and Application note describing the EVH are also available. Refer to TriQuint's website for more information

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Bill of Material: 0.7 - 4.0 GHz Operation (Mode 1)

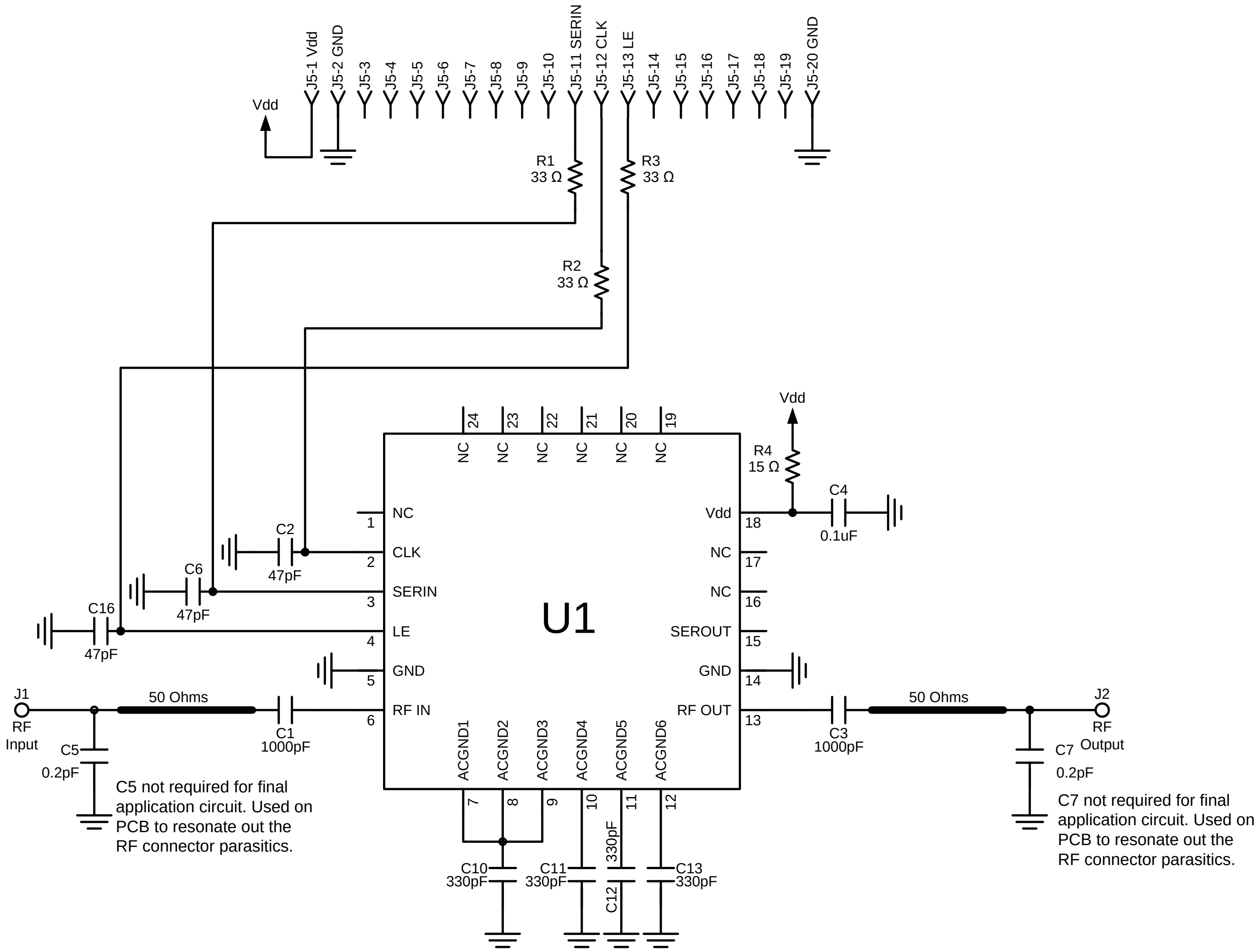
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		High Linearity 6-Bit, 31.5dB, DSA	TriQuint	TQP4M9072
C2, C6, C16	47 pF	Cap, Chip, 0402, 50V, NPO, 5%	various	
C1,C3	1000 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	
C4	0.1 uF	Cap, Chip, 0402, 50V, X7R, 10%	various	
R1, R2, R3	33 Ω	Res, Chip, 0402, 1/16W, 1%	various	
R4	15 Ω	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	DNP	Do Not Place	various	

Bill of Material: 0.04 - 4.0 GHz Operation (Mode 2)

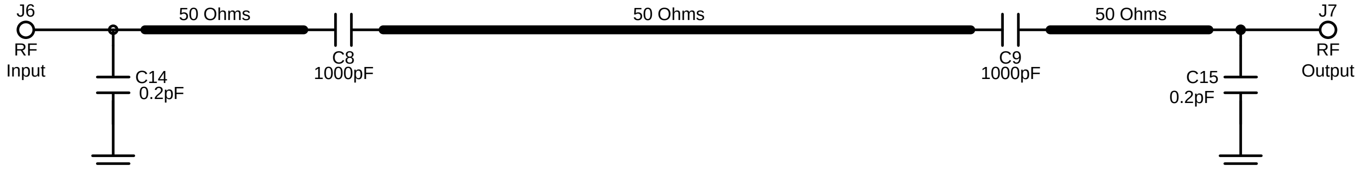
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		High Linearity 6-Bit, 31.5dB, DSA	TriQuint	TQP4M9072
C2, C6, C16	47 pF	Cap, Chip, 0402, 50V, NPO, 5%	various	
C1,C3	1000 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	
C4	0.1 uF	Cap, Chip, 0402, 50V, X7R, 10%	various	
R1, R2, R3	33 Ω	Res, Chip, 0402, 1/16W, 1%	various	
R4	15 Ω	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	330 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	

Applications Information

PC Board Schematic



Thru Calibration Line

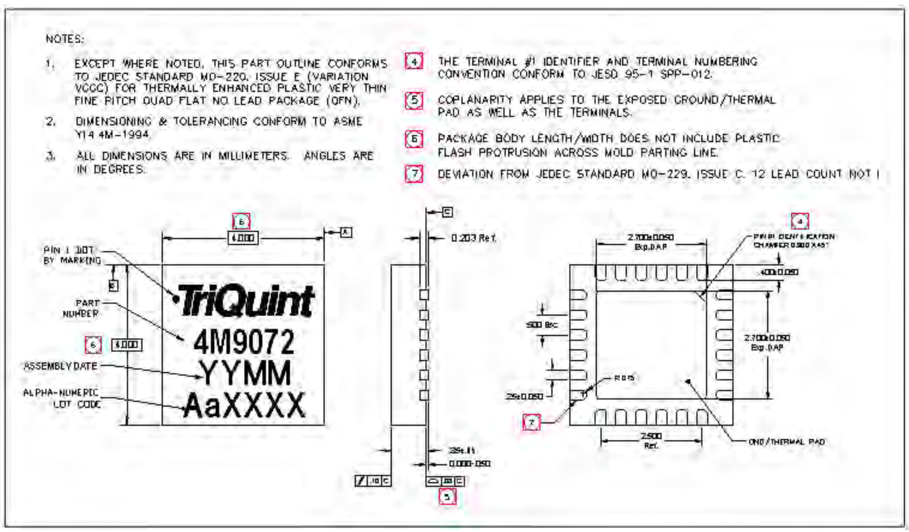


Mechanical Information

Package Information and Dimensions

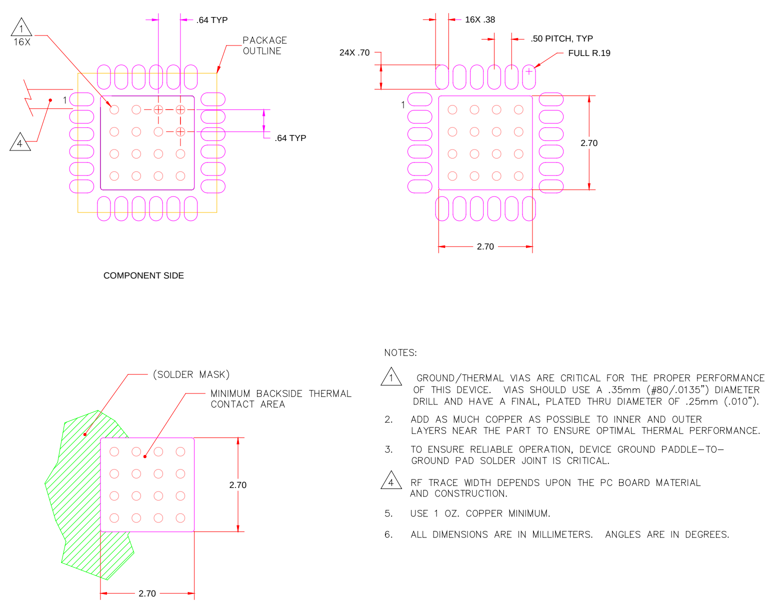
This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

The component will be laser marked with "4M9072" product label with an alphanumeric lot code on the top surface of the package.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:
1. Ground vias are critical for the proper RF performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000 V to < 2000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL 1 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with both lead-free (maximum 260 °C reflow temperature) and tin/lead (maximum 245 °C reflow temperature) soldering processes.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web:	**www.triquint.com**	**Tel:**	**+1.503.615.9000**
Email:	**info-sales@tqs.com**	**Fax:**	**+1.503.615.8902**

For technical questions and application information:

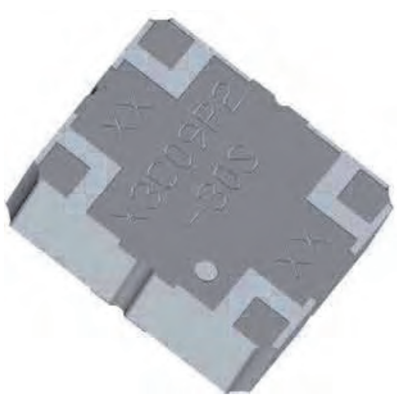
Email: **sjcapplications.engineering@tqs.com**

Important Notice

Model X3C09P2-30S

Rev B

30 dB Directional Coupler



Description

The X3C09P2-30S is a low profile, high performance 30dB directional coupler in a new easy to use, manufacturing friendly surface mount package. It is designed for AMPS, GSM, WCDMA and LTE band applications. The X3C09P2-30S is designed particularly for power and frequency detection, as well as for VSWR monitoring, where tightly controlled coupling and low insertion loss is required. It can be used in high power applications up to 225 Watts.

Parts have been subjected to rigorous qualification testing and they are manufactured using materials with coefficients of thermal expansion (CTE) compatible with common substrates such as FR4, G-10, RF-35, RO4003 and polyimide. Produced with 6 of 6 RoHS compliant tin immersion finish

Features:

- 800 - 1000 MHz
- AMPS, GSM, WCDMA and LTE band
- High Power
- Very Low Loss
- Tight Coupling
- High Directivity
- Production Friendly
- Tape and Reel
- Lead Free

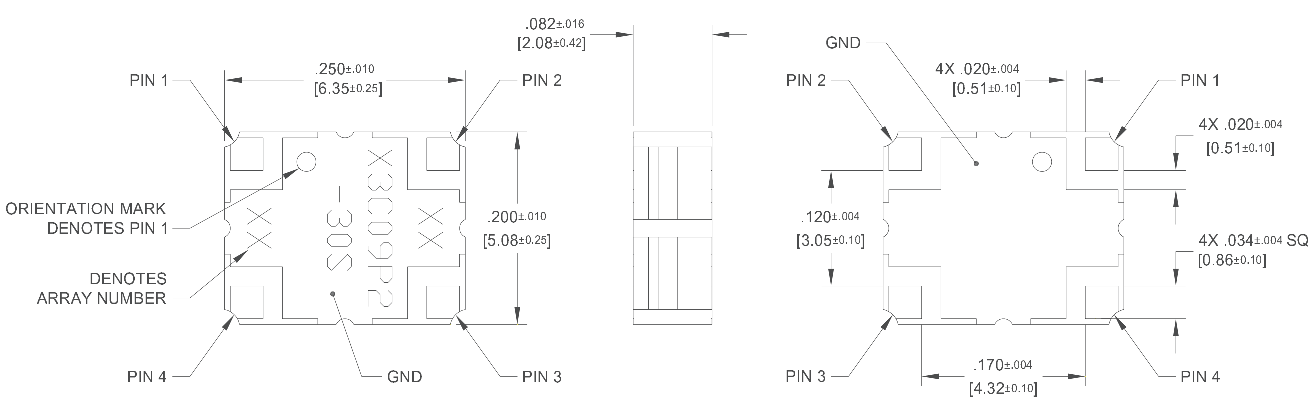
Electrical Specifications **

Frequency	Mean Coupling	Insertion Loss	VSWR	Directivity
MHz	*dB*	*dB Max*	*Max : 1*	*dB Min*
800 - 1000	30.2 ± 1.50	0.10	1.15	20
869 - 894	30.0 ± 1.50	0.075	1.12	20
925 - 960	30.0 ± 1.50	0.075	1.12	20
700 – 800	30.4 ± 1.50	0.10	1.22	20

Frequency Sensitivity	Power	ΘJC	Operating Temp.
dB Max	*Avg. CW Watts*	*ºC/Watt*	*ºC*
± 0.40	225	45	-55 to +95
± 0.1	225	45	-55 to +95
± 0.1	225	45	-55 to +95
± 0.40	225	45	-55 to +95

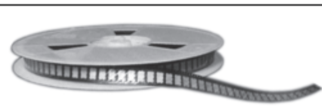
**Specification based on performance of unit properly installed on Anaren Test Board 61015-0001. Refer to Specifications subject to change without notice. Refer to parameter definitions for details.

Mechanical Outline



Dimensions are in Inches [Millimeters]
X3C09P2-30S Mechanical Outline

Tolerances are Non-Cumulative

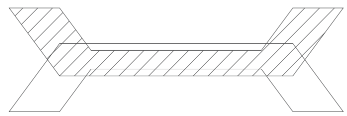


Available on Tape and Reel for Pick and Place Manufacturing.

USA/Canada: (315) 432-8909
Toll Free: (800) 411-6596
Europe: +44 2392-232392

Directional Coupler Pin Configuration

The X3C09P2-30S has an orientation marker to denote Pin 1. Once port one has been identified the other ports are known automatically. Please see the chart below for clarification:

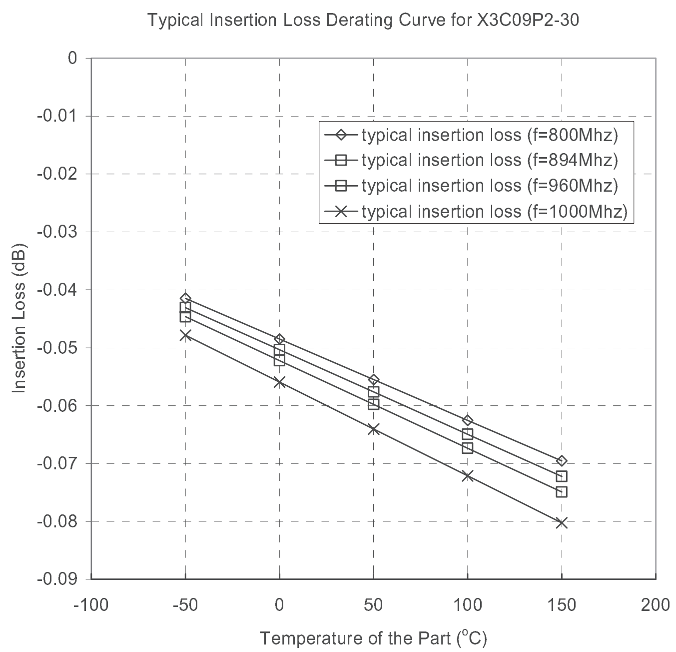


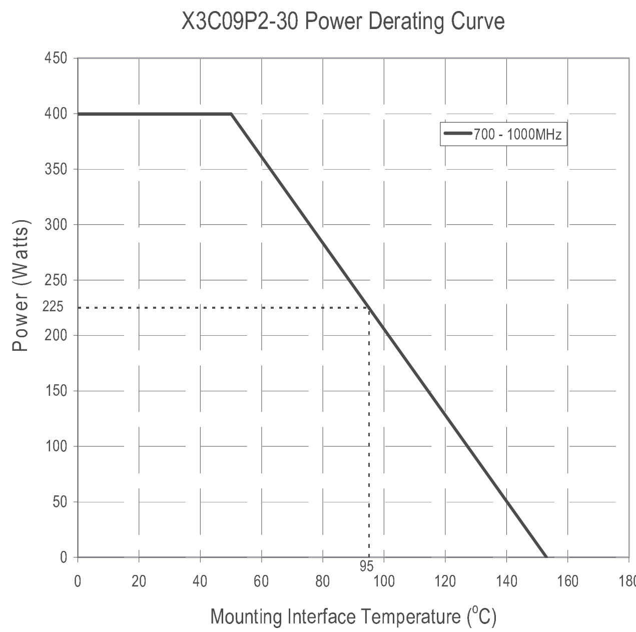
30dB Coupler Pin Configuration

Pin 1	Pin 2	Pin 3	Pin 4
Input	Direct	Isolated	Coupled
Direct	Input	Coupled	Isolated

Note: The direct port has a DC connection to the input port and the coupled port has a DC connection to the isolated port.
For optimum IL and power handling performance, use Pin 1 or Pin 2 as inputs.

Insertion Loss and Power Derating Curves





Insertion Loss Derating:

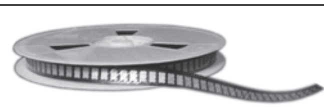
The insertion loss, at a given frequency, of a group of couplers is measured at 25°C and then averaged. The measurements are performed under small signal conditions (i.e. using a Vector Network Analyzer). The process is repeated at 85°C and 150°C. A best-fit line for the measured data is computed and then plotted from -55°C to 150°C.

Power Derating:

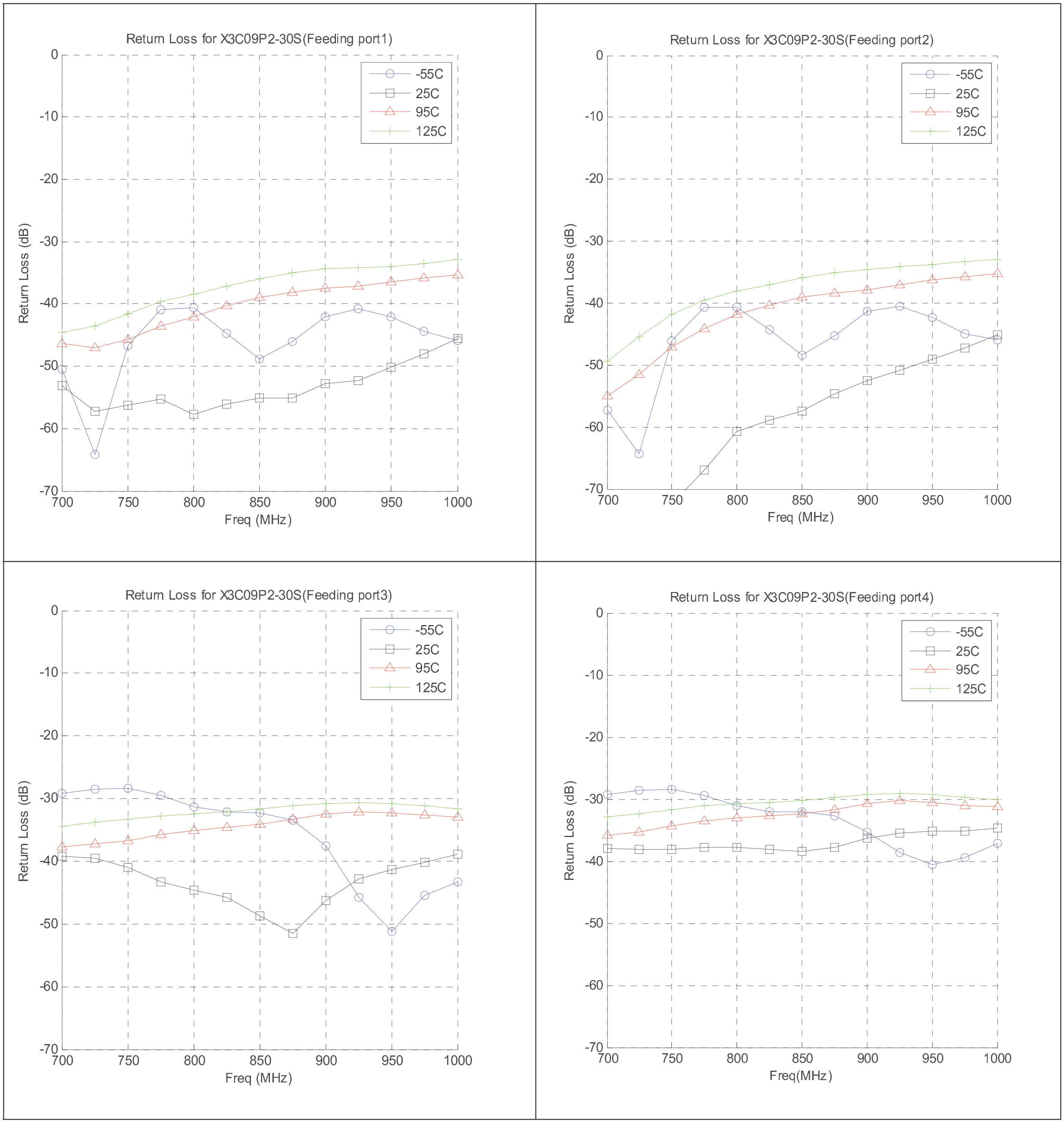
The power handling and corresponding power derating plots are a function of the thermal resistance, mounting surface temperature (base plate temperature), maximum continuous operating temperature of the coupler, and the thermal insertion loss. The thermal insertion loss is defined in the Power Handling section of the data sheet.

As the mounting interface temperature approaches the maximum continuous operating temperature, the power handling decreases to zero.

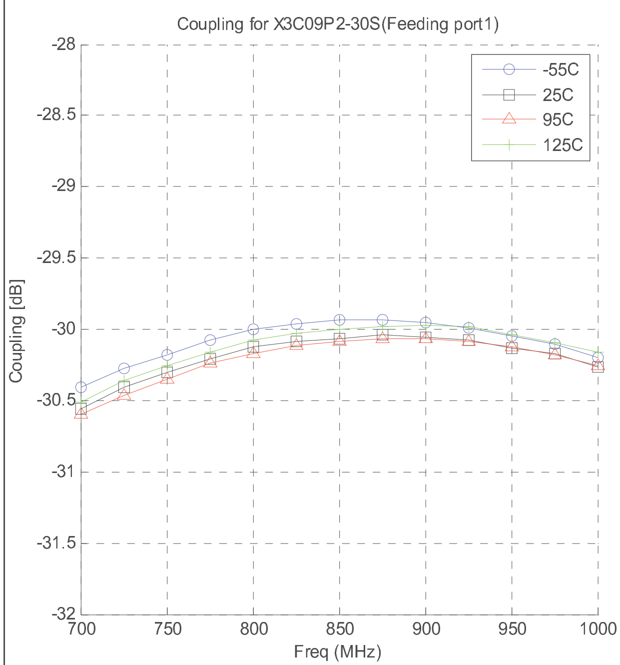
If mounting temperature is greater than 95°C, Xinger coupler will perform reliably as long as the input power is derated to the curve above.

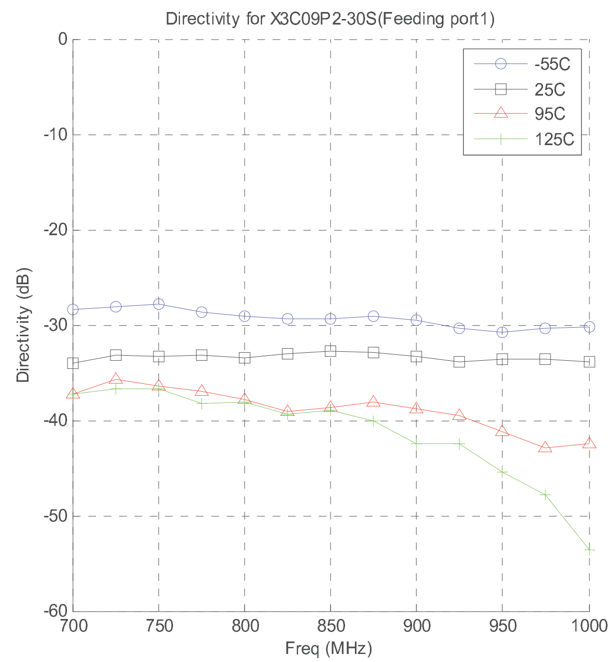


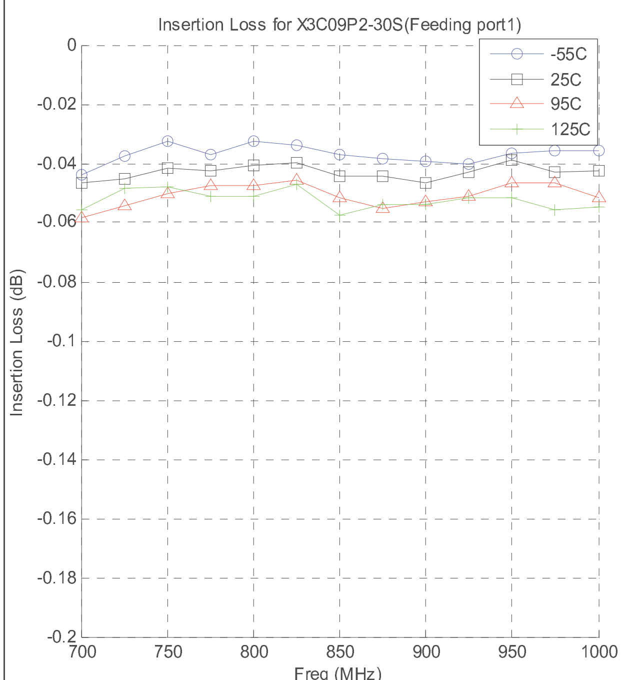
Typical Performance (-55°C, 25°C, 95°C & 125°C): 700-1000 MHz

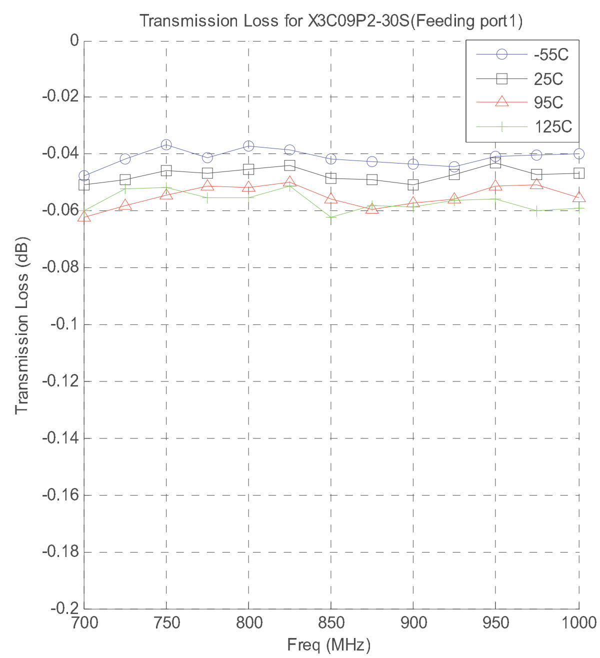


Typical Performance (-55°C, 25°C, 95°C & 125°C): 700-1000 MHz







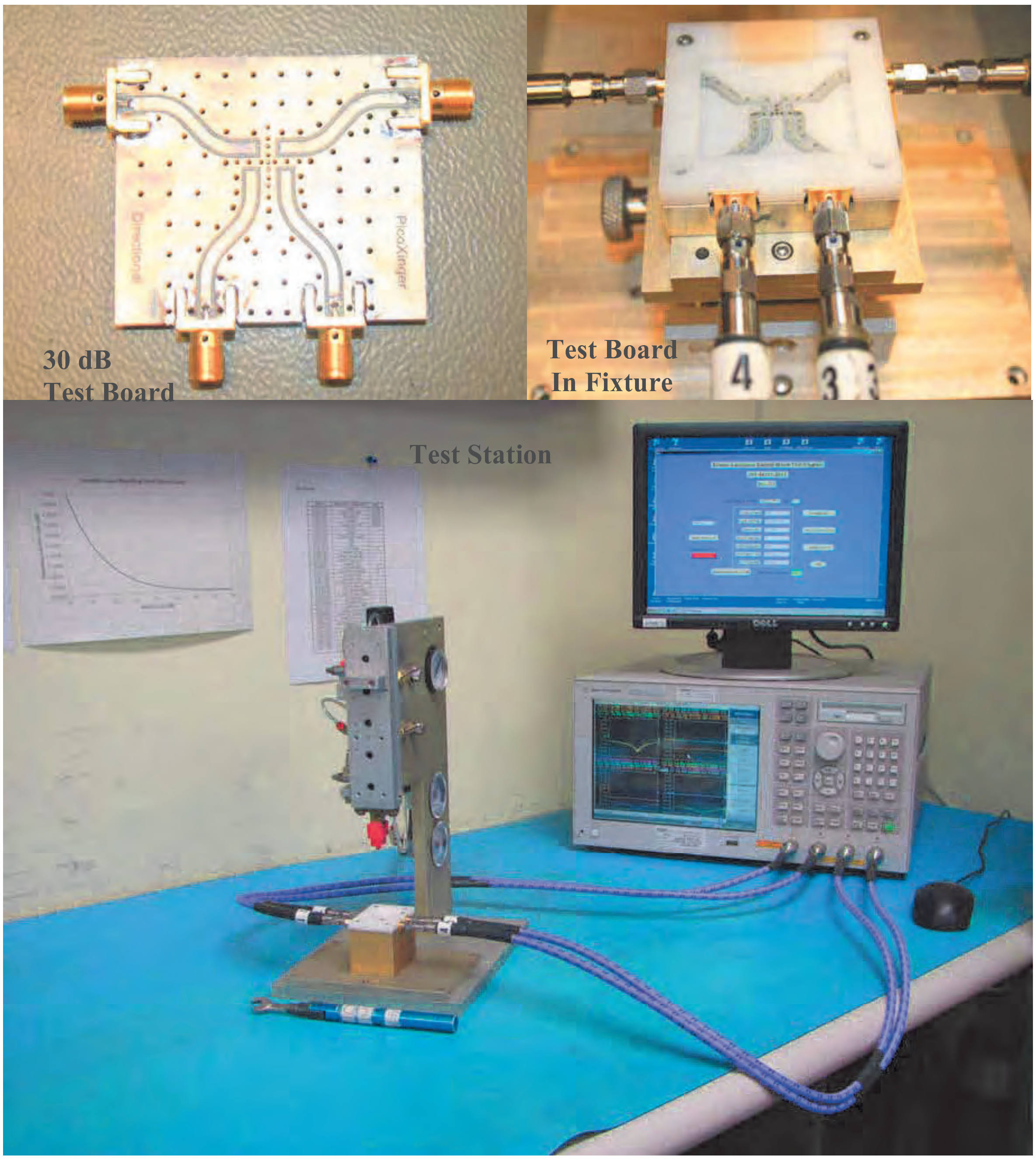


Definition of Measured Specifications

Parameter	Definition	Mathematical Representation
VSWR (Voltage Standing Wave Ratio)	The impedance match of the coupler to a 50Ω system. A VSWR of 1:1 is optimal.	$VSWR = \frac{V_{max}}{V_{min}}$ Vmax = voltage maxima of a standing wave Vmin = voltage minima of a standing wave
Return Loss	The impedance match of the coupler to a 50Ω system. Return Loss is an alternate means to express VSWR.	Return Loss (dB)= $20\log \frac{VSWR+1}{VSWR-1}$
Mean Coupling	At a given frequency (ω_n), coupling is the input power divided by the power at the coupled port. Mean coupling is the average value of the coupling values in the band. N is the number of frequencies in the band.	Coupling (dB) = $C(\omega_n) = 10\log\left(\frac{P_{in}(\omega_n)}{P_{cpl}(\omega_n)}\right)$ Mean Coupling (dB) = $\frac{\sum_{n=1}^{N} C(\omega_n)}{N}$
Insertion Loss	The input power divided by the sum of the power at the two output ports.	$10\log \frac{P_{in}}{P_{cpl}+P_{direct}}$
Transmission Loss	The input power divided by the power at the direct port.	$10\log \frac{P_{in}}{P_{direct}}$
Directivity	The power at the coupled port divided by the power at the isolated port.	$10\log \frac{P_{cpl}}{P_{iso}}$
Frequency Sensitivity	The decibel difference between the maximum in band coupling value and the mean coupling, and the decibel difference between the minimum in band coupling value and the mean coupling.	Max Coupling (dB) – Mean Coupling (dB) and Min Coupling (dB) – Mean Coupling (dB)

Notes on RF Testing and Circuit Layout

The X3C09P2-30S Surface Mount Couplers require the use of a test fixture for verification of RF performance. This test fixture is designed to evaluate the coupler in the same environment that is recommended for installation. Enclosed inside the test fixture, is a circuit board that is fabricated using the recommended footprint. The part being tested is placed into the test fixture and pressure is applied to the top of the device using a pneumatic piston. A four port Vector Network Analyzer is connected to the fixture and is used to measure the S-parameters of the part. Worst case values for each parameter are found and compared to the specification. These worst case values are reported to the test equipment operator along with a Pass or Fail flag. See the illustrations below.



The effects of the test fixture on the measured data must be minimized in order to accurately determine the performance of the device under test. If the line impedance is anything other than 50Ω and/or there is a discontinuity at the microstrip to SMA interface, there will be errors in the data for the device under test. The test environment can never be “perfect”, but the procedure used to build and evaluate the test boards (outlined below) demonstrates an attempt to minimize the errors associated with testing these devices. The lower the signal level that is being measured, the more impact the fixture errors will have on the data. Parameters such as Return Loss and Isolation/Directivity, which are specified as low as 27dB and typically measure at much lower levels, will present the greatest measurement challenge.

The test fixture errors introduce an uncertainty to the measured data. Fixture errors can make the performance of the device under test look better or worse than it actually is. For example, if a device has a known return loss of 30dB and a discontinuity with a magnitude of –35dB is introduced into the measurement path, the new measured Return Loss data could read anywhere between –26dB and –37dB. This same discontinuity could introduce an insertion phase error of up to 1°.

There are different techniques used throughout the industry to minimize the affects of the test fixture on the measurement data. Anaren uses the following design and de-embedding criteria:

- Test boards have been designed and parameters specified to provide trace impedances of 50 ±1Ω. Furthermore, discontinuities at the SMA to microstrip interface are required to be less than –35dB and insertion phase errors (due to differences in the connector interface discontinuities and the electrical line length) should be less than ±0.25° from the median value of the four paths.

- A “Thru” circuit board is built. This is a two port, microstrip board that uses the same SMA to microstrip interface and has the same total length (insertion phase) as the actual test board. The “Thru” board must meet the same stringent requirements as the test board. The insertion loss and insertion phase of the “Thru” board are measured and stored. This data is used to completely de-embed the device under test from the test fixture. The de-embedded data is available in S-parameter form on the Anaren website (www.anaren.com).

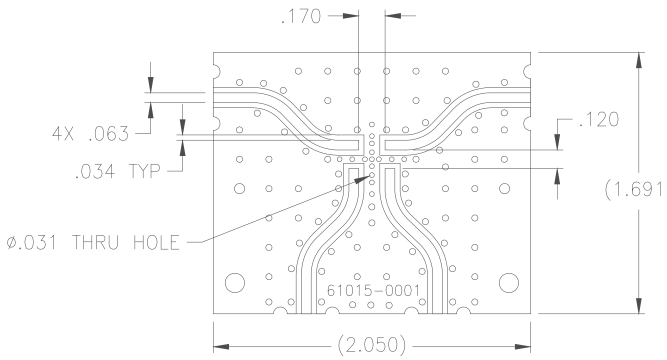
Note: The S-parameter files that are available on the anaren.com website include data for frequencies that are outside of the specified band. It is important to note that the test fixture is designed for optimum performance through 2.3GHz. Some degradation in the test fixture performance will occur above this frequency and connector interface discontinuities of –25dB or more can be expected. This larger discontinuity will affect the data at frequencies above 2.3GHz.

<u>Circuit Board Layout</u>

The dimensions for the Anaren test board are shown below. The test board is printed on Rogers RO4350 material that is 0.030” thick. Consider the case when a different material is used. First, the pad size must remain the same to accommodate the part. But, if the material thickness or dielectric constant (or both) changes, the reactance at the interface to the coupler will also change. Second, the linewidth required for 50Ω will be different and this will introduce a step in the line at the pad where the coupler interfaces with the printed microstrip trace. Both of these conditions will affect the performance of the part. **<u>To achieve the specified performance, serious attention must be given to the design and layout of the circuit environment in which this component will be used.</u>**

If a different circuit board material is used, an attempt should be made to achieve the same interface pad reactance that is present on the Anaren RO4350 test board. When thinner circuit board material is used, the ground plane will be closer to the pad yielding more capacitance for the same size interface pad. The same is true if the dielectric constant of the circuit board material is higher than is used on the Anaren test board. In both of these cases, narrowing the line before the interface pad will introduce a series inductance, which, when properly tuned, will compensate for the extra capacitive reactance. If a thicker circuit board or one with a lower dielectric constant is used, the interface pad will have less capacitive reactance than the Anaren test board. In this case, a wider section of line before the interface pad (or a larger interface pad) will introduce a shunt capacitance and when properly tuned will match the performance of the Anaren test board.

Notice that the board layout for the 3dB and 5dB couplers is different from that of the 10dB and 20dB couplers. The test board for the 3dB and 5dB couplers has all four traces interfacing with the coupler at the same angle. The test board for the 10dB, 20dB and 30dB couplers has two traces approaching at one angle and the other two traces at a different angle. **The entry angle of the traces has a significant impact on the RF performance and these parts have been optimized for the layout used on the test boards shown below.**



30dB Test Board

<u>Testing Sample Parts Supplied on Anaren Test Boards</u>

If you have received a coupler installed on an Anaren produced microstrip test board, please remember to remove the loss of the test board from the measured data. The loss is small enough that it is not of concern for Return Loss and Isolation/Directivity, but it should certainly be considered when measuring coupling and calculating the insertion loss of the coupler. An S-parameter file for a "Thru" board (see description of "Thru" board above) will be supplied upon request. As a first order approximation, one should consider the following loss estimates:

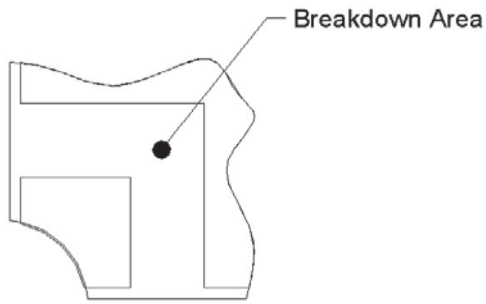
Frequency Band	Avg. Ins. Loss of Test Board @ 25°C
410 – 500 MHz	~ 0.04dB
800 - 1000 MHz	~ 0.06dB
1700 – 2300 MHz	~0.14dB
2300 – 2700 MHz	~0.155dB
3300 – 3800 MHz	~0.20dB

For example, a 1900MHz, 10dB coupler on a test board may measure –10.30dB from input to the coupled port at some frequency, F1. When the loss of the test board is removed, the coupling at F1 becomes -10.18dB (-10.30dB + 0.12dB). This compensation must be made to both the coupled and direct path measurements when calculating insertion loss.

The loss estimates in the table above come from room temperature measurements. It is important to note that the loss of the test board will change with temperature. This fact must be considered if the coupler is to be evaluated at other temperatures.

Peak Power Handling

High-Pot testing of these couplers during the qualification procedure resulted in a minimum breakdown voltage of 1.40 kV. This voltage level corresponds to a breakdown resistance capable of handling at least 12dB peaks over average power levels, for very short durations. The breakdown location consistently occurred across the air interface at the coupler contact pads (see illustration below). The breakdown levels at these points will be affected by any contamination in the gap area around these pads. These areas must be kept clean for optimum performance. It is recommended that the user test for voltage breakdown under the maximum operating conditions and over worst case modulation induced power peaking. This evaluation should also include extreme environmental conditions (such as high humidity).



Orientation Marker

A printed circular feature appears on the top surface of the coupler to designate Pin 1. This orientation marker is **not** intended to limit the use of the symmetry that these couplers exhibit but rather to facilitate consistent placement of these parts into the tape and reel package. This ensures that the components are always delivered with the same orientation. Refer to the table on page 2 of the data sheet for allowable pin configurations.

Test Plan

Xinger III 30dB couplers are manufactured in large panels and then separated. A sample population of parts is RF small signal tested at room temperature in the fixture described above. All parts are DC tested for shorts/opens. (See "Qualification Flow Chart" section for details on the accelerated life test procedures.)

Power Handling

The average power handling (total input power) of a Xinger coupler is a function of:

- Internal circuit temperature.
- Unit mounting interface temperature.
- Unit thermal resistance
- Power dissipated within the unit.

All thermal calculations are based on the following assumptions:

- The unit has reached a steady state operating condition.
- Maximum mounting interface temperature is 95°C.
- Conduction Heat Transfer through the mounting interface.
- No Convection Heat Transfer.
- No Radiation Heat Transfer.
- The material properties are constant over the operating temperature range.

Finite element simulations are made for each unit. The simulation results are used to calculate the unit thermal resistance. The finite element simulation requires the following inputs:

- Unit material stack-up.
- Material properties.
- Circuit geometry.
- Mounting interface temperature.
- Thermal load (dissipated power).

The classical definition for dissipated power is temperature delta (ΔT) divided by thermal resistance (R). The dissipated power (P_{dis}) can also be calculated as a function of the total input power (P_{in}) and the thermal insertion loss (IL_{therm}):

$$P_{dis} = \frac{\Delta T}{R} = P_{in} \cdot \left(1 - 10^{\frac{-IL_{therm}}{10}} \right) \quad (W) \qquad (1)$$

Power flow and nomenclature for an “H” style coupler is shown in Figure 1.

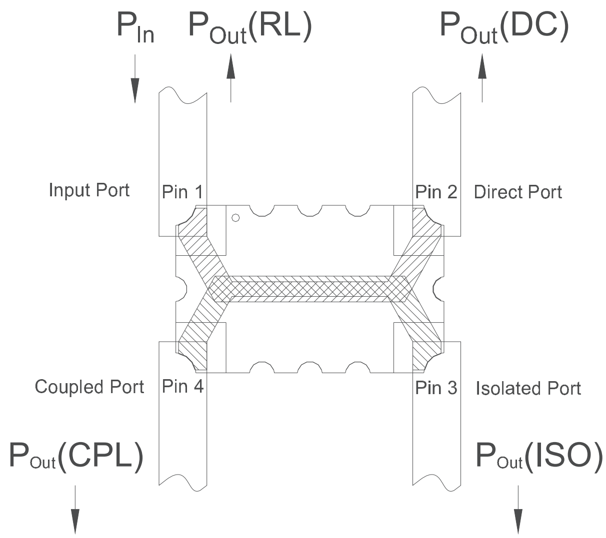


Figure 1

The coupler is excited at the input port with P_{in} (watts) of power. Assuming the coupler is not ideal, and that there are no radiation losses, power will exit the coupler at all four ports. Symbolically written, $P_{out(RL)}$ is the power that is returned to the source because of impedance mismatch, $P_{out(ISO)}$ is the power at the isolated port, $P_{out(CPL)}$ is the power at the coupled port, and $P_{out(DC)}$ is the power at the direct port.

At Anaren, insertion loss is defined as the log of the input power divided by the sum of the power at the coupled and direct ports:

Note: in this document, insertion loss is taken to be a positive number. In many places, insertion loss is written as a negative number. Obviously, a mere sign change equates the two quantities.

$$IL = 10 \cdot \log_{10}\left(\frac{P_{in}}{P_{out(CPL)} + P_{out(DC)}} \right) \quad (dB) \qquad (2)$$

In terms of S-parameters, IL can be computed as follows:

$$IL = -10 \cdot \log_{10}\left(|S_{31}|^2 + |S_{41}|^2 \right) \quad (dB) \qquad (3)$$

We notice that this insertion loss value includes the power lost because of return loss as well as power lost to the isolated port.

For thermal calculations, we are only interested in the power lost “inside” the coupler. Since $P_{out(RL)}$ is lost in the source termination and $P_{out(ISO)}$ is lost in an external termination, they are not be included in the insertion loss for thermal calculations. Therefore, we define a new insertion loss value solely to be used for thermal calculations:

$$IL_{therm} = 10 \cdot \log_{10}\left(\frac{P_{in}}{P_{out(CPL)} + P_{out(DC)} + P_{out(ISO)} + P_{out(RL)}} \right) \quad (dB) \qquad (4)$$

In terms of S-parameters, IL_{therm} can be computed as follows:

$$IL_{therm} = -10 \cdot \log_{10}\left(|S_{11}|^2 + |S_{21}|^2 + |S_{31}|^2 + |S_{41}|^2 \right) \quad (dB) \qquad (5)$$

The thermal resistance and power dissipated within the unit are then used to calculate the average total input power of the unit. The average total steady state input power (P_{in}) therefore is:

$$P_{in} = \frac{P_{dis}}{\left(1 - 10^{\frac{-IL_{therm}}{10}}\right)} = \frac{\frac{\Delta T}{R}}{\left(1 - 10^{\frac{-IL_{therm}}{10}}\right)} \quad (W) \qquad (6)$$

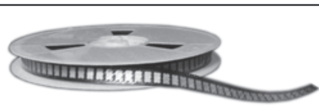
Where the temperature delta is the circuit temperature (T_{circ}) minus the mounting interface temperature (T_{mnt}):

$$\Delta T = T_{circ} - T_{mnt} \quad (^{o}C) \qquad (7)$$

The maximum allowable circuit temperature is defined by the properties of the materials used to construct the unit. Multiple material combinations and bonding techniques are used within the Xinger III product family to optimize RF performance. Consequently the maximum allowable circuit temperature varies. Please note that the circuit temperature is not a function of the Xinger case (top surface) temperature. Therefore, the case temperature cannot be used as a boundary condition for power handling calculations.

Due to the numerous board materials and mounting configurations used in specific customer configurations, it is the end users responsibility to ensure that the Xinger III coupler mounting interface temperature is maintained within the limits defined on the power derating plots for the required average power handling. Additionally appropriate solder composition is required to prevent reflow or fatigue failure at the RF ports. Finally, reliability is improved when the mounting interface and RF port temperatures are kept to a minimum.

The power-derating curve illustrates how changes in the mounting interface temperature result in converse changes of the power handling of the coupler.



Mounting

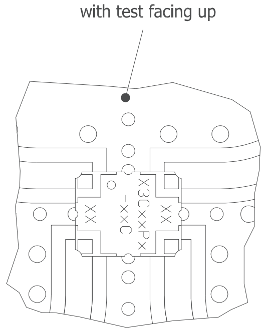
In order for Xinger surface mount couplers to work optimally, there must be 50Ω transmission lines leading to and from all of the RF ports. Also, there must be a very good ground plane underneath the part to ensure proper electrical performance. If either of these two conditions is not satisfied, insertion loss, coupling, VSWR and isolation may not meet published specifications.

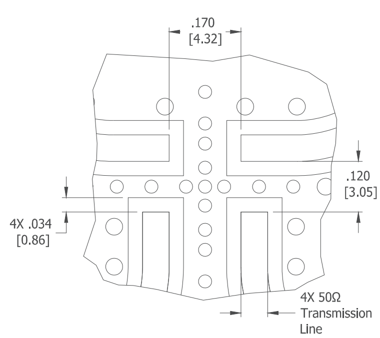
Overall ground is improved if a dense population of plated through holes connect the top and bottom ground layers of the PCB. This minimizes ground inductance and improves ground continuity. All of the Xinger hybrid and directional couplers are constructed from ceramic filled PTFE composites which possess excellent electrical and mechanical stability having X and Y thermal coefficient of expansion (CTE) of 17-25 ppm/^{o}C.

When a surface mount hybrid coupler is mounted to a printed circuit board, the primary concerns are; ensuring the RF pads of the device are in contact with the circuit trace of the PCB and insuring the ground plane of neither the component nor the PCB is in contact with the RF signal.

Mounting Footprint

To ensure proper electrical and thermal performance
there must be a ground plane with 100%
solder connection underneath the part orientated as shown
with test facing up





Dimensions are in inches [Millimeters]

Coupler Mounting Process

The process for assembling this component is a conventional surface mount process as shown in Figure 1. This process is conducive to both low and high volume usage.

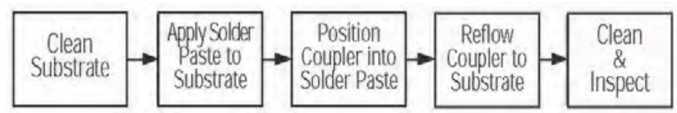


Figure 1: Surface Mounting Process Steps

Storage of Components: The Xinger III products are available in either an immersion tin or tin-lead finish. Commonly used storage procedures used to control oxidation should be followed for these surface mount components. The storage temperatures should be held between 15^{o}C and 60^{o}C.

Substrate: Depending upon the particular component, the circuit material has an x and y coefficient of thermal expansion of between 17 and 25 ppm/°C. This coefficient minimizes solder joint stresses due to similar expansion rates of most commonly used board substrates such as RF35, RO4350, FR4, polyimide and G-10 materials. Mounting to "hard" substrates (alumina etc.) is possible depending upon operational temperature requirements. The solder surfaces of the coupler are all copper plated with either an immersion tin or tin-lead exterior finish.

Solder Paste: All conventional solder paste formulations will work well with Anaren's Xinger III surface mount components. Solder paste can be applied with stencils or syringe dispensers. An example of a stenciled solder paste deposit is shown in Figure 2. As shown in the figure solder paste is applied to the four RF pads and the entire ground plane underneath the body of the part.

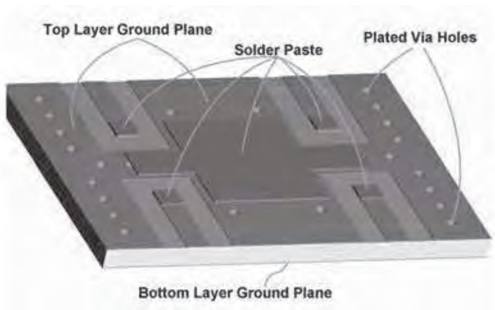


Figure 2: Solder Paste Application

Coupler Positioning: The surface mount coupler can be placed manually or with automatic pick and place mechanisms. Couplers should be placed (see Figure 3 and 4) onto wet paste with common surface mount techniques and parameters. Pick and place systems must supply adequate vacuum to hold a 0.204 gram coupler.

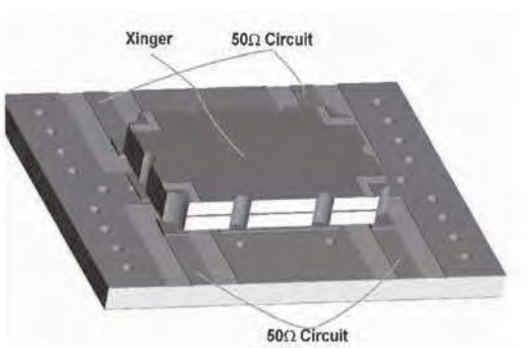


Figure 3: Component Placement

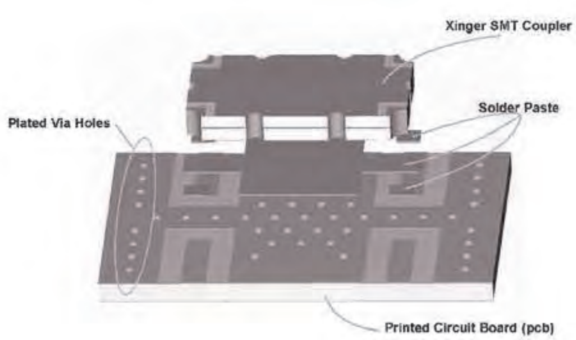


Figure 4: Mounting Features Example

Reflow: The surface mount coupler is conducive to most of today's conventional reflow methods. A low and high temperature thermal reflow profile are shown in Figures 5 and 6, respectively. Manual soldering of these components can be done with conventional surface mount non-contact hot air soldering tools. Board pre-heating is highly recommended for these selective hot air soldering methods. Manual soldering with conventional irons should be avoided.

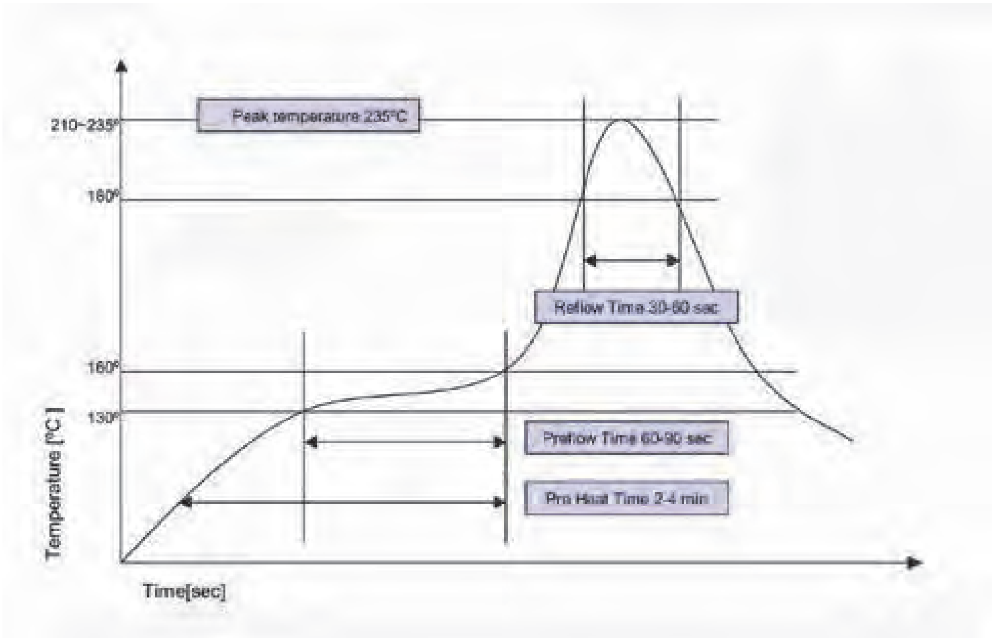


Figure 5 – Low Temperature Solder Reflow Thermal Profile

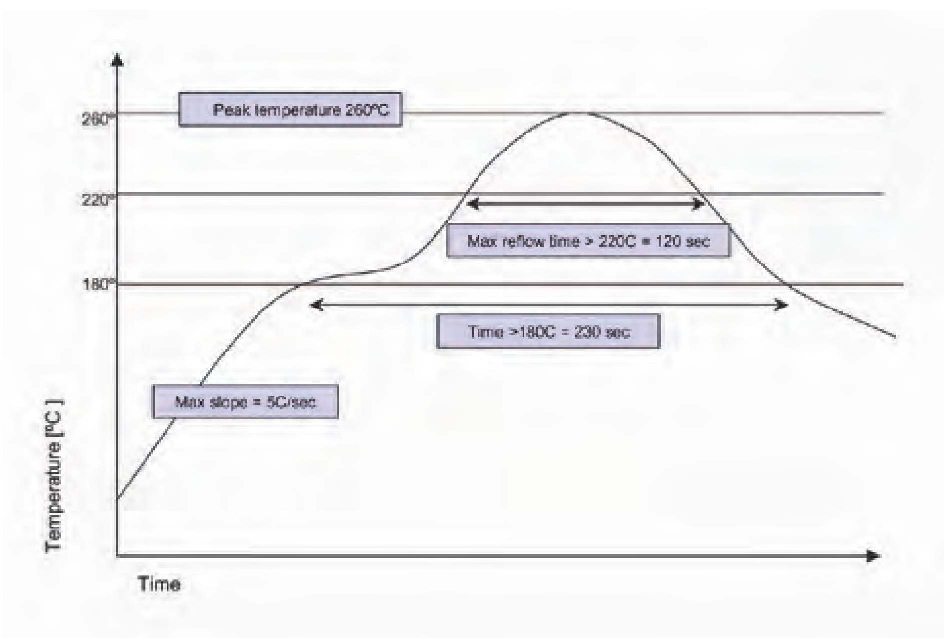
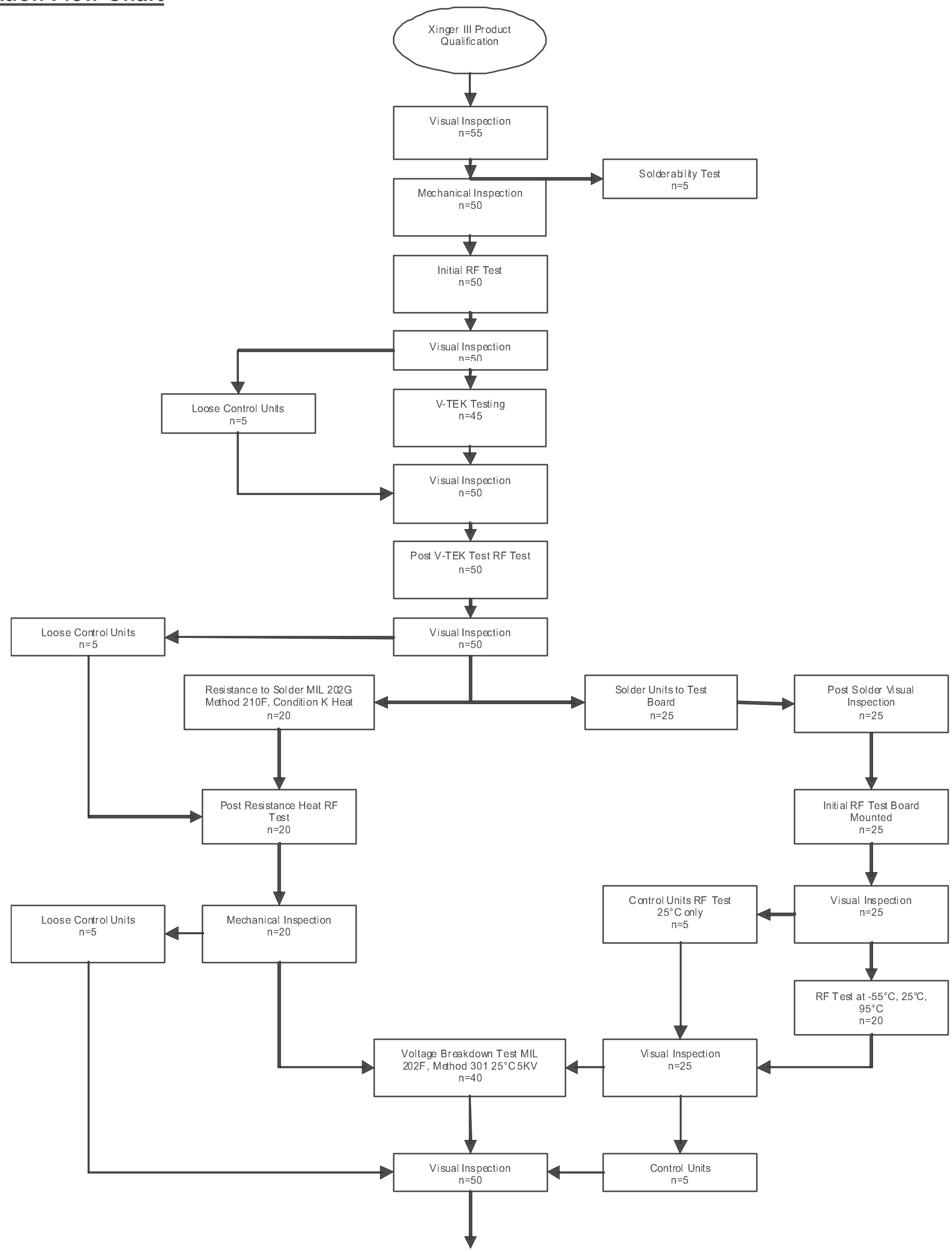
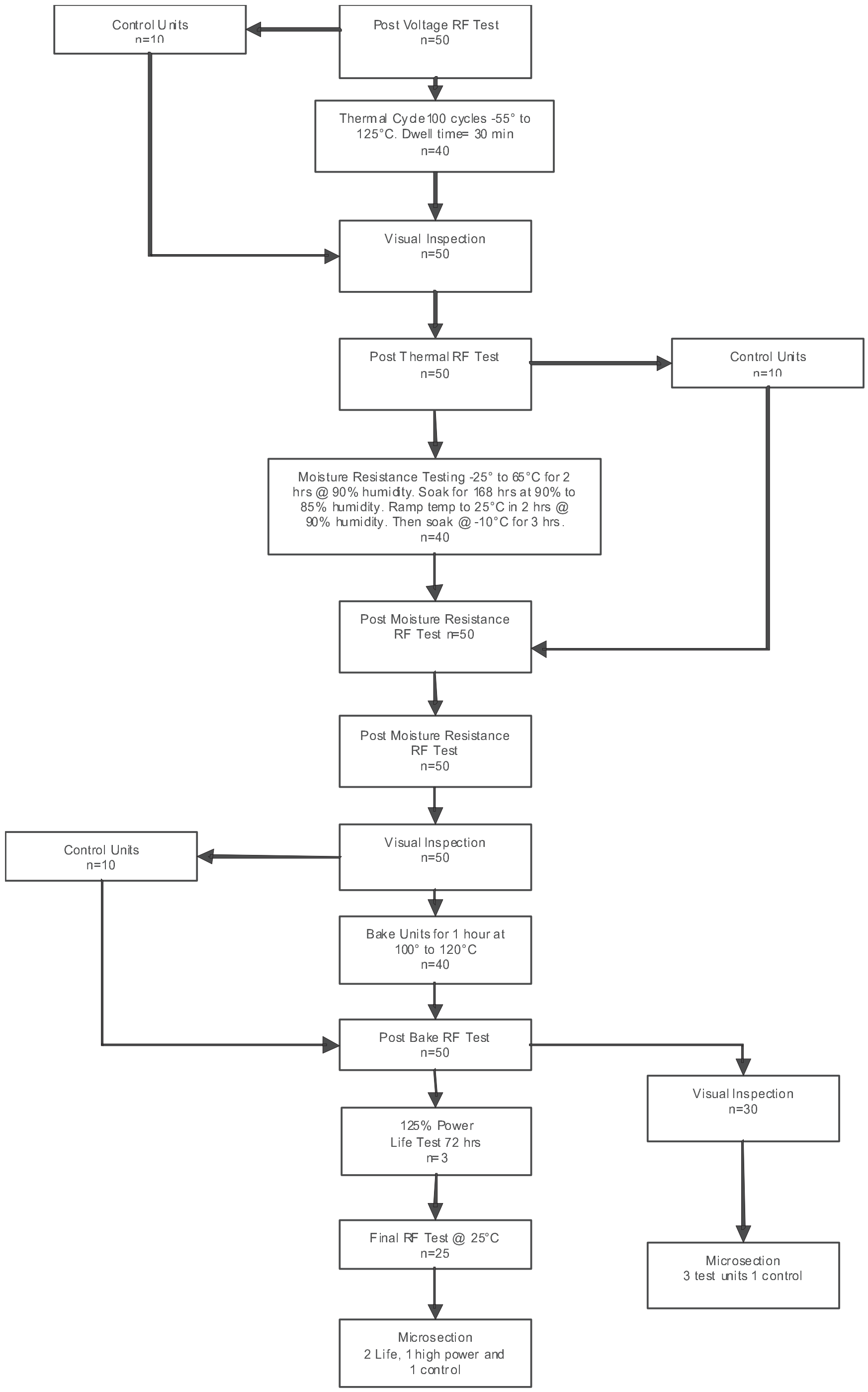


Figure 6 – High Temperature Solder Reflow Thermal Profile

Qualification Flow Chart





Control Units n=10
Post Voltage RF Test n=50
Thermal Cycle 100 cycles -55° to 125°C. Dwell time= 30 min n=40
Visual Inspection n=50
Post Thermal RF Test n=50
Control Units n=10
Moisture Resistance Testing -25° to 65°C for 2 hrs @ 90% humidity. Soak for 168 hrs at 90% to 85% humidity. Ramp temp to 25°C in 2 hrs @ 90% humidity. Then soak @ -10°C for 3 hrs. n=40
Post Moisture Resistance RF Test n=50
Post Moisture Resistance RF Test n=50
Control Units n=10
Visual Inspection n=50
Bake Units for 1 hour at 100° to 120°C n=40
Post Bake RF Test n=50
Visual Inspection n=30
125% Power Life Test 72 hrs n=3
Final RF Test @ 25°C n=25
Microsection 3 test units 1 control
Microsection 2 Life, 1 high power and 1 control

Application Information

Directional Couplers and Sampling

Directional couplers are often used in circuits that require the sampling of an arbitrary signal. Because they are passive, non-linear devices, Anaren directional couplers do not perturb the characteristics of the signal to be sampled, and can be used for frequency monitoring and/or measurement of RF power. An example of a sampling circuit is the reflectometer. The purpose of the reflectometer is to isolate and sample the incident and reflected signals from a mismatched load. A basic reflectometer circuit is shown in Figure ap.n.1-1.

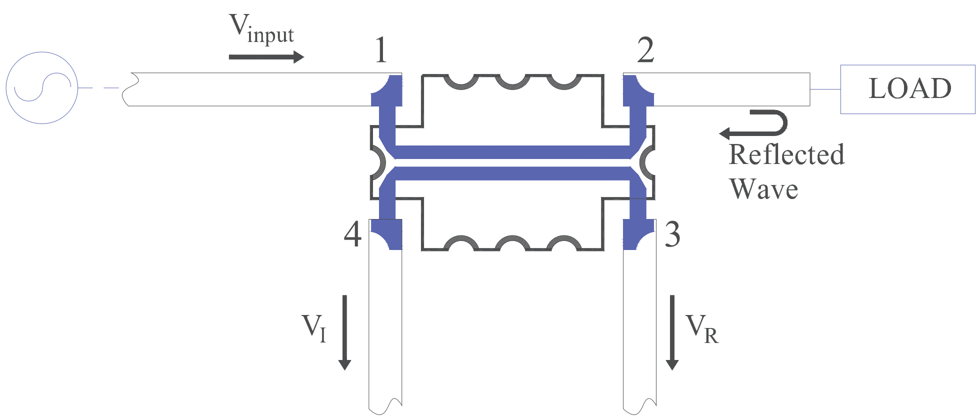


Figure ap.n.1-1. A Reflectometer Circuit Schematic

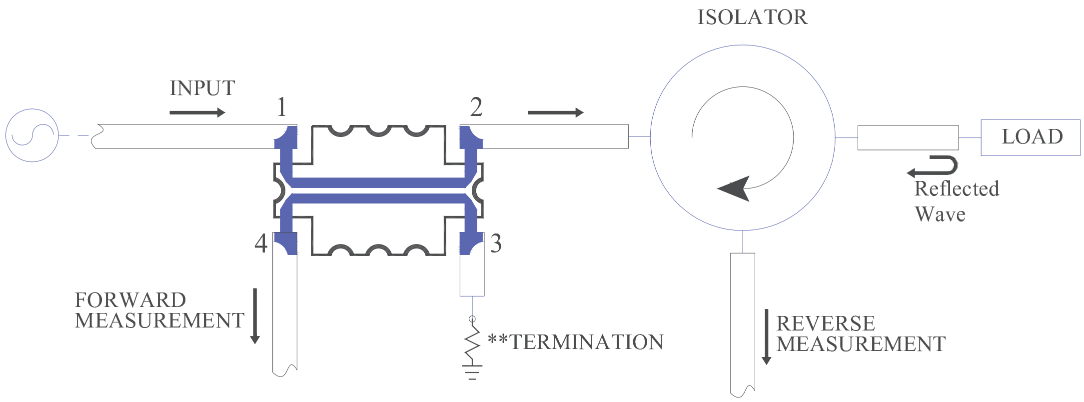
If the directional coupler has perfect directivity, then it is clear that V_I is strictly a sample of the incident voltage V_{input}, and V_R is strictly a sample of the wave that is reflected from the load. Since directivity is never perfect in practice, both V_I and V_R will contain samples of the input signal as well as the reflected signal. In that case,

$$V_I = \mathrm{C} + \mathrm{CDT}\Gamma e^{j\theta} \quad \text{Eq. ap.n.1-1}$$

and

$$V_R = \mathrm{CD} + \mathrm{CT}\Gamma e^{j\phi} \quad \text{Eq. ap.n.1-2}$$

where C is the coupling, D is the directivity, Γ is the complex reflection coefficient of the load, T is the transmission coefficient, and ϕ and θ are unknown phase delay differences caused by the interconnect lines on the test board. If we know V_I and V_R, we can easily calculate the reflection coefficient of the load. One should notice that in order to make forward and reverse measurements using only one coupler, the directivity must be really low. In specific customer applications, the preferred method for forward and reverse sampling is shown in Figure ap.n.1-2.



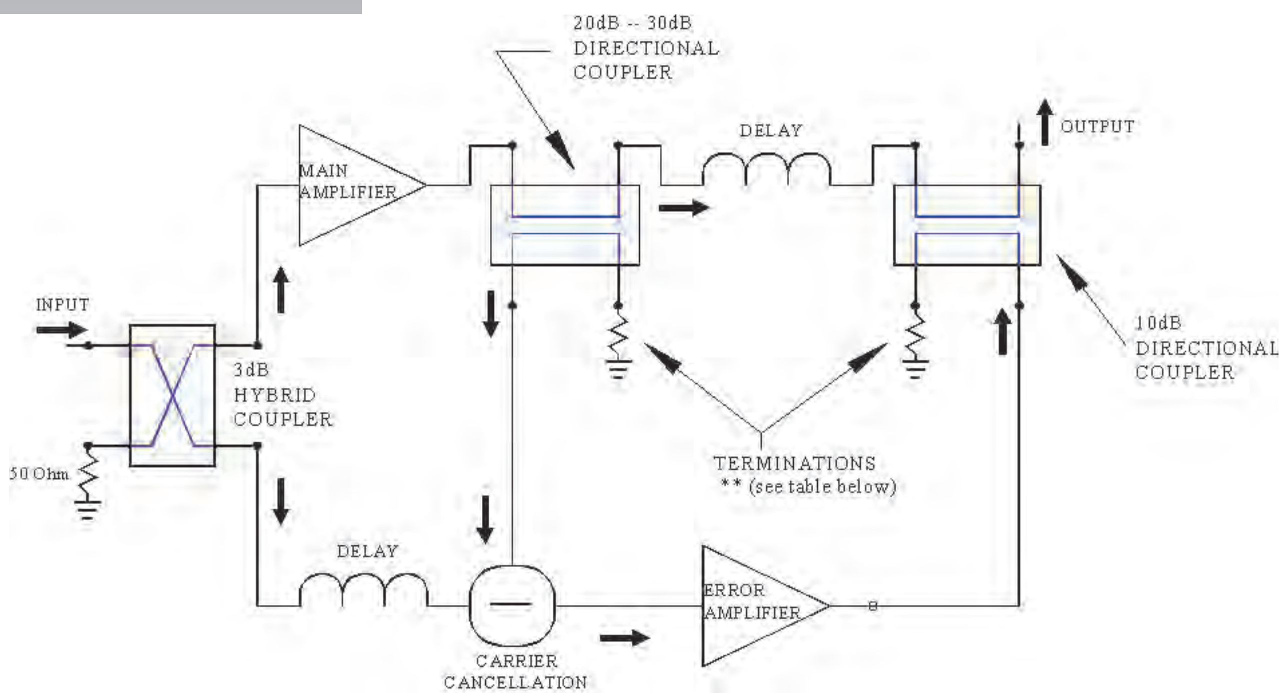
*Recommended Terminations	
Power (Watts)	Model
8	RFP- 060120A15Z50-2
10	RFP- C10A50Z4
16	RFP- C16A50Z4
20	RFP- C20N50Z4
50	RFP- C50A50Z4
100	RFP- C100N50Z4
200	RFP- C200N50Z4

Figure ap.n.1-2. Forward and Reverse Sampling

The isolator in Figure ap.n.1-2 prevents the reflected wave from exciting the directional coupler. A list of recommended terminations is shown in the figure.

Directional Couplers in Feed-Forward Amplifier Applications

Feed-forward amplifiers are widely used to reduce distortion due to nonlinearities in power amplifiers. Although the level and complexity of feed-forward amplifiers varies from one manufacturer to another, the basic building block for this linearization scheme remains the same. A basic feed-forward schematic is shown in Figure ap.n.2-1. The input signal is split in two using a hybrid coupler or power divider. The output of the main amplifier is sampled with a 20dB-30dB directional coupler. The X3C09P2-30S is an excellent candidate for this sampling since it provides great return loss and directivity. The sampled signal, which consists of a sample of the original input signal plus some distortion, is inverted and then combined with the output of the first delay line. This procedure subtracts (through destructive interference) the sample of the original input signal, leaving only the distortion or error component. The error component is then amplified and combined with the output of the second delay line using another directional coupler. In many cases, a 10dB coupler is used to combine the two signals. The XC0900E-10 is a perfect choice for this injection because it has tight coupling, superior directivity, and excellent match.



*Recommended Terminations	
Power (Watts)	Model
8	RFP- 060120A15Z50-2
10	RFP- C10A50Z4
16	RFP- C16A50Z4
20	RFP- C20N50Z4
50	RFP- C50A50Z4
100	RFP- C100N50Z4
200	RFP- C200N50Z4

Figure ap.n.2-1. Generic Feed Forward Circuit Schematic

Both directional couplers in the Figure ap.n.2-1 have one port terminated with a 50Ω resistor. In order to achieve optimum performance, the termination must be chosen carefully. It is important to remember that a good termination will not only produce a good match at the input of the coupler, but will also maximize the isolation between the input port and isolated port. Furthermore, since the termination can potentially absorb high levels of power, its maximum power rating should be chosen accordingly. A list of recommended terminations is shown in Figure ap.n.2-1. For an ideal lossless directional coupler, the power at the coupled and direct ports can be written as:

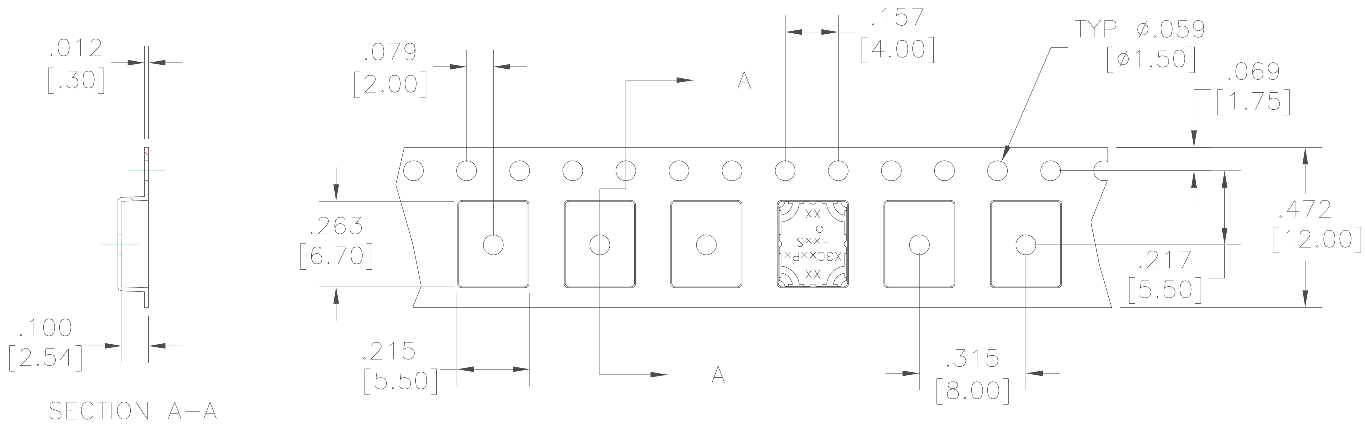
$$P_{coupled} = \frac{P_{input}}{10^{\frac{|Coupling(dB)|}{10}}} \quad Watts \qquad \text{Eq. ap.n.2-1}$$

$$P_{direct} = P_{input} - \frac{P_{input}}{10^{\frac{|Coupling(dB)|}{10}}} \quad Watts \qquad \text{Eq. ap.n.2-2}$$

where P_{input} is the input power in Watts, and Coupling(dB) is the coupling value in dB.

Packaging and Ordering Information

Parts are available in a reel and as loose parts in a bag. Packaging follows EIA 481-2 for reels. Parts are oriented in tape and reel as shown below. Minimum order quantities are 2000 per reel and 100 for loose parts. See Model Numbers below for further ordering information.



Dimensions are in Inches[MM]

Direction of Part Feed (Unloading)

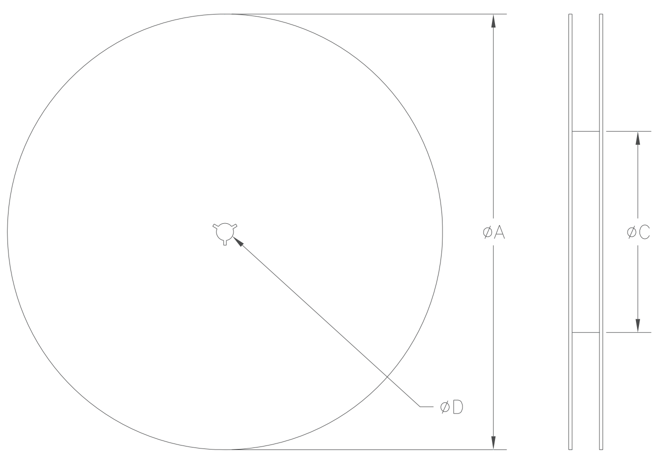


TABLE 1	
REEL DIMENSIONS (inches [mm])	
⌀A	13.0 [330.0]
B	.472 [12.0]
⌀C	4.017 [102.03]
⌀D	0.512 [13.0]

XXX XX X X - XX X

Xinger Coupler	Frequency (MHz)	Size (Inches)	Power (Watts)	Coupling Value	Plating Finish
X3C	04 = 410-500 07 = 600-900 09 = 800-1000 19 = 1700-2000 21 = 2000-2300 25 = 2300-2500 26 = 2650-2800 35 = 3300-3800	A = 0.56 x 0.35 B = 1.0 x 0.50 E = 0.56 x 0.20 L = 0.65 x 0.48 M= 0.40 x 0.20 P = 0.25 x 0.20	1 = 100 2 = 200 3 = 300	03 = 3dB 05 = 5dB 10 = 10dB 20 = 20dB 30 = 30dB	P = Tin Lead S = Immersion Tin

Example: X3C 19 P 1 - 03 S

Anaren®

Model XC0900A-20

Rev G

20 dB Directional Coupler

Xinger® II

Description

The XC0900A-20 is a low profile, high performance 20dB directional coupler in a new easy to use, manufacturing friendly surface mount package. It is designed for AMPS band applications. The XC0900A-20 is designed particularly for power and frequency detection, as well as for VSWR monitoring, where tightly controlled coupling and low insertion loss is required. It can be used in high power applications up to 200 Watts.

Parts have been subjected to rigorous qualification testing and they are manufactured using materials with coefficients of thermal expansion (CTE) compatible with common substrates such as FR4, G-10, RF-35, RO4350 and polyimide. Available in both 5 of 6 tin lead (XC0900A-20P) and 6 of 6 tin immersion (XC0900A-20S) RoHS compliant finishes.

Features:

- 800 – 1000 MHz
- AMPS
- High Power
- Very Low Loss
- Tight Coupling
- High Directivity
- Production Friendly
- Tape and Reel
- Available in Lead-Free (as illustrated) or Tin-Lead
- Reliable, FIT=0.41

Electrical Specifications **

Frequency	Mean Coupling	Insertion Loss	VSWR	Directivity
MHz	*dB*	*dB Max*	*Max : 1*	*dB Min*
800 - 1000	20.1 ± 0.60	0.18	1.15	23
700 – 800	20.7 ± 1.00	0.16	1.28	18
869 - 894	20.2 ± 0.60	0.14	1.12	23
925 - 960	20.2 ± 0.60	0.14	1.12	23
Frequency Sensitivity	**Power**	**ΘJC**	**Operating Temp.**	
dB Max	*Avg. CW Watts*	*ºC/Watt*	*ºC*	
± 0.20	150	16	-55 to +95	
± 0.40	200	16	-55 to +95	
± 0.05	200	16	-55 to +95	
± 0.05	200	16	-55 to +95	

**Specification based on performance of unit properly installed on Anaren Test Board 54606-0003. Refer to Specifications subject to change without notice. Refer to parameter definitions for details.

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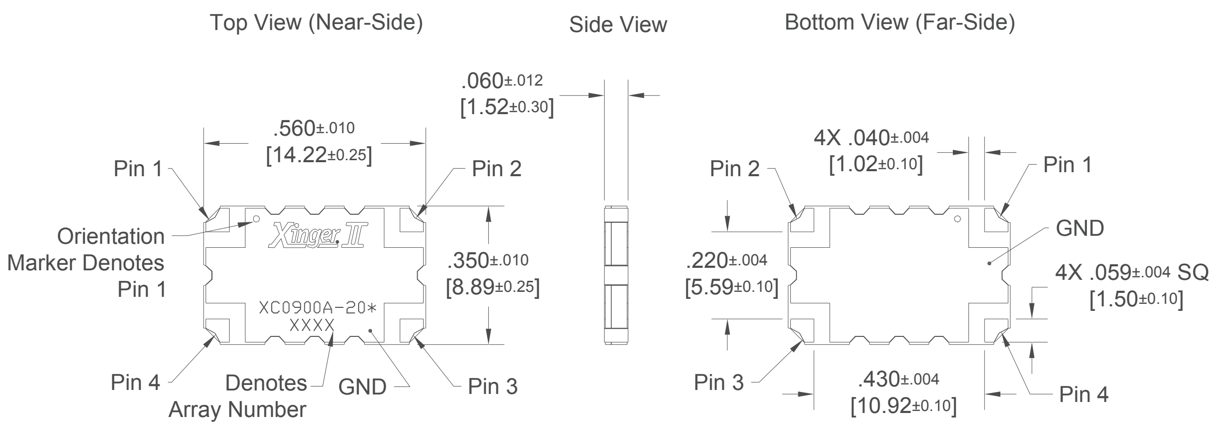


Dimensions are in Inches [Millimeters]
XC0900A-20* Mechanical Outline

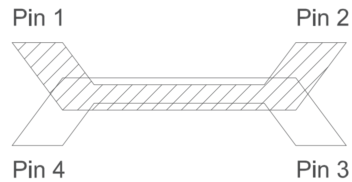
*For RoHS Compliant Versions order with S suffix
Tolerances are Non-Cumulative

USA/Canada: (315) 432-8909
Toll Free: (800) 411-6596
Europe: +44 2392-232392

Available on Tape and Reel for Pick and Place Manufacturing.

Directional Coupler Pin Configuration

The XC0900A-20 has an orientation marker to denote Pin 1. Once port one has been identified the other ports are known automatically. Please see the chart below for clarification:

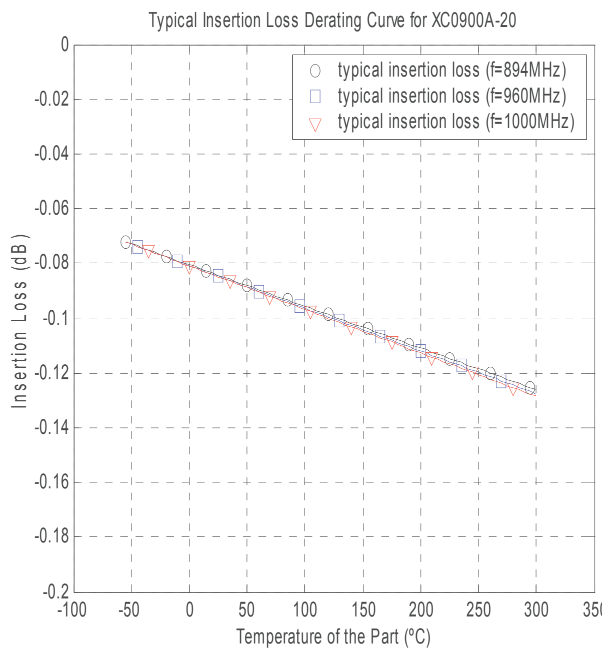


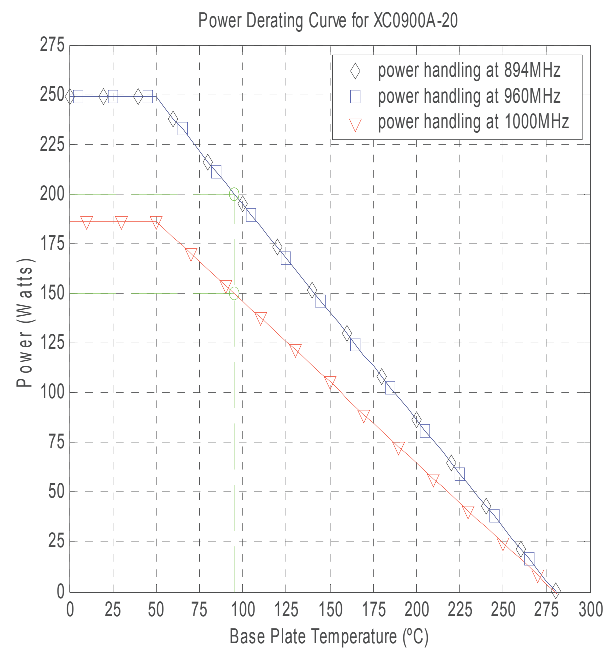
20dB Coupler Pin Configuration

Pin 1	Pin 2	Pin 3	Pin 4
Input	Direct	Isolated	Coupled
Direct	Input	Coupled	Isolated

Note: The direct port has a DC connection to the input port and the coupled port has a DC connection to the isolated port. For optimum performance use Pin 1 or Pin 2 as inputs.

Insertion Loss and Power Derating Curves





Insertion Loss Derating:

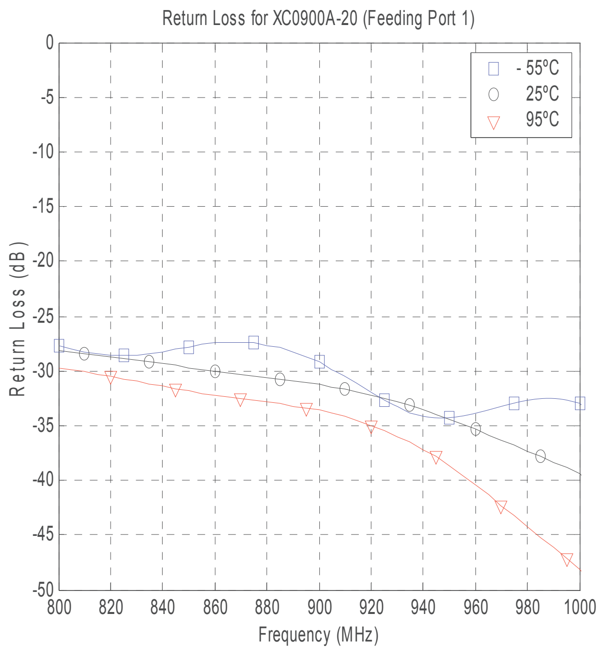
The insertion loss, at a given frequency, of a group of couplers is measured at 25°C and then averaged. The measurements are performed under small signal conditions (i.e. using a Vector Network Analyzer). The process is repeated at 95°C, 150°C, and 200°C. A best-fit line for the measured data is computed and then plotted from -55°C to 300°C.

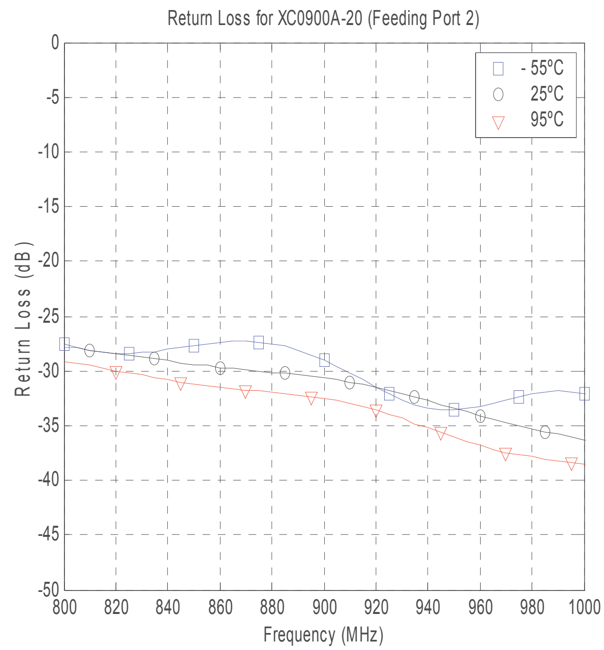
Power Derating:

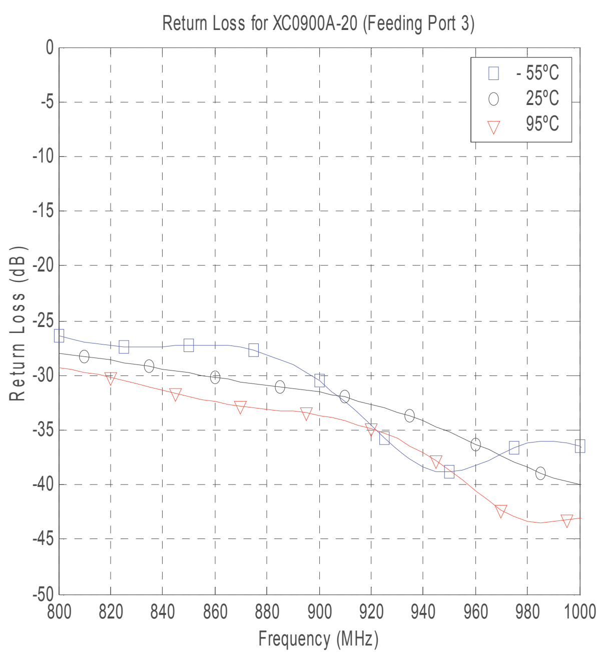
The power handling and corresponding power derating plots are a function of the thermal resistance, mounting surface temperature (base plate temperature), maximum continuous operating temperature of the coupler, and the thermal insertion loss. The thermal insertion loss is defined in the Power Handling section of the data sheet.

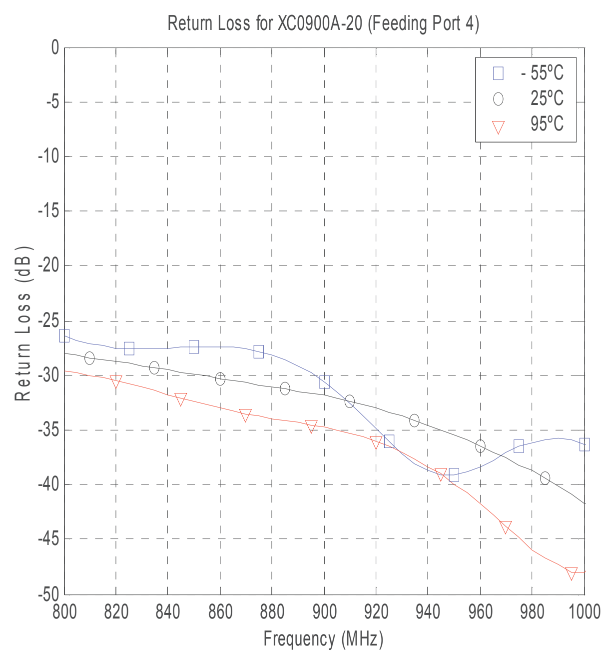
As the mounting interface temperature approaches the maximum continuous operating temperature, the power handling decreases to zero.

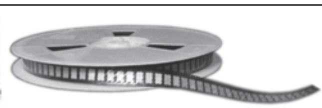
Typical Performance (-55°C, 25°C and 95°C): 800-1000 MHz



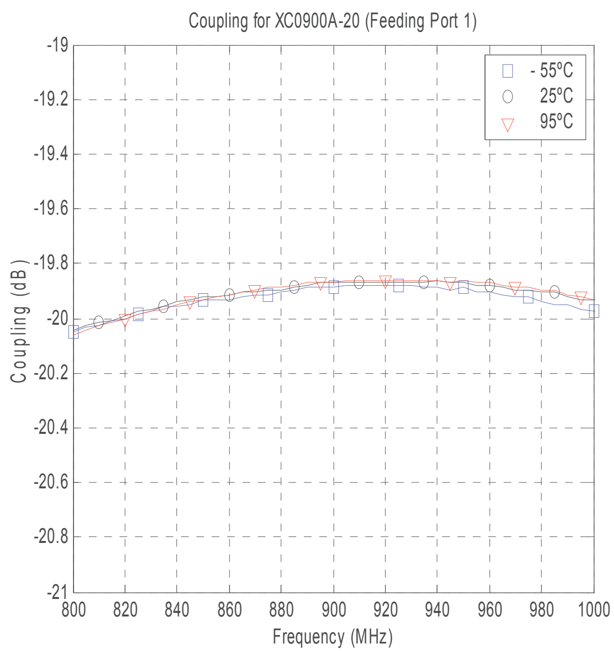


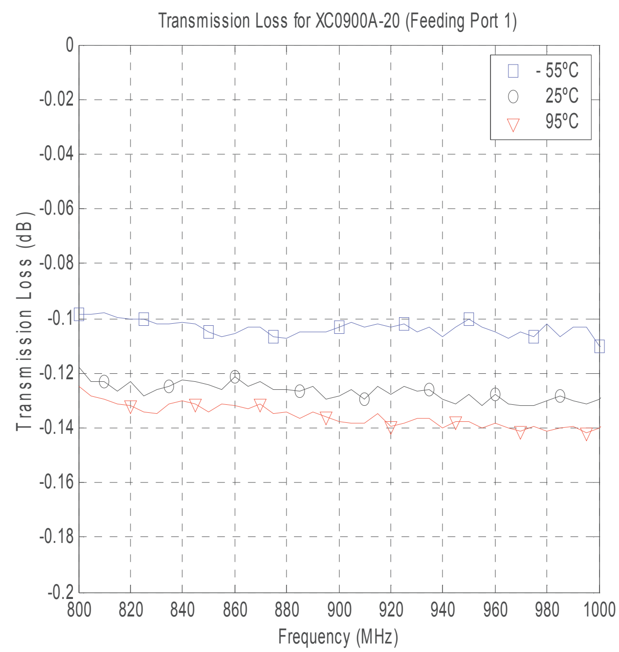


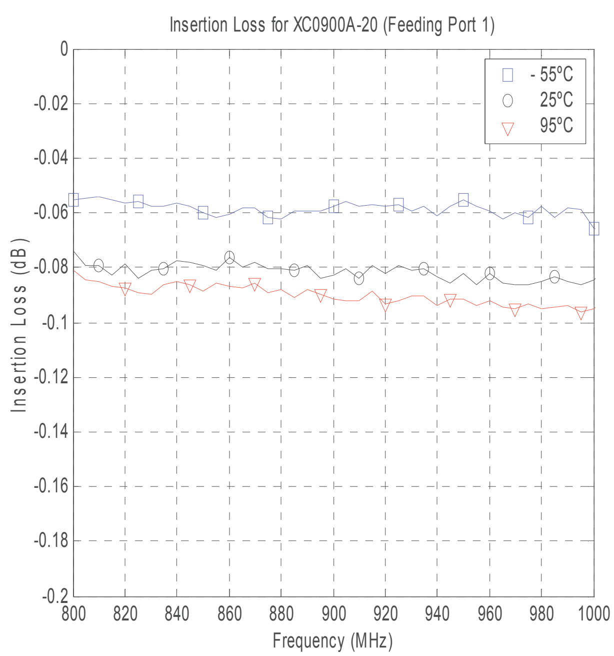


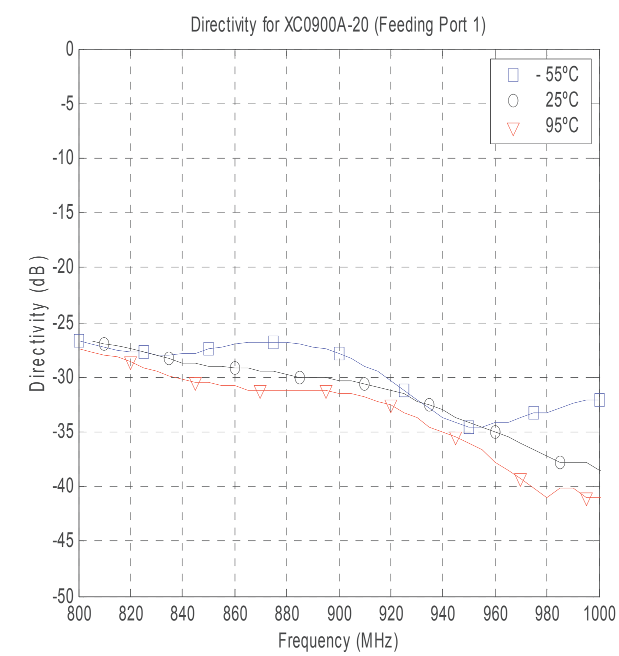


Typical Performance (-55°C, 25°C and 95°C): 800-1000 MHz



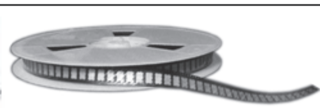






Definition of Measured Specifications

Parameter	Definition	Mathematical Representation
VSWR (Voltage Standing Wave Ratio)	The impedance match of the coupler to a 50Ω system. A VSWR of 1:1 is optimal.	$\text{VSWR} = \frac{V_{max}}{V_{min}}$ Vmax = voltage maxima of a standing wave Vmin = voltage minima of a standing wave
Return Loss	The impedance match of the coupler to a 50Ω system. Return Loss is an alternate means to express VSWR.	Return Loss (dB)= $20\log\frac{\text{VSWR}+1}{\text{VSWR}-1}$
Mean Coupling	At a given frequency (ω_n), coupling is the input power divided by the power at the coupled port. Mean coupling is the average value of the coupling values in the band. N is the number of frequencies in the band.	Coupling (dB) = $C(\omega_n) = 10\log\left(\frac{P_{in}(\omega_n)}{P_{cpl}(\omega_n)}\right)$ Mean Coupling (dB) = $\frac{\sum_{n=1}^{N} C(\omega_n)}{N}$
Insertion Loss	The input power divided by the sum of the power at the two output ports.	$10\log\frac{P_{in}}{P_{cpl}+P_{direct}}$
Transmission Loss	The input power divided by the power at the direct port.	$10\log\frac{P_{in}}{P_{direct}}$
Directivity	The power at the coupled port divided by the power at the isolated port.	$10\log\frac{P_{cpl}}{P_{iso}}$
Frequency Sensitivity	The decibel difference between the maximum in band coupling value and the mean coupling, and the decibel difference between the minimum in band coupling value and the mean coupling.	Max Coupling (dB) – Mean Coupling (dB) and Min Coupling (dB) – Mean Coupling (dB)



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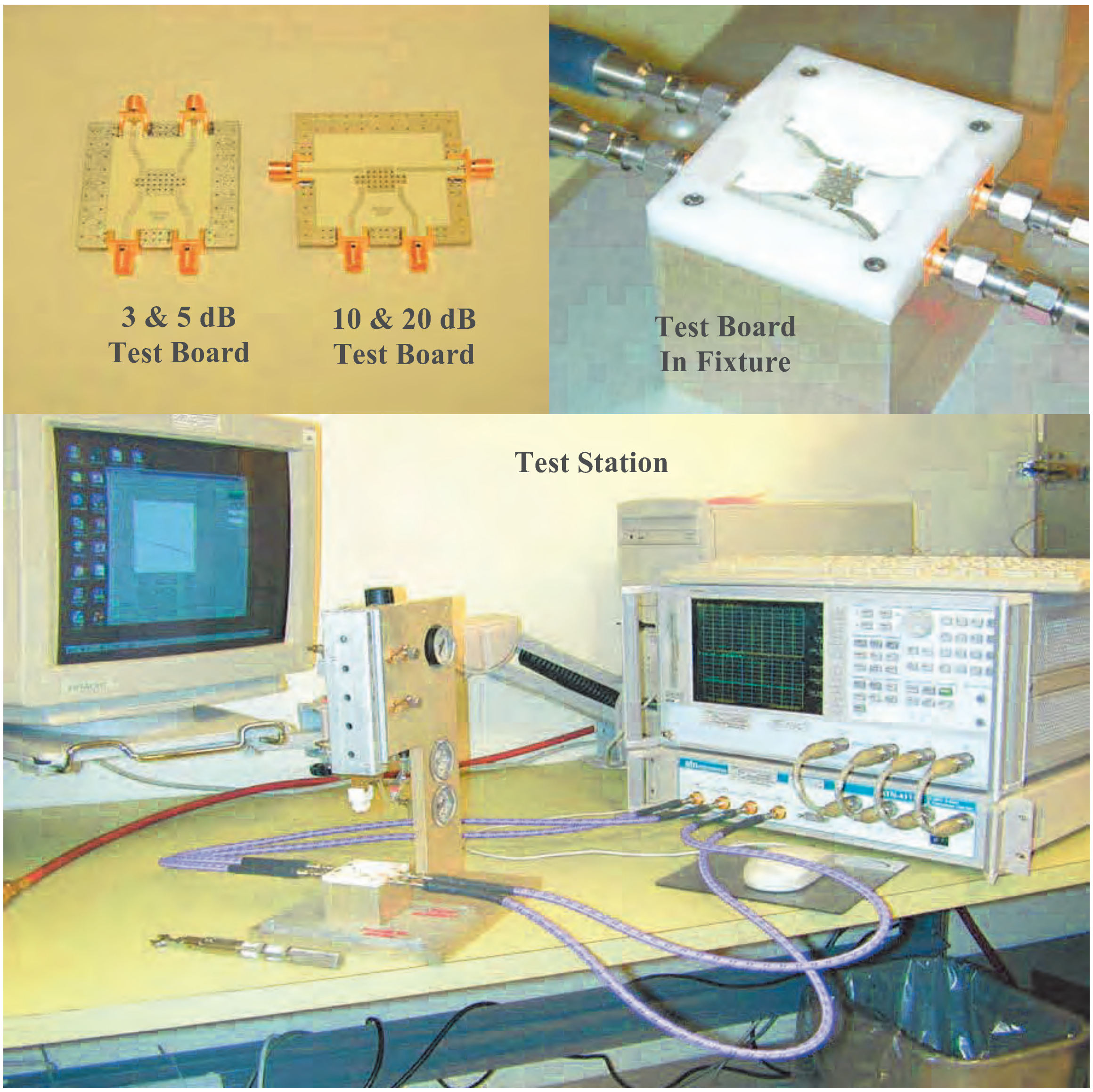
Notes on RF Testing and Circuit Layout

The XC0900A-20 Surface Mount Couplers require the use of a test fixture for verification of RF performance. This test fixture is designed to evaluate the coupler in the same environment that is recommended for installation. Enclosed inside the test fixture, is a circuit board that is fabricated using the recommended footprint. The part being tested is placed into the test fixture and pressure is applied to the top of the device using a pneumatic piston. A four port Vector Network Analyzer is connected to the fixture and is used to measure the S-parameters of the part. Worst case values for each parameter are found and compared to the specification. These worst case values are reported to the test equipment operator along with a Pass or Fail flag. See the illustrations below.



The effects of the test fixture on the measured data must be minimized in order to accurately determine the performance of the device under test. If the line impedance is anything other than 50Ω and/or there is a discontinuity at the microstrip to SMA interface, there will be errors in the data for the device under test. The test environment can never be “perfect”, but the procedure used to build and evaluate the test boards (outlined below) demonstrates an attempt to minimize the errors associated with testing these devices. The lower the signal level that is being measured, the more impact the fixture errors will have on the data. Parameters such as Return Loss and Isolation/Directivity, which are specified as low as 27dB and typically measure at much lower levels, will present the greatest measurement challenge.

The test fixture errors introduce an uncertainty to the measured data. Fixture errors can make the performance of the device under test look better or worse than it actually is. For example, if a device has a known return loss of 30dB and a discontinuity with a magnitude of –35dB is introduced into the measurement path, the new measured Return Loss data could read anywhere between –26dB and –37dB. This same discontinuity could introduce an insertion phase error of up to 1°.

There are different techniques used throughout the industry to minimize the affects of the test fixture on the measurement data. Anaren uses the following design and de-embedding criteria:

- Test boards have been designed and parameters specified to provide trace impedances of 50 ±1Ω. Furthermore, discontinuities at the SMA to microstrip interface are required to be less than –35dB and insertion phase errors (due to differences in the connector interface discontinuities and the electrical line length) should be less than ±0.25° from the median value of the four paths.

- A “Thru” circuit board is built. This is a two port, microstrip board that uses the same SMA to microstrip interface and has the same total length (insertion phase) as the actual test board. The “Thru” board must meet the same stringent requirements as the test board. The insertion loss and insertion phase of the “Thru” board are measured and stored. This data is used to completely de-embed the device under test from the test fixture. The de-embedded data is available in S-parameter form on the Anaren website (www.anaren.com).

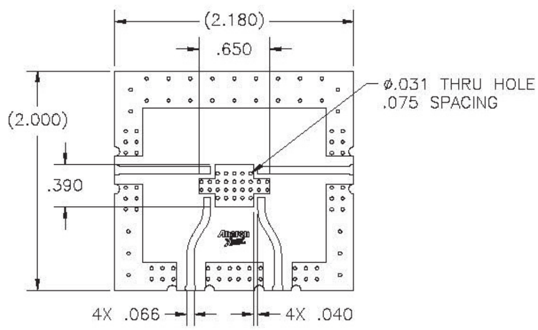
Note: The S-parameter files that are available on the anaren.com website include data for frequencies that are outside of the specified band. It is important to note that the test fixture is designed for optimum performance through 2.3GHz. Some degradation in the test fixture performance will occur above this frequency and connector interface discontinuities of –25dB or more can be expected. This larger discontinuity will affect the data at frequencies above 2.3GHz.

Circuit Board Layout

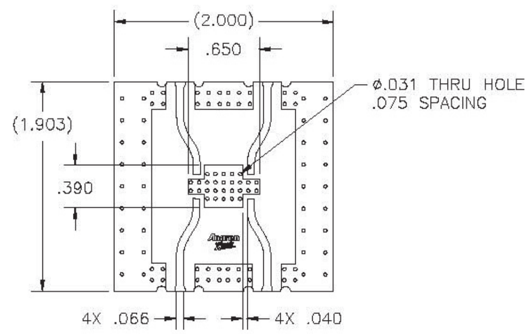
The dimensions for the Anaren test board are shown below. The test board is printed on Rogers RO4350 material that is 0.030” thick. Consider the case when a different material is used. First, the pad size must remain the same to accommodate the part. But, if the material thickness or dielectric constant (or both) changes, the reactance at the interface to the coupler will also change. Second, the linewidth required for 50Ω will be different and this will introduce a step in the line at the pad where the coupler interfaces with the printed microstrip trace. Both of these conditions will affect the performance of the part. **To achieve the specified performance, serious attention must be given to the design and layout of the circuit environment in which this component will be used.**

If a different circuit board material is used, an attempt should be made to achieve the same interface pad reactance that is present on the Anaren RO4350 test board. When thinner circuit board material is used, the ground plane will be closer to the pad yielding more capacitance for the same size interface pad. The same is true if the dielectric constant of the circuit board material is higher than is used on the Anaren test board. In both of these cases, narrowing the line before the interface pad will introduce a series inductance, which, when properly tuned, will compensate for the extra capacitive reactance. If a thicker circuit board or one with a lower dielectric constant is used, the interface pad will have less capacitive reactance than the Anaren test board. In this case, a wider section of line before the interface pad (or a larger interface pad) will introduce a shunt capacitance and when properly tuned will match the performance of the Anaren test board.

Notice that the board layout for the 3dB and 5dB couplers is different from that of the 10dB and 20dB couplers. The test board for the 3dB and 5dB couplers has all four traces interfacing with the coupler at the same angle. The test board for the 10dB and 20dB couplers has two traces approaching at one angle and the other two traces at a different angle. **The entry angle of the traces has a significant impact on the RF performance and these parts have been optimized for the layout used on the test boards shown below**.



10 & 20dB Test Board



3 & 5dB Test Board

Testing Sample Parts Supplied on Anaren Test Boards

If you have received a coupler installed on an Anaren produced microstrip test board, please remember to remove the loss of the test board from the measured data. The loss is small enough that it is not of concern for Return Loss and Isolation/Directivity, but it should certainly be considered when measuring coupling and calculating the insertion loss of the coupler. An S-parameter file for a “Thru” board (see description of “Thru” board above) will be supplied upon request. As a first order approximation, one should consider the following loss estimates:

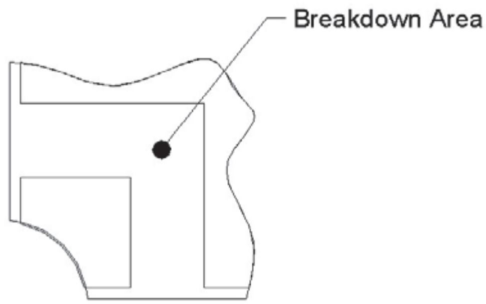
Frequency Band	Avg. Ins. Loss of Test Board @ 25°C
800 – 1000 MHz	~ 0.07dB
1700 – 2300 MHz	~ 0.12dB

For example, a 1900MHz, 10dB coupler on a test board may measure –10.30dB from input to the coupled port at some frequency, F1. When the loss of the test board is removed, the coupling at F1 becomes -10.18dB (-10.30dB + 0.12dB). This compensation must be made to both the coupled and direct path measurements when calculating insertion loss.

The loss estimates in the table above come from room temperature measurements. It is important to note that the loss of the test board will change with temperature. This fact must be considered if the coupler is to be evaluated at other temperatures.

Peak Power Handling

High-Pot testing of these couplers during the qualification procedure resulted in a minimum breakdown voltage of 1.7KV (minimum recorded value). This voltage level corresponds to a breakdown resistance capable of handling at least 12dB peaks over average power levels, for very short durations. The breakdown location consistently occurred across the air interface at the coupler contact pads (see illustration below). The breakdown levels at these points will be affected by any contamination in the gap area around these pads. These areas must be kept clean for optimum performance. It is recommended that the user test for voltage breakdown under the maximum operating conditions and over worst case modulation induced power peaking. This evaluation should also include extreme environmental conditions (such as high humidity).



Orientation Marker

A printed circular feature appears on the top surface of the coupler to designate Pin 1. This orientation marker is **not** intended to limit the use of the symmetry that these couplers exhibit but rather to facilitate consistent placement of these parts into the tape and reel package. This ensures that the components are always delivered with the same orientation. Refer to the table on page 2 of the data sheet for allowable pin configurations.

Test Plan

Xinger II couplers are manufactured in large panels and then separated. A sample population of parts is RF small signal tested at room temperature in the fixture described above. All parts are DC tested for shorts/opens. (See "Qualification Flow Chart" section for details on the accelerated life test procedures.)

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Power Handling

The average power handling (total input power) of a Xinger coupler is a function of:

- Internal circuit temperature.
- Unit mounting interface temperature.
- Unit thermal resistance
- Power dissipated within the unit.

All thermal calculations are based on the following assumptions:

- The unit has reached a steady state operating condition.
- Maximum mounting interface temperature is 95°C.
- Conduction Heat Transfer through the mounting interface.
- No Convection Heat Transfer.
- No Radiation Heat Transfer.
- The material properties are constant over the operating temperature range.

Finite element simulations are made for each unit. The simulation results are used to calculate the unit thermal resistance. The finite element simulation requires the following inputs:

- Unit material stack-up.
- Material properties.
- Circuit geometry.
- Mounting interface temperature.
- Thermal load (dissipated power).

The classical definition for dissipated power is temperature delta (ΔT) divided by thermal resistance (R). The dissipated power (P_{dis}) can also be calculated as a function of the total input power (P_{in}) and the thermal insertion loss (IL_{therm}):

$$P_{dis} = \frac{\Delta T}{R} = P_{in} \cdot \left(1 - 10^{\frac{-IL_{therm}}{10}}\right) \quad (W) \qquad (1)$$

Power flow and nomenclature for an "H" style coupler is shown in Figure 1.

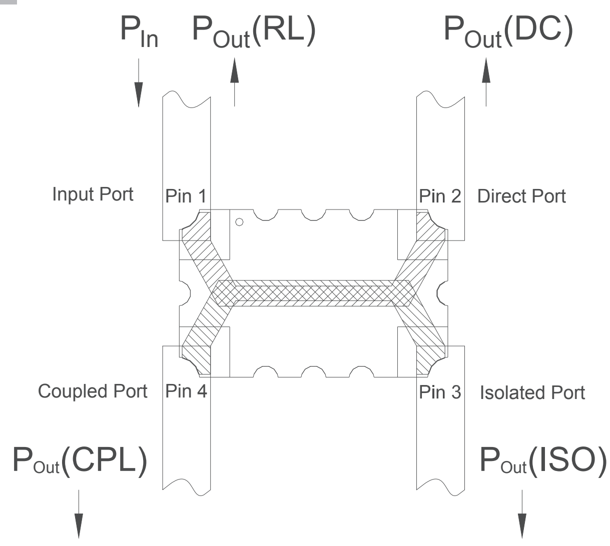


Figure 1

The coupler is excited at the input port with P_{in} (watts) of power. Assuming the coupler is not ideal, and that there are no radiation losses, power will exit the coupler at all four ports. Symbolically written, $P_{out(RL)}$ is the power that is returned to the source because of impedance mismatch, $P_{out(ISO)}$ is the power at the isolated port, $P_{out(CPL)}$ is the power at the coupled port, and $P_{out(DC)}$ is the power at the direct port.

At Anaren, insertion loss is defined as the log of the input power divided by the sum of the power at the coupled and direct ports:

Note: in this document, insertion loss is taken to be a positive number. In many places, insertion loss is written as a negative number. Obviously, a mere sign change equates the two quantities.

$$\mathrm{IL} = 10 \cdot \log_{10}\left(\frac{\mathrm{P_{in}}}{\mathrm{P_{out(CPL)}} + \mathrm{P_{out(DC)}}}\right) \quad (\mathrm{dB}) \qquad (2)$$

In terms of S-parameters, IL can be computed as follows:

$$\mathrm{IL} = -10 \cdot \log_{10}\left(|S_{31}|^2 + |S_{41}|^2 \right) \quad (\mathrm{dB}) \qquad (3)$$

We notice that this insertion loss value includes the power lost because of return loss as well as power lost to the isolated port.

For thermal calculations, we are only interested in the power lost "inside" the coupler. Since $P_{out(RL)}$ is lost in the source termination and $P_{out(ISO)}$ is lost in an external termination, they are not be included in the insertion loss for thermal calculations. Therefore, we define a new insertion loss value solely to be used for thermal calculations:

$$IL_{therm} = 10 \cdot \log_{10}\left(\frac{P_{in}}{P_{out(CPL)} + P_{out(DC)} + P_{out(ISO)} + P_{out(RL)}}\right) \quad (dB) \qquad (4)$$

In terms of S-parameters, IL_{therm} can be computed as follows:

$$IL_{therm} = -10 \cdot \log_{10}\left(|S_{11}|^2 + |S_{21}|^2 + |S_{31}|^2 + |S_{41}|^2 \right) \quad (dB) \tag{5}$$

The thermal resistance and power dissipated within the unit are then used to calculate the average total input power of the unit. The average total steady state input power (P_{in}) therefore is:

$$P_{in} = \frac{P_{dis}}{\left(1 - 10^{\frac{-IL_{therm}}{10}}\right)} = \frac{\frac{\Delta T}{R}}{\left(1 - 10^{\frac{-IL_{therm}}{10}}\right)} \quad (W) \tag{6}$$

Where the temperature delta is the circuit temperature (T_{circ}) minus the mounting interface temperature (T_{mnt}):

$$\Delta T = T_{circ} - T_{mnt} \quad ({}^{o}C) \tag{7}$$

The maximum allowable circuit temperature is defined by the properties of the materials used to construct the unit. Multiple material combinations and bonding techniques are used within the Xinger II product family to optimize RF performance. Consequently the maximum allowable circuit temperature varies. Please note that the circuit temperature is not a function of the Xinger case (top surface) temperature. Therefore, the case temperature cannot be used as a boundary condition for power handling calculations.

Due to the numerous board materials and mounting configurations used in specific customer configurations, it is the end users responsibility to ensure that the Xinger II coupler mounting interface temperature is maintained within the limits defined on the power derating plots for the required average power handling. Additionally appropriate solder composition is required to prevent reflow or fatigue failure at the RF ports. Finally, reliability is improved when the mounting interface and RF port temperatures are kept to a minimum.

The power-derating curve illustrates how changes in the mounting interface temperature result in converse changes of the power handling of the coupler.

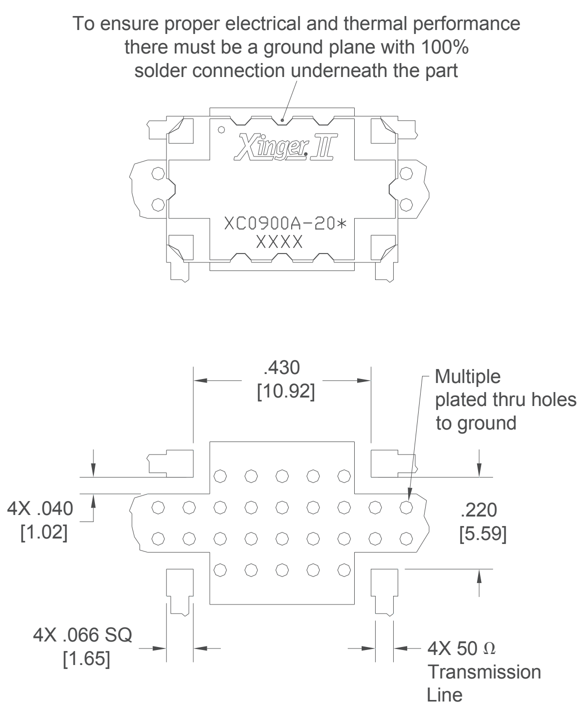
Mounting

In order for Xinger surface mount couplers to work optimally, there must be 50Ω transmission lines leading to and from all of the RF ports. Also, there must be a very good ground plane underneath the part to ensure proper electrical performance. If either of these two conditions is not satisfied, insertion loss, coupling, VSWR and isolation may not meet published specifications.

Overall ground is improved if a dense population of plated through holes connect the top and bottom ground layers of the PCB. This minimizes ground inductance and improves ground continuity. All of the Xinger hybrid and directional couplers are constructed from ceramic filled PTFE composites which possess excellent electrical and mechanical stability having X and Y thermal coefficient of expansion (CTE) of 17-25 ppm/^{o}C.

When a surface mount hybrid coupler is mounted to a printed circuit board, the primary concerns are; ensuring the RF pads of the device are in contact with the circuit trace of the PCB and insuring the ground plane of neither the component nor the PCB is in contact with the RF signal.

Mounting Footprint



Dimensions are in Inches [Millimeters]
XC0900A-20* Mounting Footprint

Coupler Mounting Process

The process for assembling this component is a conventional surface mount process as shown in Figure 1. This process is conducive to both low and high volume usage.

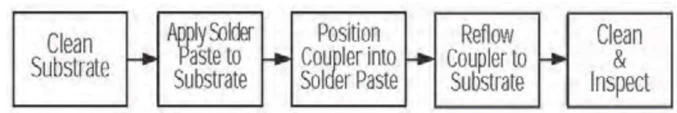


Figure 1: Surface Mounting Process Steps

Storage of Components: The Xinger II products are available in either an immersion tin or tin-lead finish. Commonly used storage procedures used to control oxidation should be followed for these surface mount components. The storage temperatures should be held between 15^{o}C and 60^{o}C.

Substrate: Depending upon the particular component, the circuit material has an x and y coefficient of thermal expansion of between 17 and 25 ppm/°C. This coefficient minimizes solder joint stresses due to similar expansion rates of most commonly used board substrates such as RF35, RO4350, FR4, polyimide and G-10 materials. Mounting to "hard" substrates (alumina etc.) is possible depending upon operational temperature requirements. The solder surfaces of the coupler are all copper plated with either an immersion tin or tin-lead exterior finish.

Solder Paste: All conventional solder paste formulations will work well with Anaren's Xinger II surface mount components. Solder paste can be applied with stencils or syringe dispensers. An example of a stenciled solder paste deposit is shown in Figure 2. As shown in the figure solder paste is applied to the four RF pads and the entire ground plane underneath the body of the part.

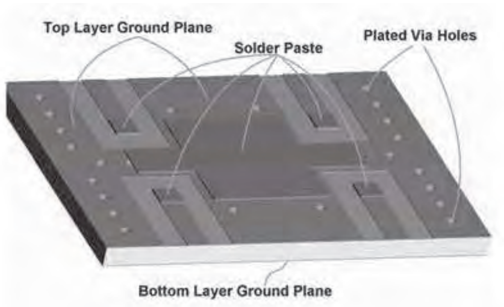


Figure 2: Solder Paste Application

Coupler Positioning: The surface mount coupler can be placed manually or with automatic pick and place mechanisms. Couplers should be placed (see Figure 3 and 4) onto wet paste with common surface mount techniques and parameters. Pick and place systems must supply adequate vacuum to hold a 0.50-0.55 gram coupler.

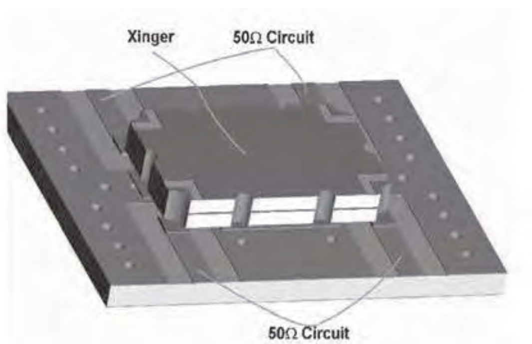


Figure 3: Component Placement

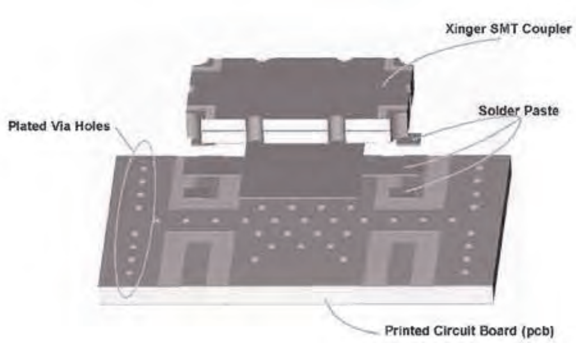


Figure 4: Mounting Features Example

Reflow: The surface mount coupler is conducive to most of today's conventional reflow methods. A low and high temperature thermal reflow profile are shown in Figures 5 and 6, respectively. Manual soldering of these components can be done with conventional surface mount non-contact hot air soldering tools. Board pre-heating is highly recommended for these selective hot air soldering methods. Manual soldering with conventional irons should be avoided.

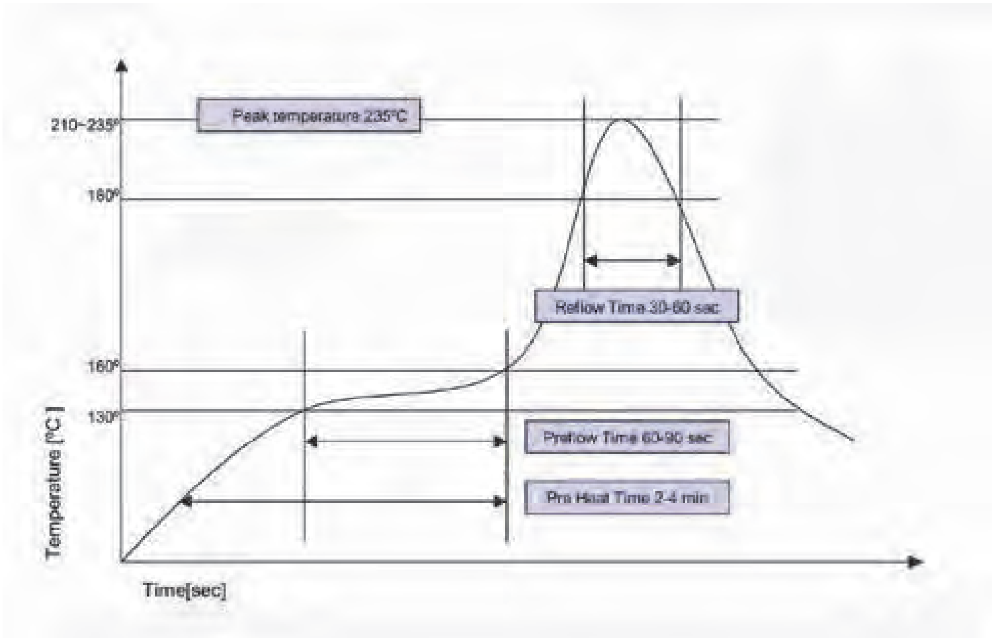


Figure 5 – Low Temperature Solder Reflow Thermal Profile

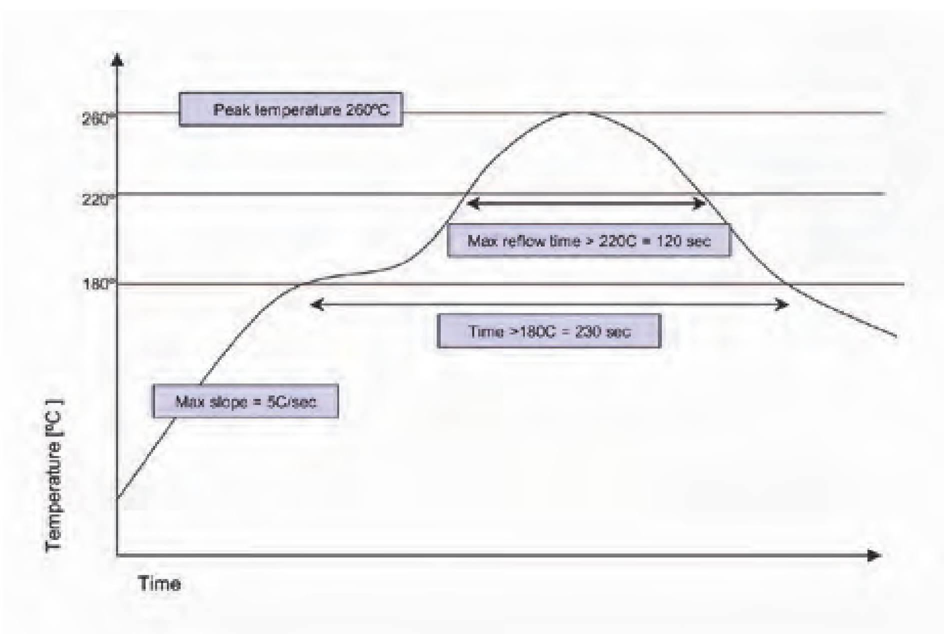
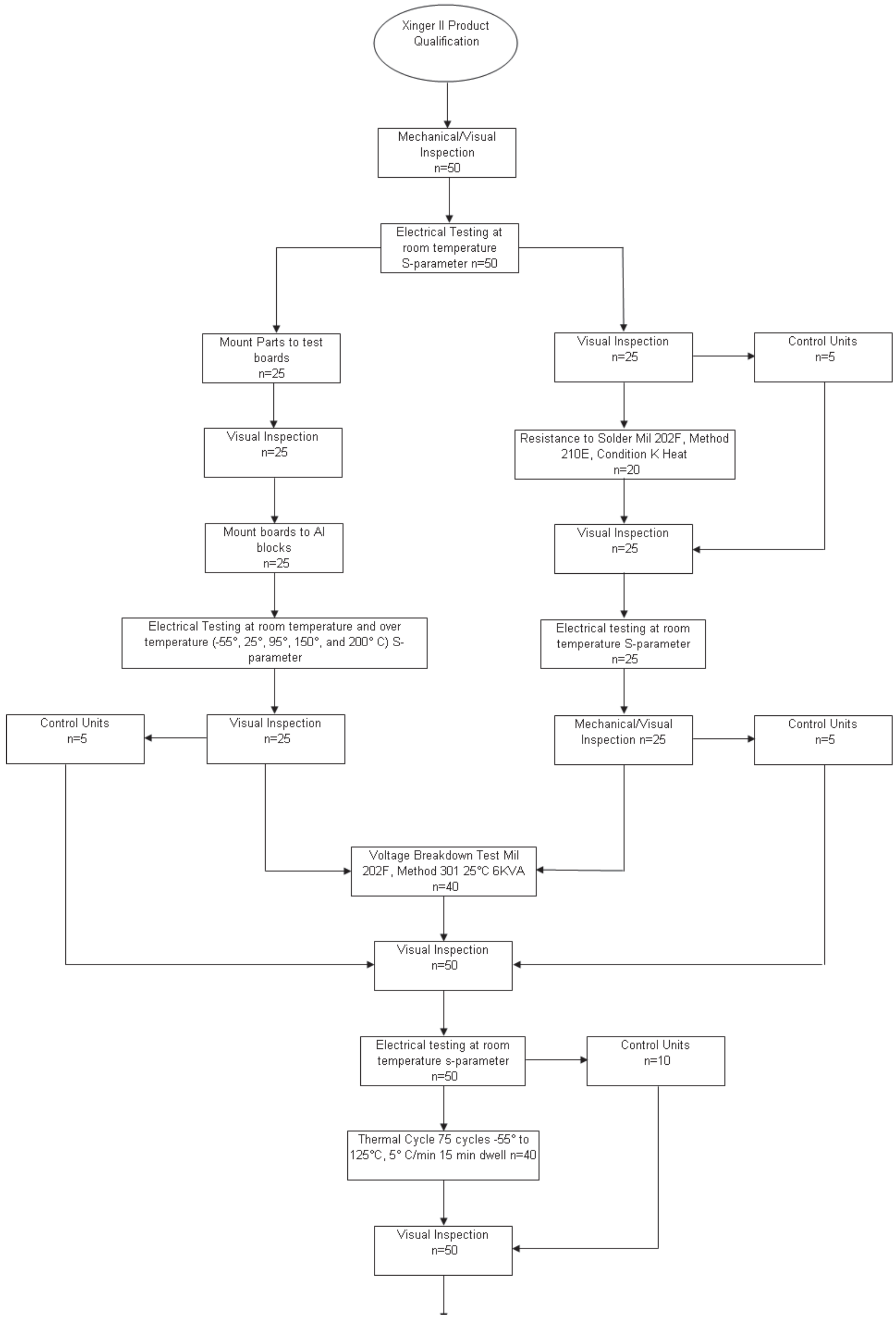
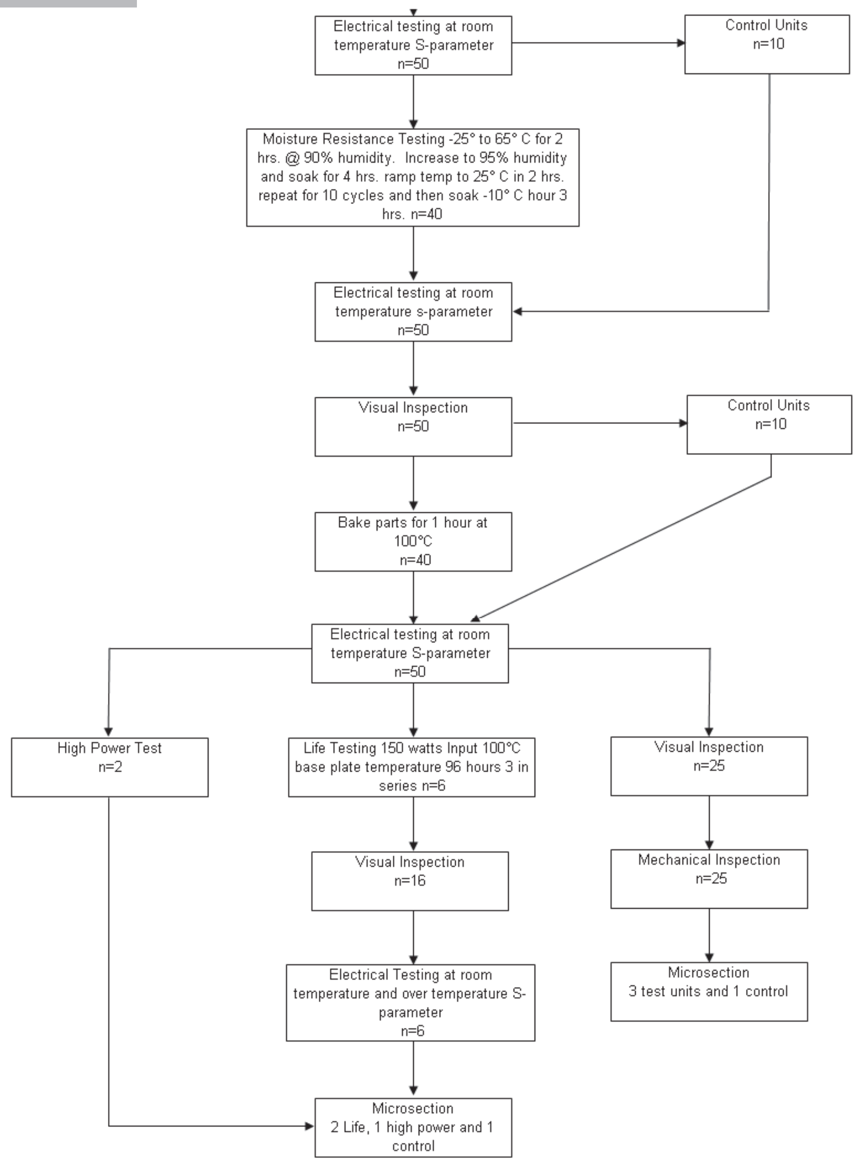


Figure 6 – High Temperature Solder Reflow Thermal Profile

Qualification Flow Chart




Electrical testing at room temperature S-parameter n=50
Control Units n=10
Moisture Resistance Testing -25° to 65° C for 2 hrs. @ 90% humidity. Increase to 95% humidity and soak for 4 hrs. ramp temp to 25° C in 2 hrs. repeat for 10 cycles and then soak -10° C hour 3 hrs. n=40
Electrical testing at room temperature s-parameter n=50
Visual Inspection n=50
Control Units n=10
Bake parts for 1 hour at 100°C n=40
Electrical testing at room temperature S-parameter n=50
High Power Test n=2
Life Testing 150 watts Input 100°C base plate temperature 96 hours 3 in series n=6
Visual Inspection n=25
Visual Inspection n=16
Mechanical Inspection n=25
Electrical Testing at room temperature and over temperature S-parameter n=6
Microsection 3 test units and 1 control
Microsection 2 Life, 1 high power and 1 control

Application Information

Directional Couplers and Sampling

Directional couplers are often used in circuits that require the sampling of an arbitrary signal. Because they are passive, non-linear devices, Anaren directional couplers do not perturb the characteristics of the signal to be sampled, and can be used for frequency monitoring and/or measurement of RF power. An example of a sampling circuit is the reflectometer. The purpose of the reflectometer is to isolate and sample the incident and reflected signals from a mismatched load. A basic reflectometer circuit is shown in Figure ap.n.1-1.

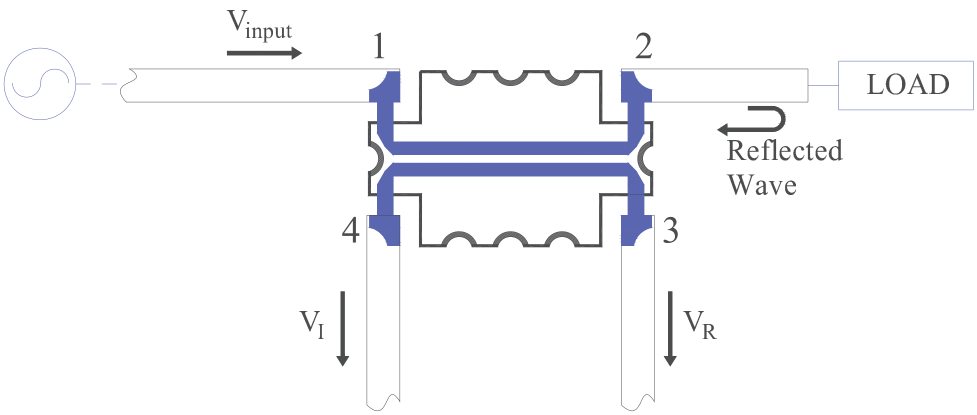


Figure ap.n.1-1. A Reflectometer Circuit Schematic

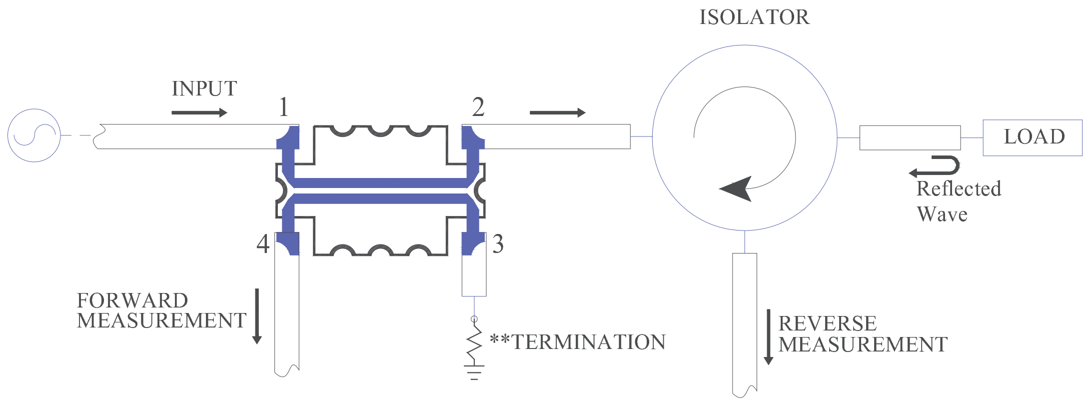
If the directional coupler has perfect directivity, then it is clear that V_I is strictly a sample of the incident voltage V_{input}, and V_R is strictly a sample of the wave that is reflected from the load. Since directivity is never perfect in practice, both V_I and V_R will contain samples of the input signal as well as the reflected signal. In that case,

$$V_I = \mathrm{C} + \mathrm{CDT}\Gamma e^{j\theta} \quad \text{Eq. ap.n.1-1}$$

and

$$V_R = \mathrm{CD} + \mathrm{CT}\Gamma e^{j\phi} \quad \text{Eq. ap.n.1-2}$$

where C is the coupling, D is the directivity, Γ is the complex reflection coefficient of the load, T is the transmission coefficient, and ϕ and θ are unknown phase delay differences caused by the interconnect lines on the test board. If we know V_I and V_R, we can easily calculate the reflection coefficient of the load. One should notice that in order to make forward and reverse measurements using only one coupler, the directivity must be really low. In specific customer applications, the preferred method for forward and reverse sampling is shown in Figure ap.n.1-2.



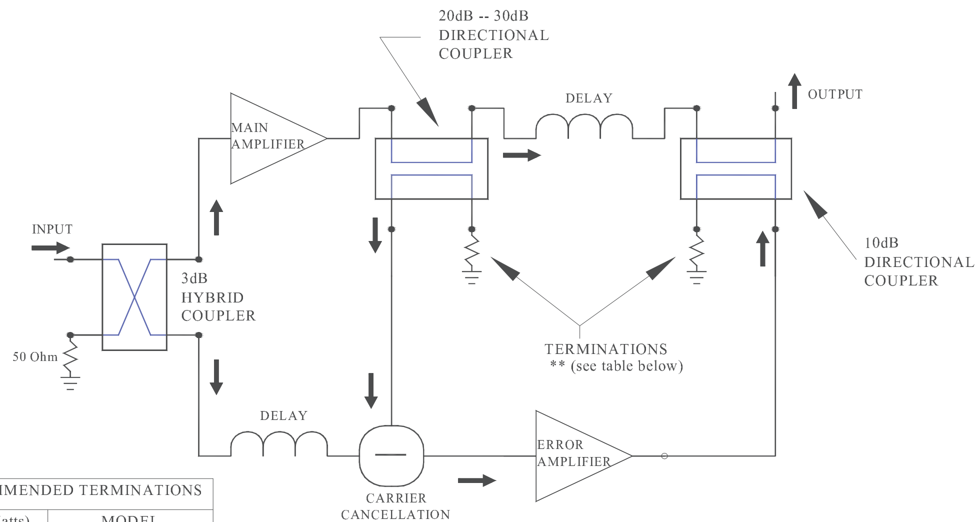
** RECOMMENDED TERMINATIONS	
Power (Watts)	MODEL
8	RFP-060120A15Z50
15	RFP-250375A4Z50
50	RFP-375375A6Z50
150	RFP-500500A6Z50

Figure ap.n.1-2. Forward and Reverse Sampling

The isolator in Figure ap.n.1-2 prevents the reflected wave from exciting the directional coupler. A list of recommended terminations is shown in the figure.

Directional Couplers in Feed-Forward Amplifier Applications

Feed-forward amplifiers are widely used to reduce distortion due to nonlinearities in power amplifiers. Although the level and complexity of feed-forward amplifiers varies from one manufacturer to another, the basic building block for this linearization scheme remains the same. A basic feed-forward schematic is shown in Figure ap.n.2-1. The input signal is split in two using a hybrid coupler or power divider. The output of the main amplifier is sampled with a 20dB-30dB directional coupler. The XC0900A-20 is an excellent candidate for this sampling since it provides great return loss and directivity. The sampled signal, which consists of a sample of the original input signal plus some distortion, is inverted and then combined with the output of the first delay line. This procedure subtracts (through destructive interference) the sample of the original input signal, leaving only the distortion or error component. The error component is then amplified and combined with the output of the second delay line using another directional coupler. In many cases, a 10dB coupler is used to combine the two signals. The XC0900A-10 is a perfect choice for this injection because it has tight coupling, superior directivity, and excellent match.



** RECOMMENDED TERMINATIONS	
Power (Watts)	MODEL
8	RFP-060120A15Z50
15	RFP-250375A4Z50
50	RFP-375375A6Z50
100	RFP-500500A6Z50

Figure ap.n.2-1. Generic Feed Forward Circuit Schematic

Both directional couplers in the Figure ap.n.2-1 have one port terminated with a 50Ω resistor. In order to achieve optimum performance, the termination must be chosen carefully. It is important to remember that a good termination will not only produce a good match at the input of the coupler, but will also maximize the isolation between the input port and isolated port. Furthermore, since the termination can potentially absorb high levels of power, its maximum power rating should be chosen accordingly. A list of recommended terminations is shown in Figure ap.n.2-1. For an ideal lossless directional coupler, the power at the coupled and direct ports can be written as:

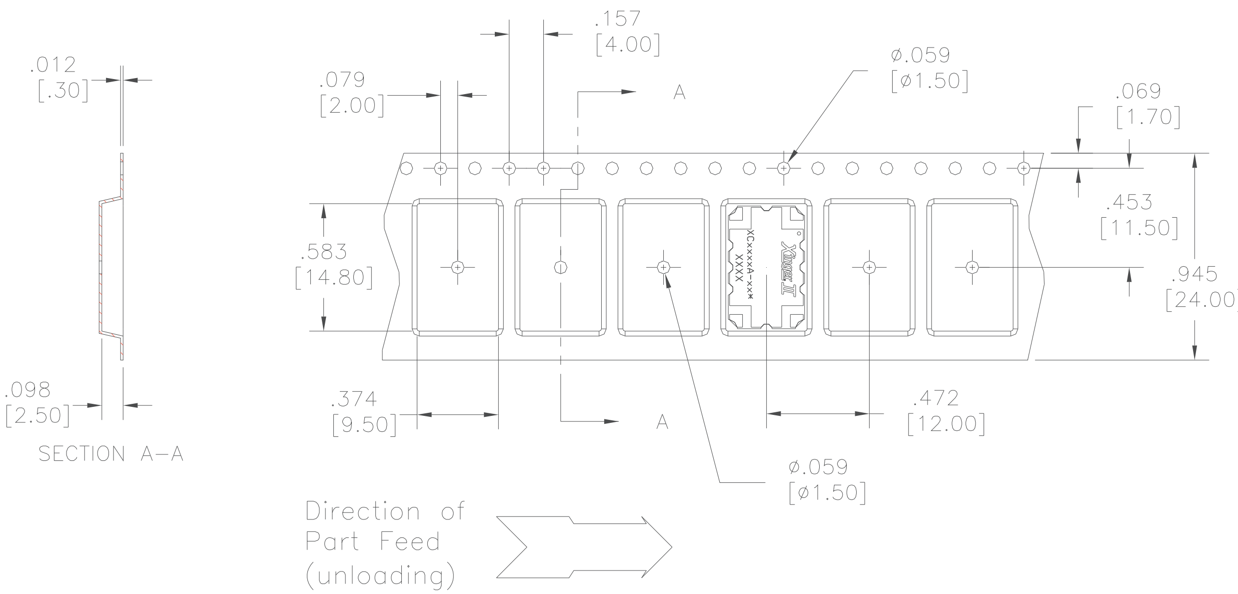
$$P_{coupled} = \frac{P_{input}}{10^{\frac{|\mathrm{Coupling}(dB)|}{10}}} \quad Watts \qquad \text{Eq. ap.n.2-1}$$

$$P_{direct} = P_{input} - \frac{P_{input}}{10^{\frac{|\mathrm{Coupling}(dB)|}{10}}} \quad Watts \qquad \text{Eq. ap.n.2-2}$$

where P_{input} is the input power in Watts, and Coupling(dB) is the coupling value in dB.

Packaging and Ordering Information

Parts are available in both reel and tube. Packaging follows EIA 481-2. Parts are oriented in tape and reel as shown below. Minimum order quantities are 2000 per reel and 30 per tube. See Model Numbers below for further ordering information.



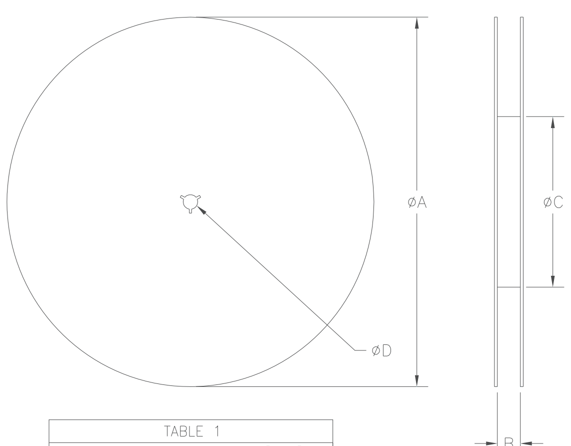


TABLE 1	
REEL DIMENSIONS (inches [mm])	
øA	13.3 [333.0]
B	0.945 [24.0]
øC	4.017 [102.03]
øD	0.512 [13.0]

XX XXXX X - XX X

Xinger Coupler	Frequency (MHz)	Size (Inches)	Coupling Value	Plating Finish
XC	0450 = 410-480 0900 = 800-1000 1900 = 1700-2000 2100 = 2000-2300 2500 = 2300-2700 3500 = 3300-3700	A = 0.56 x 0.35 B = 1.0 x 0.50 E = 0.56 x 0.20 L = 0.65 x 0.48 M= 0.40 x 0.20 P = 0.25 x 0.20	03 = 3dB 05 = 5dB 10 = 10dB 20 = 20dB 30 = 30dB	P = Tin Lead S = Immersion Tin

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