Title	**HD500-2 SP500 PM500 Test Spec**		
Doc Number	**TS00185**	**Issue**	**2**

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Approvals

Contents	**Initials**	**Date**
Part 1: Description of Operation	**KOF**	**15 Apr 2003**
Part 2: Test Equipment	**KOF**	**15 Apr 2003**
Part 3: Test Requirements	**KOF**	**15 Apr 2003**

Index

Revision Record

Rev	Date	init	comment
2	19 Jan 2004	PMB	CN00xxx All PIC references modified to include newer PICs
1	20 May 2003	KOF	Added config types (HD SP PM PR)
1	15 April 2003	KOF	not issued
draft	17 Jan 2003	KOF	unfinished and untested jig

1. Description of Operation

Summary

This description of operation uses component references as per CD00153_2.

The same PCA will be used on the HD500-2, the SP500 and the PM500. As these have different metal surrounds the range will differ. The PM uses a different antenna coil. In all other respects they are the same. In the description HD500-2 may be interpretted as SP500 or PM500.

The HD500-2 is intended to provide tag reading and interface functionality somewhat similar to the 5291. It has reduced functionality in some respects. It is preferable not to assume that functions are the same,

The HD500-2 is capable of reading ND and AD tag types. Tag reading is under control of a PIC (U9). This PIC turns on the TX drive and translates the return signal. The decoded signal is conveyed to a second PIC (U11), which manages the user interface (LEDs and sounder), and also the data interface.

The transmit drive uses a traditional series tuned circuit, driven by a gated square wave at 132 kHz. The receive signal at 66 kHz is picked up on a small coil. The signal is passed through a band pass circuit, based mostly on a MAX274 (U3), before being peak-detected (U4) and converted to a digital signal (U8). Note that there is a possibility that at some point the peak-detection process may be replaced by a transition counter in the PIC (U9). If this is the case then there will be circuit changes to include removal of the peak detection diodes and U8.

Power Supply

The power supply is specified to be 10.5V to 35.0V. The published specification max is to be 31.2V. This apparently very high operating voltage is aimed at the Swedish market, which uses 24V battery backed power supplies instead of the more usual 12V in other markets. Maximum charging voltage for a 24V lead-acid battery should be 31.2V.

Current consumption for the reader will be largely dependent on the peripherals in use, especially the LEDs. Normal operation for one LED and no other peripherals will be nominal 40 mA. Budget max current is 65 mA.

In order to disperse the heat under max conditions the power is dissipated in two regulators, both of which have wire heatsinks fitted. The potting compound is also required to dissipate the heat. However, it should be possible to operate the unpotted unit at room temperature for the purpose of testing. It is not recommended that unpotted units are provided to customers for any reason.

Regulator U10 has a 15V output. This regulator will disperse most of the excess power when operating at maximum voltage. When operating at less that approx 17V the regulator will only drop it's 'drop-out' voltage which will be 2V nominal. Note that some older regulator designs exhibit uncontrolled behaviour when the input voltage is less than the design output voltage, for instance, excessive current consumption may occur. Alternative regulator types should be tested across the range.

Fault current is limited by F1. This has been chosen, as we are familiar with this device when potted. Smaller (more expensive) parts are now available, but the operating membrane is more exposed. This fuse is rated to trip at 0.6 A, however when encapsulated in potting compound the action can be delayed both in terms of time and operating current due to the thermal conductivity of the compound. Measurements on the prototype have revealed a max short circuit current of 0.5A can be achieved before the fuse trips. Historic 5291 measurements reveal a potential 0.85 current max. Therefore any external wiring should be capable of operating with continuous 1A. (Ground voltage-drop considerations in normal operation may further increase the current carrying requirement.)

Reverse connection is protected against by D19. This is provided even though many voltage regulators have intrinsic reverse connection, in order to allow widest possible choice. Note that if selecting an alternative for this part, Schottky types should be avoided due to the high reverse leakage, which is temperature dependent. Operation at high reverse voltage and temperature of schottky diodes is likely to lead to failure to short circuit.

Transient protection is provided by D18. This will have a nominal 32V operation, but is guaranteed 1mA max at 36V.

Note it may be possible to translate this design to 5V operation, but this has not been tested nor detail design checked through. Low dropout regulators are available to fit either U10 or U6, linking out the other regulator. with R57 or R1. MIC5209 in U6 location looks like a good candidate.

Transmitter circuit

The clock for the transmitter originates at OSC2 on U11. At this point the signal looks like a 5Vpp rough sinusoid, at 7.392 MHz. Half of U7 divides this by 2 to give 3.969 MHz. Which being less than 4 MHz can be used as a clock for the PIC (U9).

Shift register U5 together with Q1 divides this by 14 to give 264 kHz[1]. Then the other half of U7 further divides by 2 to give 132 kHz. The transmitter gate, or envelope control TXG originates at U9,6[2]. In order to ensure the shift register U5 does not power up with a random number, which would lead to reduced Tx and increased spurious emissions, the turn-on pulse of TXG also causes the shift register to clear to zero. This is enabled by means of a short pulse allowed through C29. R56 and D16 keep the pulse to normal logic levels.

U1 translates[3] the CMOS high impedance drive to a low impedance drive to the Tx circuit. The transmit circuit consists mainly of L4 in series tuned with C5 and C6. Parallel capacitors C7 C8 are made available in to give some flexibility in case of difficulty obtaining the first choice. The transmit capacitors are split before and after the coil in order to reduce the emitted electric field, mainly so as to reduce coupling into the Rx circuit. This technique will also reduce the electric field at a distance[4] at 132 kHz. In addition, the required operating voltage is halved, but at the expense of twice the required capacitance. In the absence of a metal surround expect to see 60 Vpp on C6 referred to ground. C8 will have a similar (anti-phase) voltage, but the square wave drive will also be mixed in. The Tx field is capable of activating a 928 tag at 30cm or more.

[1] 264 kHz was to be used for synchronous power conversion, but this was not implemented.
[2] Note the envelope control does not halt the 264 kHz clock.
[3] The cost of this part has increased significantly. It is likely that this can be done more cheaply.
[4] Less of a problem legally nowadays. Some countries (Belgium) used to measure this and impose stringent limits.

The transmit circuit is targetted to tune to 132 kHz when the metal frame is fitted. The metal frame, will reduce the Tx coil inductance at 132 kHz. Note that change of metal type, particularly from non-magnetic to magnetic, will affect tuning.
L2 C25 attenuate high frequency components of the square wave drive, so as to avoid infringing emitted spurious RF limits. R3 is required to damp the resonance of L5 C25, which would otherwise create a band of failing frequencies. L1 C4 attenuate the conducted emissions both to avoid conducted emissions limits, and to reduce the internal effect on the power supply.

Receiver Circuit

The 66 kHz receive signal is picked up in L3, which looks not unlike a 928 tag coil. This is coupled and tuned with C11 C9 into the virtual earth of U2 input. The input impedance of this circuit is defined primarily by the coil loss of L3. This has been measured to be 50 ohm nominal at 66 kHz. R29 is available to increase this, however this has not been used.

The preamp U2 is required, as the following filter chip is quite noisy. The gain of the preamp is defined by the Rx coil impedance together with C10 impedance. This is done in preference to using a resistor as the gain at 132 kHz will be half that at 66 kHz so that the risk of Tx saturation of the input circuit is reduced. The effect of Tx saturation would be to reduce the apparent signal level. In this design, the Rx coil position is fixed in a location intended to be at or close to the null position of the Tx. The nominal gain of the preamp is 48 at 66 kHz.

The following MAX274 chip is a state-variable filter consisting of 4 identical stages. This is a complex circuit and readers should refer to the full specification if contemplating changes. See the Maxim data book "New Releases 1993". Copies of the relevant pages are also held in the Engineering data file for N148.

A summary of the more useful equations follows. Note that the databook references are used, not those in CD00153.

$$F0\ (Hz) = \left(\sqrt{\left(1/([R2]*[R4 + 5k\Omega\ ])\right)}\right)*2\ e9 \qquad \text{Gain at F0} = (R3/R1)$$

$$Q = \left(\sqrt{\left(1/([R2]*[R4 + 5k\Omega])\right)}\right)*R3*(RY/RX)$$

As we are using this device towards the top end of its working frequency range there will be errors introduced by the limited GBW of the op amps in the circuit. It has been found by comparing results to simulation that 180 is an appropriate value to use. This will give an F0 close to 66kHz, while the equation above suggests 67kHz.

Stray capacitance will also have some effect, particularly when tight bandwidths are attempted. This will be layout dependent, but as a start-point 4 pF overall input to output is suggested.

Nominal values of RY/RX (kΩ) in this configuration are 65/13
Chosen values R2 = 33k 1%. R4 = 22k 1%. R3 = 22 k 5% (or 1%) R1 = 6k8 5%

In each stage, two resistors determine the operating frequency of 66 kHz. These are thus 1% components, e.g. R9 R10. The other two components in each stage determine the gain and bandwidth[5], and so may be 5% components as this is less critical. E.g. R7 R8. There are three ranges of gain and bandwidth one of which is chosen by setting PC to pseudo-ground.

[5] Values differ from 5291 as the bandwidth has been increased to accommodate x6 tags.

Nominal stage at gain at 66 kHz is 3.24, and thus 4-stage gain 109.6.

Gain at 132 kHz is approx -5 dB per stage, and so provided the Tx coupling into the Rx remains below approx 3Vpp then the Tx level at the output of the MAX274 will not be significant.

The output from the MAX274 is fed into a peak detector arranged around U4. Noise or signal at the input will have no effect until the amplitude reaches approx 800 mV pp. this minimum amplitude it set by an offset introduced by R28. The feedback diodes around U4 are required to prevent the amplifier from going into saturation, which can require excessive time to recover. In addition, the amplifier may suffer output inversion if this is allowed[6].

R27 C16 smooth[7] the output from the peak detector. U8 converts this smoothed output into digital levels. R39 R40 adjust the output voltage to be compatible with the PIC input. PIC input threshold range is 0.8V to 0.25Vdd+0.8V (nom 2.05V), while the MIC6211 output voltage range is 1.2 to 3.8 V.

Q12 Q13 together with surrounding components provide a crude, fast acting ACG. This is required mainly to accommodate active tags at X6 when close to the reading head. The AGC circuit causes a R34 to be switch in parallel with the Rx coil greatly reducing the signal and damping ringing-on, which may otherwise swamp the receiver. The AGC is activated when the negative-going peak output from MAX278 reaches within one Vbe voltage of the ground i.e. the amplitude will be approx 3.7 Vpp.

EMC measures

The PR500 was rather close to the limits on radiated emissions. Several changes have been made in the HD500-2 to reduce the emissions. As these were all made at once it is not known which are the most effective. The PCB has been laid out in such a way as to isolate the digital sections from analogue and IO. R62 and R63 isolate the digital section from the rest.

The power conductors may be connected through L5 L6, but these are linked out. These are 0805 size in case it proved necessary to fit inductors. SM inductors are more readily available in 0805.

Most connections on the PIC chips have series resistors fitted, particularly where the tracks are of any length. These resistors are fitted close to the PIC chips. These are intended to prevent HF transients as the PIC chips are reputed to be noisy. In some cases the resistors are fitted only for this reason, e.g. R64 R65 R66

The 264 kHz clock from U7 has been slugged with R44 C3 R67. Testing showed these measues to be unecessary, and so to avoid possible problems C3 is not fitted and R44 is zero ohms.

[6] It is worth reviewing the choice of all Op Amps used in this circuit. It is entirely possible that suitable amps are now available at lower cost than the ones in use, which are as used on the 5291.
[7] Different values from 5291, in order to speed up for x6 operation.

Working Range

Expect ranges as shown.

Typical[8]

tag \ reader	HD	SP	PM	PM (free space)
928 active card	23 cm	28 cm	13 cm	22
968 passive card	8 cm	9 cm	3.5	7
931 passive keyring	4.5	5.5	3 cm	4.5

Minimum[9]

tag \ reader	HD	SP	PM	PM (free space)
928 active card	20 cm	25 cm	11 cm	20
968 passive card	7 cm	8 cm	3.0	6
931 passive keyring	4.0	5.0	2.5 cm	4

HD500-2

NB when testing the "forward" and "backwards" ranges are very dissimilar when the frame is fitted.

SP500
Expect the working range of a 928 tag to be 28 cm.
The transmit field of the SP500 will be higher than the HD500-2 as the screening effect of the metal frame is absent.

PM500
Expect a working range of a 928 tag to be 13 cm. (When mounted behind the steel "window")
There is a receive null virtually on the axis. With active tags this is not noticable. With the 931 keyring it is possible to place the tag in the null position. Provided the tag is not placed in the null location expect the working range to be 2.5 to 3 cm. While this is not a great range it has been judged adequate.

Inputs/Outputs

All inputs and outputs are protected against transient voltages by 5V devices. If these are connected to voltages more than 6V they may permanently fail short-circuit, thus rendering the reader inoperative.

<u>All inputs = Hold, Horn, R, R/G</u>

The operating voltage of all inputs the determined by the comparator voltage set in the PIC (U11). This will be set to 2.5V +- 100 mV.[10]

All inputs have a 10k pull-up to 5V[11].

[8] Based on early production samples
[9] Estimated. Includes worst case tuning and worst case 928. Estimate of 968 and 931 to be confirmed.
[10] Comparator resolution is 200 mV. Accuracy is better than 100 mV. The nominal value of 2.5 V may change by +- 100 mV in the final version.
[11] SIA spec required 1k pull-ups, but this is incompatible with BClink driver (which can have 300R on output) when two PR500s connected. Also there is a theoretical current consumption problem when input pulled to ground permanently. All inputs are slow-moving for Weigand, and so 10k pull up is unlikely to cause a problem.

Hold (C)

Data hold. Also BClink Rx input, which is now called "C".

Horn (Addr)
External horn control or address input for BC link.
For BC link this will be connected to DA to select one address or left open otherwise. DA will be briefly set to low during the power up or reset sequence in order to read the setting.

R
Red led control

R/G
Single wire LED toggle control, or Green led control

DA, D1 outputs
These are simple open-drain drivers, with 10k pull-ups..

The use of FETs vs direct drive from the PIC gives an improved ground-noise margin compared to bipolar, which will be particularly useful in instances where the control equipment connected has a low input threshold voltage, and long wires are in use. Direct connection to the PIC would also make the unit more susceptible to transient voltage damage.

D0 (D) output
Weigand D0 or BClink Tx out, which is now known as (D).

There are at least three variants of BClink input circuit. The line may also be connected to another BClink reader in parallel where output contention may occur. In order to accommodate all combinations it has been necessary to provide a 'real' tristate output. A single PIC output cannot deal with the contention current, and so the output has been buffered by Q2 Q5. If the PIC output is high impedance then the resistor network R58, R59, R60, R61 is arranged such that both transistors are turned off, as the bases are 0.44 V from the respective rail.

When driving Weigand 5mA can be sunk whilst ensuring the transistor stays in saturation[12] as the base current is 0.5 mA.

[12] This is possibly heavy handed, but harmless.

Microcontroller configuration

The reader is controlled by two of Microchip's PIC microcontrollers, one to control the tag reading process (U9) and the other to control the resulting I/O actions / processes (U11). The two communicate with each other using a custom-made two-wire communications protocol. Memory and processor constraints mean the protocol is limited in its capability. This protocol is called PIC2COMMS. In order to understand the protocol refer to the coded together with ES00626 PIC2 timing.gif.

The clock for U11 originates from the 7.392MHz crystal. The clock signal seen at OSC2 is fed to half of U7 which divides this by 2 to give 3.969 MHz, and being less than 4 MHz can be used as a clock for U9.

Each device has an 8 bit timer / counter (TMR0) available.

U11 (a.k.a Host PIC)(PIC16C622 or PIC16F87)

Memory – 2K x 14 of program memory (ROM) resides between locations 0000h – 07FFh with the Reset Vector at 0000h and the Interrupt Vector at 0004h. In the PIC16F87 another 2K x 14 resides between locations 0800h - 0FFFh.
Data memory (RAM) is organised into banks, two banks (Bank0 and Bank1) in the PIC16C622, four banks (Bank0, Bank1, Bank2 and Bank3) in the PIC16F87. Each bank contains General Purpose and the Special Function Registers. Bank0 resides from 00h to 7Fh, Bank1 from 80h to FFh, Bank2 from 100h to 17Fh and Bank3 from 180h to 1FFh. The Special Function Registers are located on the first 32 locations of Bank0 and Bank1, and on the first 16 locations of Bank2 and Bank3. The General Purpose Registers reside in locations 20h to 7Fh (Bank0) and A0h to BFh (Bank1) in the PIC16C622; and in locations 20h to 7Fh (Bank0), A0h to EFh (Bank1), 110h to 16Fh (Bank2) and 190h to 1EFh (Bank3) in the PIC16F87.

Inputs –
RA0 = Hold (C)
RA1 = Horn (Addr)
RA2 = R (a.k.a Red Input)
RA3 = R / /G (a.k.a Red /Green Input or Single Wire Control)
RA4 = /ACK / Command (Acknowledge Command from the reader processor)

Outputs –
RB0 = /REQ / DATA (Request Data to the reader processor)
RB1 = D0 (D) (standard output when not transmitting BCLink commands)
RB2 = D1
RB3 = DA
RB4 = Drive signal to on-board Horn
RB5 = Drive signal to on-board Red Led
RB6 = Drive signal to on-board Amber Led
RB7 = Drive signal to on-board Green Led

Watchdog -
The Watchdog Timer (WDT) is internal and needs to be updated nominally every 18ms using

the 'CLRWDT' command. A separate pre-scaler is available and is used in the PIC16F87 to extend the update time to around 1sec. **Warning** this time is very temperature dependent and can be halved at very low temperatures. There are also internal Power-On-Reset and Brown-out Reset mechanisms.

Processor Configuration -
The following processor configuration details are set up when the PICstart programmer is enabled. The 'Configuration' word is written to directly when each device is programmed.

Oscillator = HS (High Speed crystal oscillator mode)
Watchdog Timer = On
Power Up Timer = On
Code Protect = Off
Brown Out Detect = On

For the PIC16F87 there are additionnal configuration bits which also have to be set.

CCP Pin Slection = RB3
Debug = Disabled
Write Protection = Off
EE Data Protect = Off
Low Voltage Programming = Off
Master Clear = External
Internal External Switchover = Disabled
Fail-safe Clock Monitor = Disabled

U9 (a.k.a Reader PIC) (PIC12CE519 or PIC12F629)

Memory – 1K x 14 of program memory (ROM) resides between locations 0000h – 03FFh with the Reset Vector at 0000h and the Interrupt Vector at 0004h.
Data memory (RAM) is organised into two banks, (Bank0 and Bank1). Each bank contains General Purpose Registers and the Special Function Registers. In the PIC12CE519 Bank0 resides from 00h to 1Fh and Bank1 from 20h to 3Fh, whilst in the PIC12F629 Bank0 resides from 00h to 7Fh and Bank1 from 80h to FFh. The Special Function Registers are located on the first 7 locations of Bank0 and Bank1 in the PIC12CE519 and the first 32 locations of each bank in the PIC12F629. The General Purpose Registers reside in locations 07h to 1Fh and 30h to 3Fh in the PIC12CE519; locations 20h to 5Fh and A0h to DFh in the PIC12F629. Also available are 16 bytes of EEPROM memory in the PIC12CE519 and 128 bytes in the PIC12F629. This is used to store the Distributor / Secondary Codes and Reader Configuration details.

Inputs Outputs –
GP0 = Input - Rx signal from receiver
GP1 = Output - Tx signal to transmitter
GP2 = Input - /REQ / DATA (Request Data from the host processor)
GP3 = Output - /ACK / Command (Acknowledge Command to the host processor)
OSC2/GP4 = N/C in crystal oscillator mode
OSC1/GP5 = 3.969MHz clock signal originated by 7.393MHz crystal

Watchdog -
The Watchdog Timer (WDT) is internal and needs to be updated every 12ms[13] using the 'CLRWDT' command.

Processor Configuration -
The following processor configuration details are set up when the PICstart programmer is enabled. The 'Configuration' byte is written to directly when each device is programmed.

Oscillator = HS (High Speed crystal oscillator mode)
Watchdog Timer = On
Power Up Timer = On
Code Protect = Off
Brown Out Detect = On
EE Data Protect = Off
Master Clear = Internal

[13] This used to state 18 ms but note the WDT is temperature sensitive, and requires 12 ms at -30°C

2. Test Equipment

Description of Test Process

Prior to use the PCB's shall have been 'bare board tested'. This shall confirm that all tracking is correct and no short circuits exist.

Prior to reaching test the Unit Under Test (UUT) shall been passed by the Manufacturing Defect Analysis (MDA) system. This shall confirm that all components are correctly fitted and solder bridges etc have not been incurred during the manufacturing process.

Special Test Equipment

The testing of HD500-2 Readers shall be carried out using the HD500-2 Test Jig (ES00628). This along with a selection of tags and the readers manufacturing test routine, shall enable the testing of the UUT. Presentation of the 'special' manufacturing test tag (coded with 0E00000000000000h) to the reader within the first 4 seconds of power being applied shall initiate the manufacturing test routine.

The test procedure is an appendix to this document.

3. Minimum test Requirements[14]

Prepot

Current consumption

Conditions: Red on, Green on, Horn on, Scanning (no tag). 35V DC input
60 mA max. (i.e. averaged over time).
Test kit will illuminate a warning LED at between 70 and 80 mA. At 90 to 100 mA the unit will not operate.

Operating voltage

The 5V and 15V supplies will be checked.
Present test kit does not do this. If the 5V regulator is faulty, we may expect this to show up in other tests. If the 15V reg is faulty (or wrong part fitted), we may suffer from premature thermal shutdown.

Tx field strength

The test kit checks the Tx field by virtue of a carefully positioned passive tag.

Rx min and max reception at x1 and x6

Present test kit used a carefully positioned passive tag to check min Rx performance.
X6 operation and saturation checks are not carried out.

LEDs and sounder operation

Check each of the LEDs and Sounder operates with sufficient intensity.

Inputs operating threshold

External LEDs, horn and Hold control are required to operate at a nominal 2.5 V.

D1 DA outputs

Check that each output can achieve a logic high or low.

Tristate output D0

Check the output drive into a 47 ohm load to the opposite rail.[15]
Check that in high impedance output mode not more than 10 uA[16] can be drawn in either high or low.

Memory retention

Check that the unit remembers it's configuration etc.
This test is not carried out on prepot. It is checked post pot by virtue of the read test immediately after power-up.[17]

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[14] The present test kit lacks some features as identified below, and so does not test to the minimum requirements. We have taken the view that the associated risk of product failure is low, and so will proceed to use this. The minimum requirement remain 'for the record' and potential risks identified.
[15] This checks that both transistors are properly fitted and the output resistor is the right value. ATE tests may make this much detail unnecessary. In fact the test kit in effect checks for drive "close to" the rail.
[16] 10 uA is a random choice. Test kit will indicate at about 1 mA and so this test is not really carried out, but again low risk on the basis of ATE tests.
[17] There is a theoretical risk that faulty ICs will be received. If this become an issue a prepot test will need to be introduced.

Visual check of heatsink

Check that the heatsink wires are present and properly formed.

Post pot test

(To ensure nothing damaged during the process).

Tx

Rx

LEDs and sounder operation

Inputs operation

Output operation

Configuration

Configure as required for the model type. Ensure matching model label affixed.

TS00185-appendix_1 Test Procedure for HD500-2 SP500 PM500

HD500-2 may also mean SP500 or PM500

The test jig includes an HD "frame" with a tag mounted at a fixed distance. This "range-frame" is used only with the HD range test.
SP and PM each have their own adaptor plate with a range test tag mounted on a platform. The tag is turned off (shorted) with a push button so as to avoid interfering during the I/O test and configuration.

Using test jig ES00628

The test jig should be supplied with 34 to 35 V DC regulated

Prepot

1. Check power switch is off. Fit the HD500-2 to the jig
2. Turn on the power and configure as "HD500-2 regular". The unit will respond to each tag.
3. Press the range test button (SP/PM). The horn will sound and the DA LED will flash (HD - position "range-frame")
4. Check the current is less than 70 mA. The overcurrent LED may light at higher currents.
(4A - HD remove "range-frame")
5. Cycle the power and offer the OE test tag. The unit will respond.
6. Check all LEDs and the sounder are off.
7. Press each of the eight buttons in turn while checking the respective LEDs or sounder.
(Note only one LED or sounder should operate)

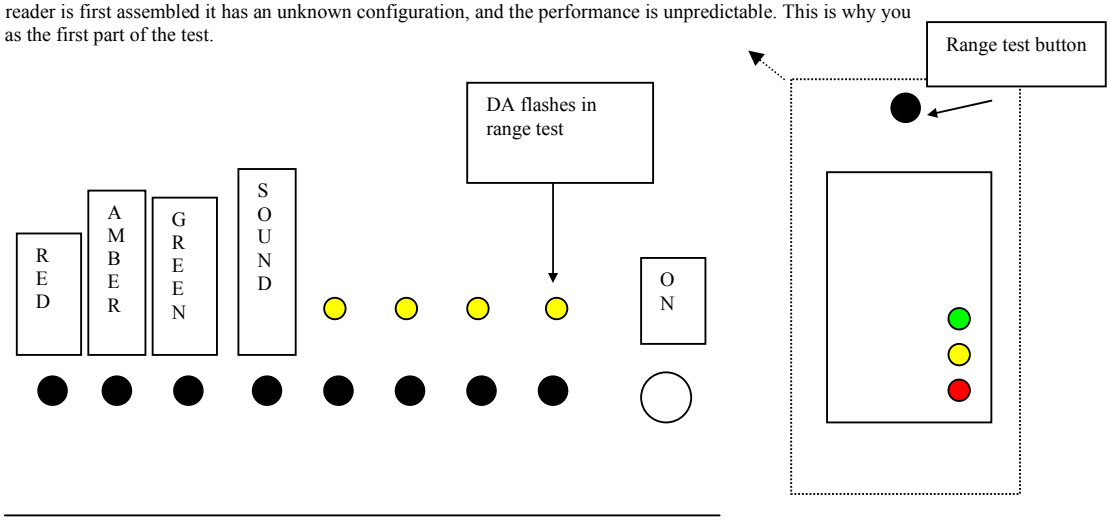
Post pot

1. Check the power switch is off. Fit the HD500-2 to the jig.
2. Turn on the power. Press the range test button. The horn will sound and the DA LED will flash. (HD - position "range-frame")
(2A - HD remove "range-frame")
3. Cycle the power and offer the OE test tag. The unit will respond.
4. Check all LEDs and sounder is off
5. Press each of the eight buttons in turn while checking the respective LEDs or sounder.
6. Cycle the power and configure the reader to the required format.
7. Affix appropriate configured label

Configuring

In order to configure the reader two tags must be offered in the right order and within a few seconds of power on.
NB - When configuring ensure the config tag matches the shape (HD SP PM PR) other wise the wrong "product" will be reported to the system.
We are using passive keyring tags as they have relatively short range and reduce the risk of inadvertently reading the wrong tag.
Keep the workspace clear of other tags for this reason.
As each tag is read the amber LED will light and the sounder will bleep.
If there is a problem with either read then repeat the whole process.

When the reader is first assembled it has an unknown configuration, and the performance is unpredictable. This is why you configure as the first part of the test.



DoLo D0Hi D1 DA

Procedure for calibrating ES00628

Range test

The **SP/PM** range test uses a 931 tag. This has been chosen as its short range and low output levels means that it can be fixed at a convenient point on the test jig. Also there is no battery to maintain. The tag does not require calibration.

The 931 tag is held off by the push button, which shorts out the coil until the button is pressed.

Calibration is carried out by adjusting the tag position and height.

The tag is fixed with the coil near the axis SP/PM500 Tx coils.

Select a "good" SP/PM500, which is known to meet the range performance specifications[18].

Mount this reader into the test jig.

Connect a scope probe to the tag coil, with a 1 M ohm resistor in series withe the scope probe so as so prevent detuning the tag. Connect another probe to the output of the MAX274 (pin 19). Hold in the button (or disconnect it).

Adjust the tag position so that the tag is just reading. Then adjust the position so that the tag signal and the output of the MAX274 are increased by 50 %. The tag signal will be approx. .[19] 1Vpp and the MAX274 output will be approx. 1.3 V pp. Beware of mounting the tag close to a null position, particularly on Rx, as a tiny shift of tag position can lead to large changes of output level. Check against this by shifting the tag 1 mm or so in each direction from the chosen position.

It is easier to find a good location if the height is first adjusted so that the Tx field is at or slightly above the required level over a large area. Conversly if the tag is too close to the reader is will be difficult, if not impossible to find a sutable location, and the Tx Rx levels are likely to be very position sensitive.

The **HD** uses a 968 tag. A 931 was found to be unsuitable as, when the frame is fitted, there tends to be a Rx null in the (otherwise) right spot for locating the tag. The 968 does not have the same problem. Calibration requires using a known good reader, in a frame. The tag height is adjusted to find the max read height, and then reduced by 1 cm[20]. As it happens the Rx level in this configuration is approx 2Vpp, which although perhaps a little high, is acceptable.

[18] PM should be checked both with and without metal case.
[19] Depends on probe capacitance vs "temporary" 1Mohm resistor. If this procedure or equivalent is not used, then when the scope is removed, the tag signal will probably increase.
[20] For the record - pillar height 7 cm on jig at first issue.