Circuit Description

Of

MP252WDNB

Integrated Access Device

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Revision History

Revision	Date	Changed by	Description
0	Mar 15,2011	D. Li	1st Release
1	June 29,2011	Zi Qun Yeung	Revise block diagram and description

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1 Introduction

Integrated Access Device (IAD) is an internet connectivity product. MP252-WDNB is a residential IAD product branded by AudioCodes , it is targeting to be sold to service providers world-wide.

MP252-WDNB is developed among Danube , the Lantiq SoC generation for ADSL2/2+ IAD/Gateway solution with integrated Voice Over IP technology , which is based on MIPS24KEc Network Processor and integrates embedded VoIP Engine , ADSL2+PHY and Protocol Processing Engine.

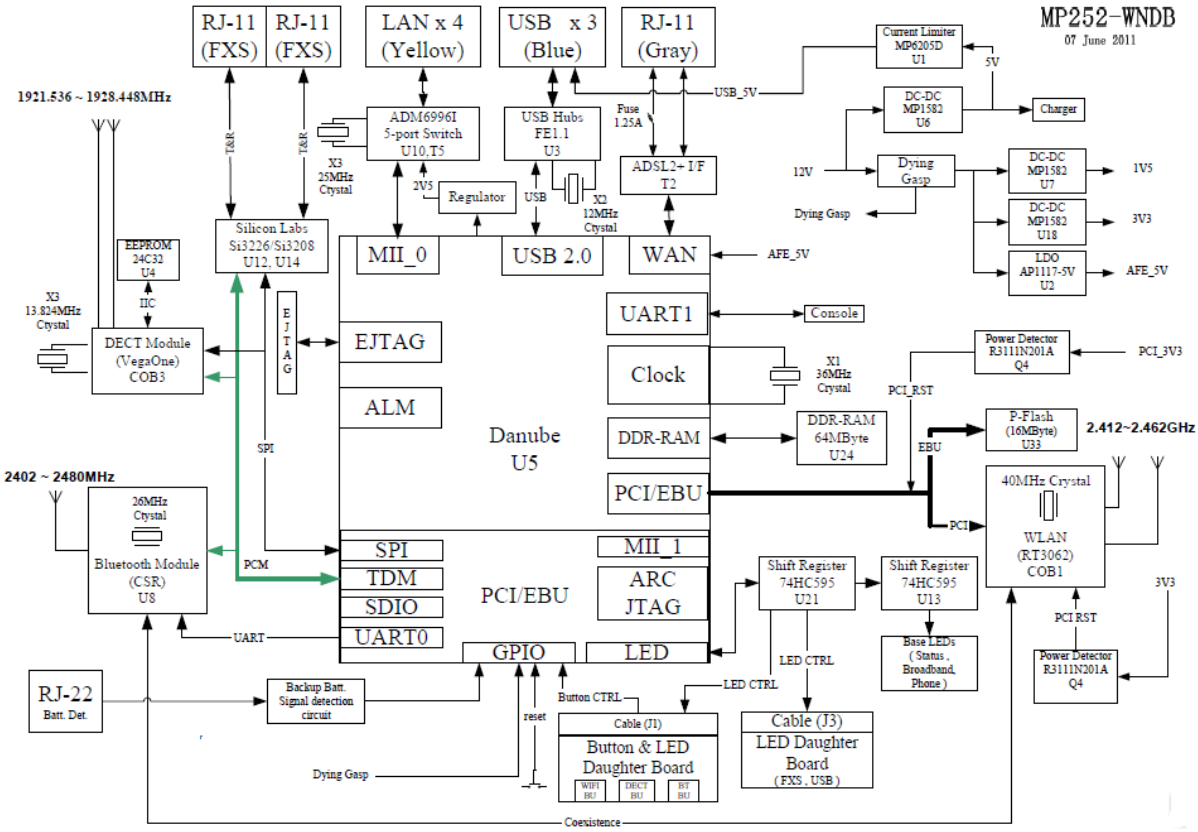
The product uses Danube as host to be associated with Ethernet Switch Controller, Dual ProSlic chipset and WLAN, DECT,Bluetooth to support below features:

- ADSL Interface
- WAN Interface
- 10/100 Ethernet LAN Interface
- WIFI
- DECT
- Bluetooth (No support)
- USB 2.0 host and device function through USB Interface
- FXS Interface

2 Block Diagram & Functional Description Of Base Main

2.1 Main board

2.1.1 Functional Block Schematics



2.1.2 Circuit Description

MP252WDNB consists of a main board, separated COBs for WIFI/DECT/Bluetooth modules , front LED and button daughter board , 12 LEDs indicators totally are used on front and rear of the unit to indicate each operating status , which are Status , Broadband , Phone , FXS1 & 2 , USB, ADSL, WIFI,.DECT and Bluetooth. Three front buttons are also used for WIFI, DECT and Bluetooth .

PSB50702 (U5) is one of the single chip belongs to Danube product family.

The main board consists of Danube of ADSL2 IAD/Gateway SoC , ADM6996I of Ethernet Switch Controller , Si3226/Si3208 of Dual ProSLIC , shift register for LED control (74HC595), WIFI module (RT3062),DECT module (PNX8019) with EEPROM , Bluetooth module (CSR-BC4), Crystals , NOR Flash , DDR-SDRAM and Power Management Units .

Two daughter boards are used for MP252 base . One is LED board which connect the LED from base to rear cabinet for the ports of FXS and USB . The rest daughter is a LED/button board which connect the LED and button from base to front cabinet .

2.1.2.1 MCU and Memory

Danube which is packed in PG-LBGA-256, acts as the system host of the product, it operates by using crystal X1 , a single 36MHz crystal oscillator .

16 megabytes of NOR flash (MX29GL128ET21-90Q) is used as firmware storage associate with Danube through PCI bus, which access time is 90nS.

64 megabytes of DDR-SDRAM (A3S12D304DETP) is operated under 266MHz clock.

2.1.2.2 Ethernet Switch Controller

The Ethernet Switch Controller of ADM6996I operates by using Crystal X3 , a single 25MHz crystal oscillator, which supports 10M/100M auto-detect Half/Full duplex switch ports.

2.1.2.3 USB

The Danube USB sub system provides USB2.0 high speed / full speed host controller function as well as USB2.0 high speed / full speed device function. U6 (MP1582) is a monolithic step-down switch mode converter which switching frequency is at 1.4MHz , it would convert the input voltage of 12V to 5V as the power supply of USB port.
U1 (MP6205D) is a power distributer which is of a current limiter to limit the max. current draw by external USB device at 1A .
U3 (FE1.1) is an USB hubs controller , which is used to handle the data traffic for three USB ports . It operates by X2, the 12MHz crystal oscillator .

2.1.2.4 ADSL circuit

Danube (U5) is a single chip solution which integrates an ADSL2/2+ transceiver including AFE and LD . The external circuit for ADSL on MP252 application just involves an ADSL transformer (T2) , a common mode choke (T1) and a lightning surge suppressor (D41) mainly . T2 is used as impedance matching and isolation for MP252 device to PSTN line of outside . T1 is a CMC which used to reject the common mode noise from PSTN line to ensure the ADSL signal quality . D41 is used to absorb the lightning surge from the PSTN line to protect the device of MP252 .

2.1.2.5 Backup battery circuit

This circuit is composed of three inverter circuits which is mainly used to limit the signal logic level from RJ22 (J2) at 3V3 in max. to protect the host of MP252. The signal at J2 is from an external power adapter with backup battery as option , the signal is used to allow MP252 host to aware of the situation of the adapter to work in a right mode .

2.1.2.6 Shift register for LED control.

As the GPIO of Danube (U5) is not enough to handle so many control pin for functional circuit and LEDs , two pieces of 74HC595 , the shift register device are used on MP252 application to extend the GPIO quantity to provide enough control pin for the application .

2.1.2.7 FXS

The Dual ProSLIC of Si3226/3208 each consist of a low-voltage CMOS device integrating both SLIC and CODEC functionality in combination with a high voltage linefeed IC (LFIC) . It operates from a single 3.3V supply and interface to standard PCM/SPI. A built-in DC-DC controller automatically generates the optimal battery voltage required for each line-state, the PCM clock is operated up to 8.192MHz .

2.1.2.8 Power Management Unit

The product is powered by an external 220VAC to 12VDC switching mode adapter . There are two monolithic step-down switch mode converters (U7 , U18) which switching frequency is at 1.4MHz provide 1.5V and 3.3V for operation of Danube , Memories , WIFI and other circuitries .

The 2.5V of DDR-SDRAM supply is provided by the regulator which is adjusted by Danube .

LDO of AP117-5V (U2), is used to provide 5V for AFE (analog front end) of Danube for ADSL application .

MP252 is of Dying Gasp circuit for ADSL . Dying Gasp circuit is used to ensure the Danube could detect the power failure message several second before the system is shut down . It is a requirement of ADSL Telco.

The charger circuit consists of to resistors connected in parallel as current limiter , which is used for handset battery charging .

2.1.2.9 Button & LED Daughter board

The button & LED daughter board consists of three buttons and three dual-color LEDs which are used for WIFI , DECT and BT on/off switch and indication .

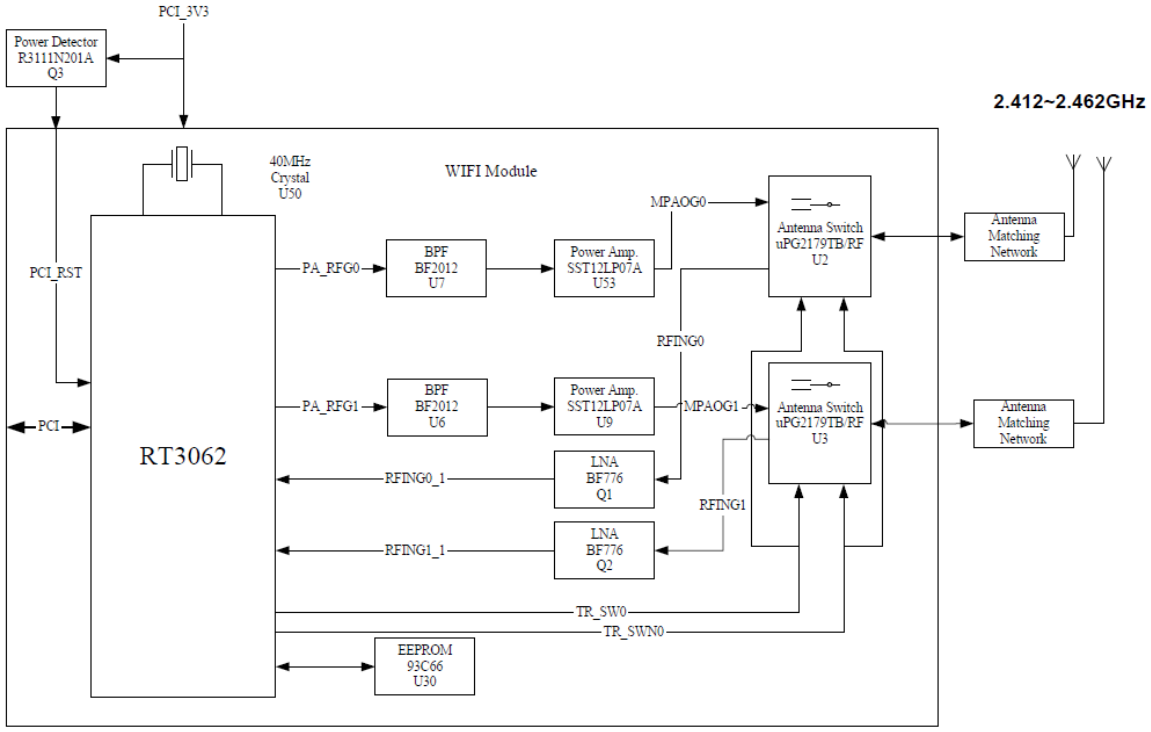
To ensure the contact of button works well , the design on MP252WDNB button & LED board is using two pads in parallel for each button .

2.1.2.10 LED Daughter Board

The LED daughter board consists of four LEDs for the indication of two FXS ports and USB ports respectively .

2.2 WIFI Module

2.2.1 Block diagram



2.2.2 Circuit description

The WIFI module consists of a processor (RT3062) which is a highly integrated MAC/BBP and 2.4RF single chip with up to 300Mbps PHY rate supporting , a PA , a LNA and an antenna switch device are used to support the module operates in 802.11b/g/n mode respectively .

MP252WDNB WIFI could fully complied with IEEE802.11b supports transmission rates ranging up to 11Mbps via direct-sequence spread spectrum (DSSS) modulation schemes at 2.4GHz .

MP252WDNB WIFI could fully complied with IEEE 802.11g supports transmission rates ranging up to 54Mbps via Orthogonal Frequency Division Multiplexing (OFDM) modulation schemes at 2.4GHz.

MP252WDNB WIFI could fully complied with IEEE 802.11n which supports transmission rates ranging up to 300Mbps @40MHz BW and 150Mbps@20MHz BW via Orthogonal Frequency Division Multiplexing (OFDM) modulation schemes at 2.4GHz. The IEEE 802.11n could operate in 1T1R and 2T2R mode (MIMO) which is relied on the client configuration .

- When the WIFI works in 2T2R mode , two antennas will be activated at the same time and operated according to the MIMO algorithm .
- When the WIFI works in 1T1R mode , the WIFI will select either Antenna 0 or Antenna 1 according to the detected signal strength .

2.2.2.1 BPF

MP252WDNB WIFI module is using the BPF of BF2012 (U6 , U7) to filter out the spurious for TX path .

2.2.2.2 Power amplifier

PA of SST12LP07A (U9, U53) is used as RF power amplifier to provide the desired WIFI TX power according to the standard so as to achieve the desired range .

2.2.2.3 Lower noise amplifier

LNA of BF776 (Q1 , Q2) is used to amplify WIFI RX signal to achieve the desired RX sensitivity so as to achieve the desired range .

2.2.2.4 EEPROM and Crystal

The crystal oscillator of 40MHz (U50) is used to provide the reference clock for RT3062. The 4Kbit serial EEPROM (U30) is used to save the relevant information including tunable parameter , MAC address and etc. to support the operation of RT3062.

2.2.2.5 Power detector

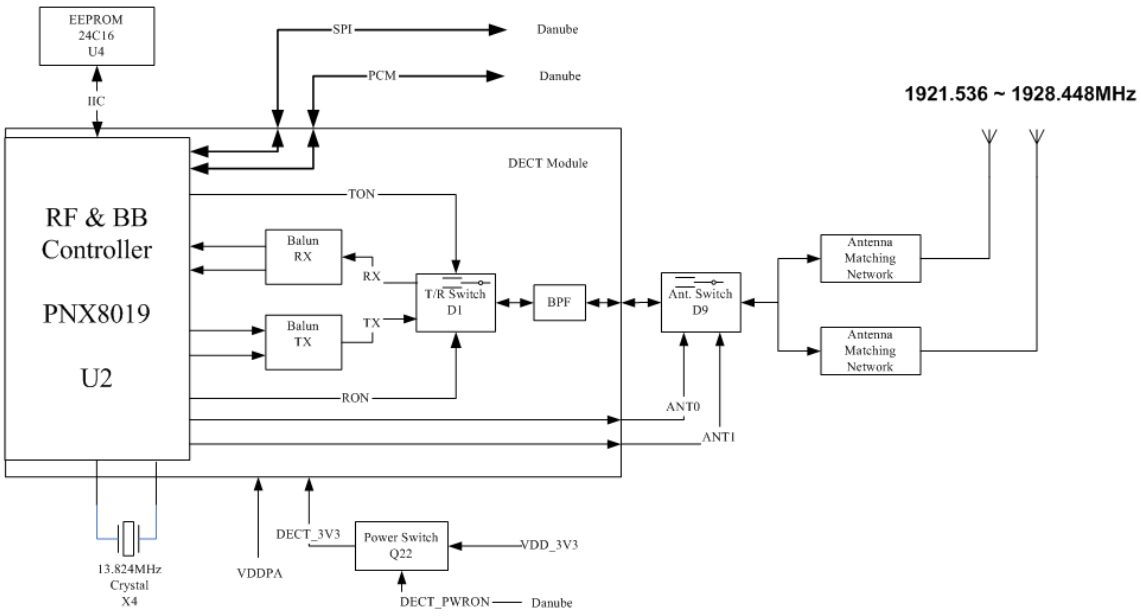
As WIFI interface is sharing the same PCI bus as NOR flash memory device , to prevent the PCI bus from being conflicted in timing between the devices each other , a voltage detector is used to slippage the wake up of WIFI module during powering up .

2.2.2.6 Antenna

MP252WDNB use two IFA antennas for WIFI. Antenna 0 will be fixed as active while the WIFI works in both 802.11b and 802.11g mode . Two antennas will be actived at the same time to support MIMO while it works in 802.11n mode .

2.3 DECT Module

2.3.1 Block diagram



2.3.2 Circuit description

The DECT module consists of DSPG PNX8019 , the integrated RF & Baseband controller, two Balun circuits and a T/R switch on TX and RX RF path and BPF. There is a EEPROM (U4), 13.824MHz crystal oscillator (X4) , antenna switch , antenna matching network and a power switch (Q22) are developed on base to support the operation of DECT module on the design of MP252WDNB . The communication between Danube and DECT is via SPI and PCM , SPI is used for control while the PCM is for signal .

The DECT standard is based on Multi-Carrier TDMA-TDD access , which modulation used is Gaussian Frequency Shift Keying (GFSK) with a bandwidth-bit period product of 0.5 .

2.3.2.1 DSPG PNX8019

DSPG PNX8019 , the integrated RF & Baseband Controller , which is composed of an ARM968E-S microprocessor , SRAM for the micro controller . the micro controller program a 4-channel hardware ADPCM , interface circuit , Audio CODEC , auxiliary A/D , D/A conversion and RF modem . This results in a one-chip implementation of the complete feature cordless terminal .

2.3.2.2 Balun circuit

There are two Balun circuitries are used at TX and RX RF path of DECT module to convert the RF signal from single to differential mode for RX and differential to single mode for TX .

2.3.2.3 T/R switch

The T/R switch (D1) is used to switch the signal path of TX and RX according to the frame of DECT standard for the BMP of PNX8019.

2.3.2.4 BPF

The BPF is composed of discrete components on the design of MP252WDNB , which is used to filter out the outband spurious to ensure the TX and RX signal quality .

2.3.2.5 EEPROM

MP252WDNB is using a 24C32 EEPROM chip to store the tunable parameters relevant information for DECT module to support its operation .

2.3.2.6 Crystal Oscillator

Crystal oscillator of 13.824MHz is used on the design of MP252WDNB to provide the reference clock for PNX8019.

2.3.2.7 Antenna Switch

Antenna switch of D9 is used to provide the diversity antenna topology for DECT on MP252WDNB. The Antenna switch will be operated according to the signal strength detected in each frame of DECT standard to judge which antenna need to be selected for the application .

2.3.2.8 Antenna match network

The antenna matching network is used to have the antenna worked in high efficiency situation .

2.3.2.9 Power switch

The power switch (Q22) is used to allow Danube to do reset operation whenever the system need and control the power up sequence for DECT module .

2.3.2.10 Antenna

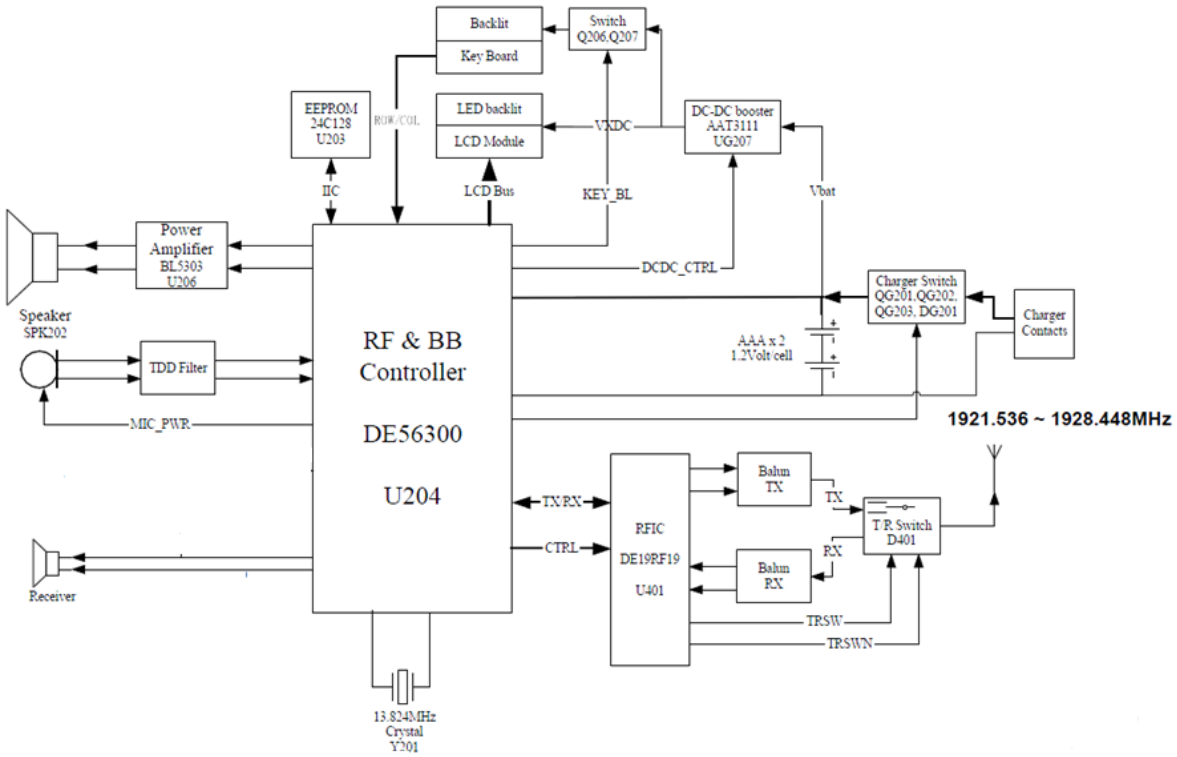
MP252WDNB uses two IFA antennas as diversity for DECT .

2.4 Bluetooth Module

No support .

3 Block Diagram & Functional Description Of Handset

3.1 Block Diagram Of Handset



3.2 Circuit Description

MP252WDNB is of a DECT 6.0 handset which consists of RF&BB Controller (U204) of DE56300 , RFIC (U401) of DE19RF19, EEPROM (U203) , power amplifier (U206) , battery charge circuit , speaker , receiver , transducter , key board , LCD module , Balun for TX , T/R switch and single DECT antenna .

3.2.1 RF& BB Controller

The DE56300 (U204) is a highly integrated, mixed-signal, TeakLite™ based chip for telephony and multimedia applications. It contains two types of advanced Burst Mode Controller (BMC) modems for DECT (Digital Enhanced Cordless Telephone standard) and EDCT (DSPG proprietary digital cordless standard) to provide frequency-hopping spread-spectrum multi-handset cordless communication.

3.2.2 RFIC

The DE19RF19 RFIC is a transceiver for DECT standard application operating in North American frequency ranges allocated for DECT , which is used in conjunction with DE56300 , the RF&BB controller which including the DECT BMC .

3.2.3 EEPROM

MP252WDNB handset uses a 128Mbit EEPROM (U203) , which is used to save the tunable parameters to support DECT working , it is also used to save the data to support the feature of handset such as ringer tones , phone book , CID and redial record.

3.2.4 Power amplifier

The power amplifier (U206) is used to drive the speaker which support the handsfree feature of handset .

3.2.5 LCD module

MP252WDNB handset uses a color LCD module which supports the display of handset for the feature and operation .

3.2.6 DC-DC boost

The DC-DC boost (UG207) is used to boost up the voltage from 2.2V to 3.7V to support the backlit of LCD module and key pad .

3.2.7 Key board

Key board used by MP252WDNB is to support the feature of handset dial-out and display edit . It is of 22 keys which is defined as numeric and function key respectively .

3.2.8 Speaker , receiver and transductor

The speaker , receiver and transductor used by MP252WDNB handset is for talking and hearing . Speaker is used to support the feature of handsfree , receiver is used to support earpiece , transductor is used for speech sending in both earpiece and handsfree modes .

3.2.9 TX Balun

The TX balun circuit is used to convert the TX RF signal from differential to single end operation .

3.2.10 T/R switch

The T/R switch (D401) is used to switch the antenna for TX and RX according to the frame of DECT standard .

3.2.11 Switch circuit

The backlit switch circuit (Q206, Q207) is used to control the backlit on/off for key pad , it is controlled by DE56300 according to the operation .

3.2.12 Charge switch

The charge switch consists of QG201 ~ 203 , DG201 is used to determine the battery charge current , which is controlled by DE56300 according to the charging algorithm .

3.2.13 Crystal oscillator

The crystal oscillator of 13.824MHz (Y201) provides the reference clock for DE56300.

4 WIFI Radio

It is described in separated document.

5 DECT Radio

It is described in separated document .

6 Bluetooth Radio

Not support.

END

RF Module
(2.4GHz WIFI)

Theory of Operation

Model: MP252WDNB
Base unit

Revision History

Revision	Date	Changed by	Description
1.0	5MAY, 2011	JIMMY WONG	1st Release
1.1	23May, 2011	JIMMY WONG	2nd Release
1.2	22JUN,2011	JIMMY WONG	3rd Release

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Definitions

LNA	Low Noise Amplifier
PA	Power Amplifier
PLL	Phase Locked Loop
RX	Receive(r)
TX	Transmit(er)
UPCS	Unlicensed Personal Communications Services
VCO	Voltage Controlled Oscillator
AP	Access Point
TR	Transmit and receive

Introduction

The purpose of this document is to describe both the 2.4 GHz WIFI RF module operation in MP252_WDNB base unit It also describes the interface between the baseband and RF circuits.

WIFI RF Module Description

The radio module is used for the 2.4 GHz systems for MP252_WDNB base unit. It uses a highly integrated single chip solution RT3062 from Ralink. This RFIC includes the RF transceiver, PA, filter, LNA and TR switch. Figure 1 shows RFIC block diagram.

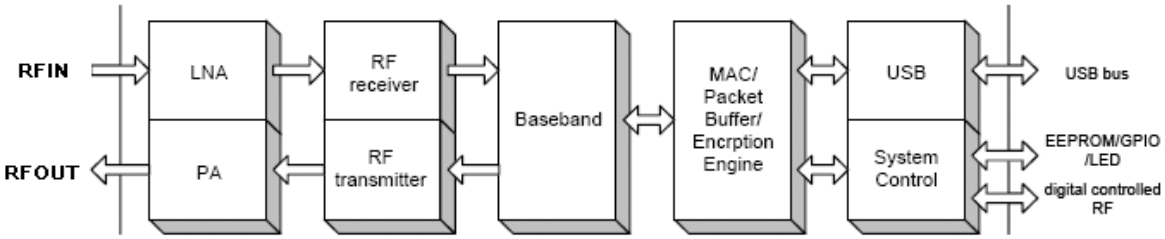

Figure1 RFIC (RT3062) Block Diagram

There is only one VCO in the RFIC. This VCO operates during both transmit and receive slots and Figure 2 below displays the RF block diagram of the RT3062.

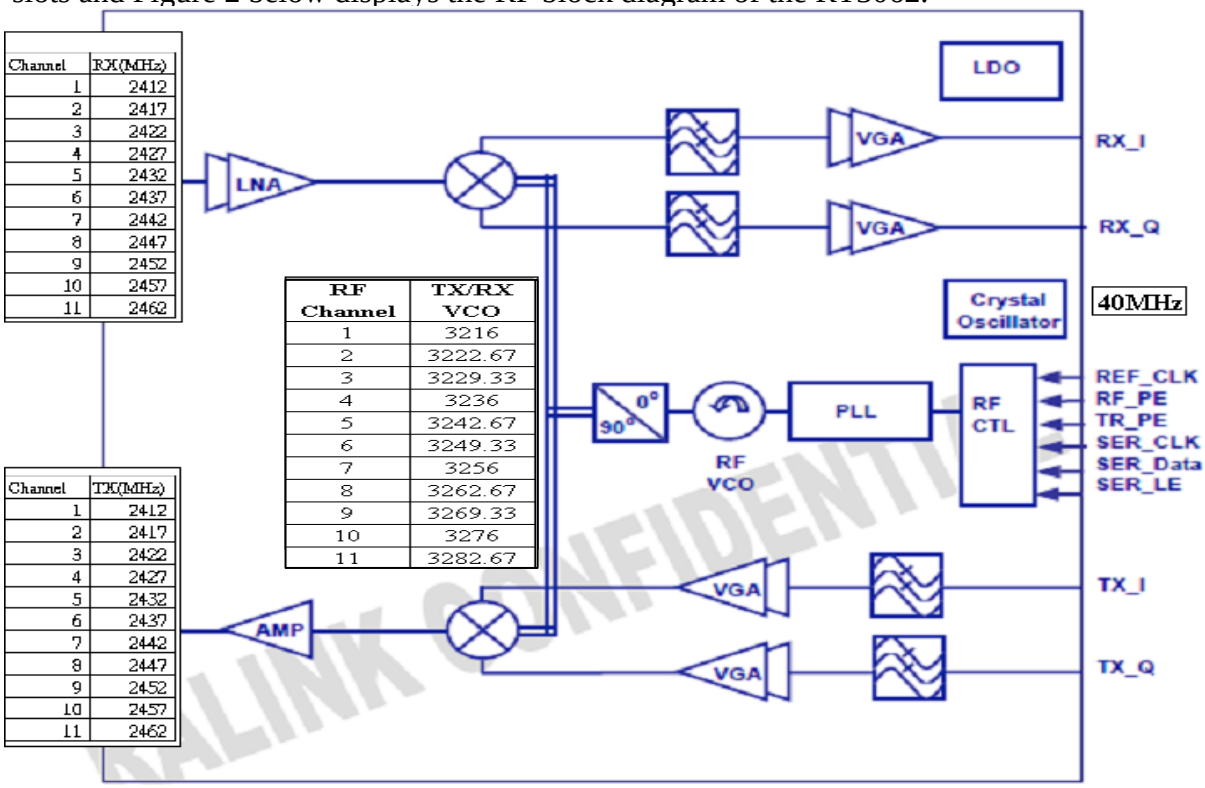

Figure 2 RFIC (RT3062) RF Block Diagram

3.1 VCO/PLL/IF Section

The PLL is synthesized with baseband crystal (40MHz). The signal outputed from the PLL entering the VCO which operates at 3.216 ~ 3.282GHz. Then, the VCO is divided by ¾ to become the LO. The LO operates at 2412~2462MHz. The LO mix with the IF to become RF. In RT3062, the IF is zero. Therefore, the TX and RX RF is also operating at 2412~2462MHz.

3.2 TX Chain

The 2.4GHz signal is amplified through a pre-amplifier inside the chipset. There is a T/R switch inside the chip. When the TX path is switched on, the signal comes out from the driver and goes through a external balun. Then the signal goes through a band pass filter to remove higher harmonic and VCO spurious contents. The output of the bandpass filter is routed to the antenna. The signal will pass to a permanently soldered antenna.

3.3 RX Chain

In RX mode, the front end circuitry is sharing with the TX Chain. The antenna is connected to the same bandpass filter. Then, the output of the bandpass filter is connected to the RFIC-RT3062. The internal T/R switch will set to Rx path during Rx. In RT3062, the signal then enters into the LNA to reduce the noise and amplify the signal. The output of the LNA is connected to the input of the image reject mixer. The mixer's LO is set by the VCO. Zero IF is implemented in the system.

The output from the mixer is passed through an internal IF bandpass filter or the channel filter to further improve the channel selectivity. The output of this filter connects to a limiter stage. The limiter amplifies the signal and its output connects to the demodulator, which is in the digital block within the same chip. The demodulator FM demodulates the output signal to a baseband analog signal.

RF Module Specifications

Wifi RF Module

	Parameter	Min	Typ	Max	Units
1	RF Channel Spacing		5		MHz
2	Transmitter Frequency Offset (over temperature range) in G mode	-48		48	kHz
3	Wifi Antenna 0 Gain		2		dBi
4	Wifi Antenna 1 Gain		2		dBi
5	Receiver Sensitivity (BER=0.001)in G mode		-70		dBm

Channel Frequency Plan

For the US market, the 2.4GHz WiFi lowest channel frequency used is 2412 MHz and the highest channel frequency is 2462MHz.

Wifi RF Module

XTAL frequency	40 MHz				
Channel Spacing	5 MHz				
IF frequency	0 MHz				
	802.11b	802.11g	802.11n(20M)	802.11n(40M)	
No.of channel	11			7	
Max Bit Rate	11Mbps	54Mbps	150 Mbps	300 Mbps	
RF Channel	TX/RX VCO (MHz)		TX/RX LO (MHz)	TX/RX VCO (MHz)	TX/RX VCO (MHz)
1	3216.00		2412	NA	NA
2	3222.67		2417	NA	NA
3	3229.33		2422	3229.33	2422

4	3236.00	2427	3236.00	2427
5	3242.67	2432	3242.67	2432
6	3249.33	2437	3249.33	2437
7	3256.00	2442	3256.00	2442
8	3262.67	2447	3262.67	2447
9	3269.33	2452	3269.33	2452
10	3276.00	2457	NA	NA
11	3282.67	2462	NA	NA

RF Modules (1.9GHz DECT 6.0)

Theory of Operation

Model: MP252WDNB

Base Unit

Revision History

Revision	Date	Changed by	Description
1.0	23MAY, 2011	Jimmy Wong	1st Release

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1 Definitions

ATE	Automated Test Equipment
BS	Base Unit
BER	Bit Error Rate
FHSS	Frequency Hopping Spread Spectrum
FM	Frequency Modulation
GFSK	Gaussian Frequency Shift Key
LNA	Low Noise Amplifier
PLL	Phase Locked Loop
RX	Receive(r)
TDMA	Time Division Multiple Access
TX	Transmit(er)
UPCS	Unlicensed Personal Communications Services
VCO	Voltage Controlled Oscillator

2 Introduction

The purpose of this document is to describe the 1.9 GHz DECT 6.0 RF module operation in MP252_WDNB base unit. It also describes the interface between the baseband and RF circuits.

3 DECT 6.0 RF Module Description

The radio module is used for the 1.9 GHz system in BS. The baseband MCU and RF circuits (synthesizer, modulator, VCO and power amplifier) are highly integrated into a single chip called VegaOne manufactured by DSPG. This radio is a single down conversion system with an IF frequency of 864kHz. Since the radio is used in a TDMA system, only 1 VCO is required. This VCO operates during both transmit and receive time slots. Figure 1 below displays the RF block diagram of the integrated chip for both the fixed (i.e. Base) and portable parts (handset).

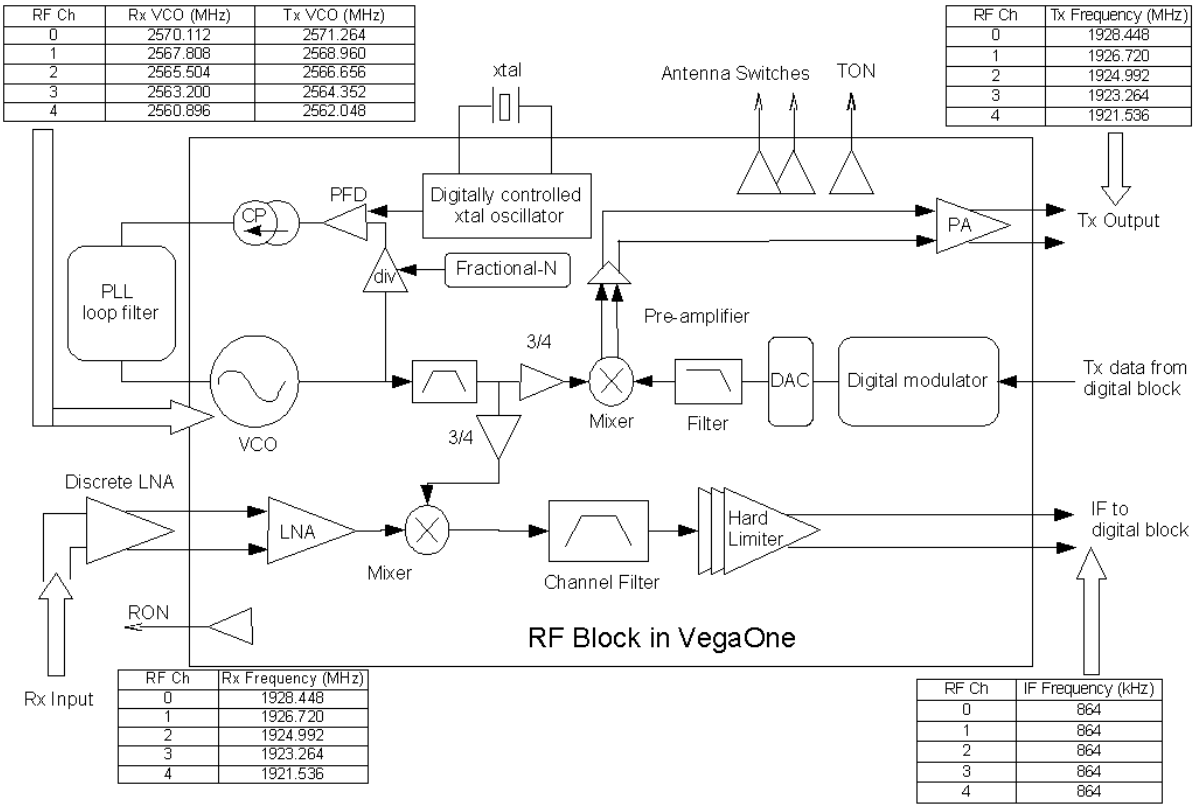

Figure 3.1 RF Block Diagram insides VegaOne

3.1 VCO/PLL Section

The RF block in the VegaOne is designed with an internal transistor to be used for an oscillator. The tank circuit including the inductors and varactor diode are internal to the IC. The VCO operates at 2.5 GHz and is then divided to 1.9 GHz by 4/3 multipliers.

The PLL adapts fractional-N technique to divide down the desired 1.9GHz signal. The baseband crystal frequency (13.824MHz) is buffered by digitally controlled crystal oscillator and then connected to the phase frequency detector (PFD) for the phase-lock loop circuit. The synthesized 2.5 GHz will pass through a bandpass filter to suppress the spurious components. This frequency will then divided by 4 for the sub-harmonics 600MHz and then multiplies by 3 to the 1.9GHz for either Tx or Rx. This method to obtain desired 1.9GHz can reduce the load-pull effect of the power amplifier to the VCO. The modulator uses close-loop modulation.

At the beginning of the guard slot, the VegaOne digital block will turn on the RF block by internal control signaling in TX or RX mode. The VCO then locks and settles during the remaining guard slot time. The PLL is

then switched off and the IC is ready for an active slot. If it is a receive slot, the LNA and mixer will be activated. If it is a TX slot, the pre-amplifier and power amplifier will be turned on.

3.2 TX Chain

The TX DATA is a Gaussian shaped (β=0.5) signal. The data rate for DECT 6.0 is 1152 kbps. The TX DATA is applied to the anode of the tank varactor diode. Since the fractional-N PLL and closed-loop modulation are introduced, the frequency drift during the active slot is promised. The audio signal is first digitized and separated into I, Q channels before modulating to the carrier as a GFSK signal.

The 1.9GHz signal is amplified through a pre-amplifier inside the chip. The output from the driver has differential amplitude of +3dBm. This differential signal is then fed to the internal power amplifier providing an output level of +23dBm. The output of the power amplifier goes through a balun and then to a Tx/Rx diode switches controlled by RON and TON signal. If TON is high, the Tx path will be switched on. Then the signal will go through a bandpass filter to remove higher harmonic and VCO spurious contents (eg: 3.8GHz, 5.7GHz).

The output of the bandpass filter is routed to the antenna switch if any. The VegaOne supports two antenna switches with the fast antenna diversity algorithm. Then, the signal will pass to a permanently soldered antenna with a power level of around +20 dBm conducted in to the antenna as per the FCC guidelines.

3.3 RX Chain

The front end circuitry is the same as the TX Chain. The antenna is connected to the same bandpass filter.

The bandpass filter connects to the TX/RX Switch. In RX mode, RON goes high to switch the diode to RX path. The output of the switch fed into a discrete LNA in order to improve the sensitivity. The output of discrete is fed to the balun to change the signal to differential-ended. Then it is connected to the VegaOne. The LNA input is differential and the LNA matching incorporates phase shifting and noise figure matching. The output of the LNA is connected to the input of the image reject mixer. The mixer's LO is set by the VCO. The output of the mixer is at 864kHz, the IF frequency.

The 864kHz output from the mixer is passed through an internal IF bandpass filter or the channel filter to further improve the channel selectivity. The output of this filter connects to a limiter stage. The limiter amplifies the signal and its output connects to the demodulator which is in the digital block within the same chip. The demodulator FM demodulates the 864kHz to a baseband analog signal. The recovered signal is fed through a low pass post detection filter. The recovered data is then separated to two paths. One is the data going directly to the data slicer. The second is the reference voltage for the data slicer. The 0101 preamble at the beginning of each RX slot is used to determine the average DC voltage of the incoming data. Once locked, this voltage is used by the data slicer as a reference to shape the data. The output of the data slicer is the signal that is delivered to the Baseband section.

4 RF Module Specifications

Specifications marked with * are guaranteed at the nominal testing temperature and voltage on all units with the use of automated production test equipment (ATE).

DECT 6.0 RF Module

	Parameter	Min	Typ	Max	Units
5.1.1	Number of RF Channels Available		5		
5.1.2	RF Channel Spacing		1.728		MHz
5.1.3	26 dB Bandwidth			1.728	MHz
5.1.4	RF Frequency Band	1921.536		1928.448	MHz
5.1.5 *	Transmitter Frequency Offset (over temperature range)	-50		+50	kHz
5.1.6 *	Transmitter Frequency Drift	-15		+15	kHz
5.1.7 *	Base Unit Transmit Power	+16	+19	+20.5	dBm
5.1.8a	**Base Unit Antenna 0 Gain**		**2**		**dBi**
5.1.8b	**Base Unit Antenna 1 Gain**		**2**		**dBi**
5.1.9 *	Frequency Deviation	320	340	380	kHz
5.1.10*	Receiver Sensitivity (BER=0.001)		-98		dBm
5.1.11	Adjacent Channel Rejection (at 1.728MHz offset)	+27	+35		dB
5.1.12	Image Rejection	+13	+25		dB
5.1.13	Intermodulation Rejection	+23	+36		dB
5.1.14	Co-channel Rejection	-10	-6		dB

5 Channel Frequency Plan

For DECT 6.0, the minimum channel frequency used is 1921.536 MHz and the highest channel frequency is 1928.448 MHz. The Tx frequency band should be within the UPCS operating frequency band 1920-1930 MHz.

DECT RF Module

XTAL frequency	**13.824**	**MHz**						
Channel Spacing	**1.728**	**MHz**						
IF frequency	**0.864**	**MHz**						
RF Channel	**TX**		**RX LO**		**TX_VCO**		**RX_VCO**	
0	**1928.448**	**MHz**	**1927.584**	**MHz**	**2571.264**	**MHz**	2570.112	**MHz**
1	**1926.72**	**MHz**	**1925.856**	**MHz**	**2568.96**	**MHz**	2567.808	**MHz**
2	**1924.992**	**MHz**	**1924.128**	**MHz**	**2566.656**	**MHz**	2565.504	**MHz**
3	**1923.264**	**MHz**	**1922.4**	**MHz**	**2564.352**	**MHz**	2563.2	**MHz**
4	**1921.536**	**MHz**	**1920.672**	**MHz**	**2562.048**	**MHz**	2560.896	**MHz**