1.0 GENERAL INFORMATION

The following Application for FCC Certification of a Class B Digital Device is prepared on behalf of ALINCO, INC. in accordance with Part 15.247 of the Federal Communications Commissions rules and regulations. The Equipment Under Test (EUT) was the ALINCO, INC. Model: XE642T Direct sequence system Spread spectrum transceiver unit, FCC ID: EUGXE642T. The test results reported in this document relate only to the item that was tested.

All measurements contained in this Application were conducted in accordance with ANSI C63.4 Methods of Measurement of Radio Noise Emissions, 1992. The instrumentation utilized for the measurements conforms to the ANSI C63.4 standard for EMI and Field Strength Instrumentation. Some accessories are used to increase sensitivity and prevent overloading of the measuring instrument. These are explained in the appendix of this report. Calibration checks are performed regularly on the instruments, and all accessories including the high pass filter, preamplifier and cables.

All radiated and conducted emissions measurement were performed manually at Rhein Tech, Incorporated. The radiated emissions measurements required by the rules were performed on the three meter, open field, test range maintained by Rhein Tech Laboratories, Inc., 360 Herndon Parkway, Suite 1400, Herndon, Virginia 20170. Complete description and site attenuation measurement data have been placed on file with the Federal Communications Commission. The power line conducted emission measurements were performed in a shielded enclosure also located at the Herndon, Virginia facility. Rhein Tech, Labs, Inc. is on the FCC accepted lab list as a Facility available to do measurement work for others on a contract basis.

1.1 PRODUCT DESCRIPTION

This unit is consisted of the frequency synthesized circuit, power circuit, transmitter circuit, receiver circuit, and control circuit. Following are the description of each unit.

1. Frequency Synthesized Circuit (PLL)

When the power is turned on, IC501 (PLL IC) is received the frequency data through IC9 (micro processor.) The 22 MHz of frequency is generated by IC24 and will be divided into 100 kHz. This frequency signal can be used for both the 1st local (2,288.5 MHz) and 2nd local (307MHz) as a reference signals. The output signal of 2,288.5MHz from the VCO501, the VCO unit for the 1st local oscillator, will be injected to IC11 (the down converter for receiver), IC5 (the up converter for transmitter), and the PLL circuit. The loop filter is consisted of R518, R519, C534, and C537. The VCO circuit for the 2nd local oscillator utilizes the clap oscillator circuit. The output frequency will be changed by varying the DC voltage applied to the D501 diode. The loop filter is consisted of R504, R509, C510, C514, and C520. The output signal from the VCO will be injected to IC13, a demodulator on the IF section through the high-pass filter (L504, C509), low-pass filter (L502, C504, C517, C518) to suppress the spurious signals. When either VCO is unlocked, the #10 of IC501 will go Low and will output the unlock status signal to the micro processor. In the meantime, the ACPU will inhibit to transmit from the unit.

2. Clock Circuit, Power Circuit

IC24 and X1 (crystal) will generate the reference frequency for the PLL, and other clock frequencies for the each circuit for X1 has been designed to minimize the frequency drift. The reference frequency can be readjusted by TC1 (trimmer capacitor.) The clock frequency of 11 MHz divided by IC10-A will be used as a clock frequency for the micro-processor (IC9.) IC25 (voltage regulator) will supply 3.3 V of DC voltage to drive IC3 (antenna switch) and IC24 (spread spectrum baseband processor.) IC 21 is DC-DC

converter and generate -4.4 V of DC voltage to supply as a bias voltage of the power amplifier. Each circuit has been built-in the dc-coupling circuit to get maximum stability.

3. Transmitter Circuit

The TX Data will be input synchronized with clock signal that come from the TSDCK terminal of the IC24. The input serial data will converted as 2 bits of I,Q parallel data and will be modulated as either the BPSK mode or QPSK signal. In this circuit, the differential modulator has been used because of its simple circuitry. Then the output signals will be led to the spread modulation circuit. The spread code is a 11 Mbps, 11chip Barker Series. The below is a block diagram of the circuit. The modulated I, Q channels of signals will be applied to the IC13, modulator/de-modulator. After coming through the base-band filter (cut-off frequency 8.8 MHz, 5th butter-worth; cut-off 30dB/Oct.) to limit the bandwidth, the signals will be converted to 153.5 MHz of the IF signal and will be output from IC13. The output transmit IF signals coming from IC13 will be amplified by IC7 (IF amplifier). Then the side-robe of the signals and will be suppressed by FL2 (a filter with 11 MHz of bandwidth.) The output power will be also adjusted by IC7. The IF signals with limited bandwidth will be converted to 2,442 MHz of the operation frequency mixed with the 1st local oscillator signal. After coming through FL3 (filter), the output signals will be amplified by the driver amplifier, power amplifier (IC6, IC4) and fed to IC3 (antenna switch) and the antenna connector.

4.Reciever Circuit

The received signal at the antenna connector will be injected to the low noise amplifier (LNA), that is a part of IC11 (down converter) through FL1 (filter) and IC3 (antenna switch). Output from the LNA will be amplified by IC12 (RF amplifier) and will be fed to the mixer, a part of IC11. Being mixed with the 1st local oscillator output coming from the PLL circuit, it will be converted to the 153.5 MHz of the IF signal. IF signal output from IC11 will be rejected any nearby unwanted signals by FS5 (filter with 11 MHz of bandwidth.) Then it will be led to IC13 (limitter amplifier.) IC13 is a two stage of the limitter amplifier and has 80dB of total gain. The limitter output will be input to the demodulator, a part of IC3, and will be converted with two channels, (I, Q signals) of baseband signals by the carriers that has 90 degrees of phase shift coming from the 2nd local oscillator. The I,Q of baseband signal output from IC13 will be converted with digital data by the A/D converter that is a 4 bit converter and operates with 22 MHz of sampling frequency. The digital ouput data from IC14 will be led to IC24. It is a Spread Spectrum Baseband Processing IC. These I, Q signals will be multiplied by the NCO (Numeric Controlled Oscillator), a part of IC24. As a result, frequency offset between the transmitter and receiver will be rejected. Then these I, Q signals will be led to the digital matched filter and will be reverse-spreaded. In the meantime, only real I, Q data signal will be extracted through it. Consequently, the de-modulated serial data can be obtained after passing through the differential de-modulator and parallel/serial converter.