1.2 PRODUCT DESCRIPTION

Overview

This device is a Wireless Remote-controller (referred to as "the device") for an electronic measuring device used in construction / interior decoration industry.
The main device (electronic measuring device) that employs laser technology will be separately applied for the FCC type-approval so it is excluded from this volume. THIS APPLICATION IS ONLY FOR THE CONTROLLER.
The frequencies used are 9 channels selectable manually as follows.
426.2625,429.3000,429.3625,429.4375,429.5250,429.6500,429.6750,429.7375MHz.
The device is easy to use and low power. When any key on the device is pressed by user then it turns and key operation is not done for certain period of time, the device is going to sleep condition.
This device has function of inhibit to transmit to avoid interference on same frequency.

Dimension, weight

Dimension 157 (H) x 64 (W) x 25 (D)
Weight 0.24kg

Frequency and Modulation system

Receiver system: Double-conversion super-heterodyne
The 1st IF frequency: 21.7MHz
The 2nd IF frequency: 450kHz

Transmitter system: Pre-mix (Single-conversion)
The 1st Local oscillator: X'tal 10.85MHz
The 2nd Local oscillator: Frequency synthesizer

Modulation system: Variable reactance frequency modulation

Circuits description

This device consists of the control circuits and RF UNIT including frequency-synthesized circuits, power circuits, receive circuits for carrier detect and transmit circuits. Following are the description of each unit.
Control circuits
1.1 General
Control circuits consist of an 8-bits CMOS CPU (IC3) and peripheral circuits.
Reset IC (IC2) outputs "H" when the circuits turned on.
Voltage detector IC (IC4) outputs "H" when Vcc line exceeds its threshold voltage.
11 tact-switches (SW1 – SW11) are function switch.
Rotary switch (SW12) decides operation frequency.
X'tal Oscillator (X2) is master CPU clock (4.9152MHz).
X'tal Oscillator (X1) work at CPU sleep mode.
Connector (CN1) is connected battery.
Connector (CN2) is connected program writer when CPU (IC3) program.
Connector (CN3) is connected radio unit.
LED indicator D3 is blink RED when carrier sense or PLL unlock.
LED indicator D3 is blink GREEN when transmitting.
LED indicator D4 is indicated RED when status "X".
LED indicator D5 is indicated RED when status "Y".
LED indicator D6 is blinked when low battery.

1.2 reset circuit

Reset circuits consisted of RESET IC (IC2), R38 and C16. This reset circuit resets the CPU (IC3) with RESET IC (IC2). The RESET IC (IC2) outputs "H" when installing batteries into the body and the "Vcc" line exceeds its threshold voltage. Output signal from RESET IC (IC2) is applied to the CPU RESET port (IC3 #12).

Low battery Indicator

When the battery voltage becomes lower than 3.3V, Voltage detector IC (IC2) outputs "L" and the CPU (IC3) port PB7 becomes "L". When the port PB7 of the CPU (IC3) receives "L", the CPU outputs pulse, 1Hz duty (ON/OFF) cycle 20%, through the port P64 of the CPU for low battery indication, and the CPU inhibits to data transmission due to avoid CPU miss-operations. The pulse from the port P64 of the CPU is applied to LED (D8) for low battery indication.

Frequency synthesized circuits

2.1 VCO circuits

The VCO circuit is consisted of oscillator Q112, variable capacitor diode D105, D106 and Buffer amplifier Q111. PLL is designed for Pre-mix, because output frequency on transmit and receive is same frequency.

Output signal level from buffer amplifier is –12dBm. And Supply voltage to VCO circuits is regulated for 2.2V by regulator IC (IC101).

2.2 PLL circuits

When function key is pushed, PLL IC (IC102) is received the frequency data from CPU (IC3) through CN3 #5, #6, #7.

The 21.25MHz of frequency X101 is generated by 2nd local oscillator, a part of PLL IC (IC102), and will be divided into 12.5kHz. This frequency signal is used for the 1st local frequency as a reference signal.

The output signal from Q111, for the 1st local oscillator, will be injected to transmit mixer Q104, Receiver 1st mixer Q108, and the PLL IC (IC102 #2).

The loop filter is consisted of R170, R171, R172, R173, C145, C175, C176, C178, C188 and C189. Varying the DC voltage applied to the variable capacitor diode D105, D106 will change the output frequency.

2.3 Unlock detector circuits

When VCO is unlocked, the PLL IC (IC102 #7) will go "H" and will output UNLOCK status signal to the port P10 of the CPU (IC3 #67) through CN3 #18. In the meantime, the CPU will inhibit to transmit from the unit.

Power circuits

When the batteries are installed into the body, DC 4.5V typically is applied to the CPU through CN1 directly.

When any switch is pressed, the CPU (IC3) enters into active condition and "H" is applied to the GATE of the MOS-FET (Q1) through the port P14 of the CPU (IC3 #68).

When MOS-FET (Q1) becomes ON, DC 4.5V is applied to VCO circuits and PLL circuits in RF UNIT through CN3 and the R3V line becomes ON. And R3V is applied to receiver circuits and carrier sense circuits.

When the controller is transmitting, power line for transmit (T3V) is applied to the 1st local oscillator circuits and the modulation circuits through Q114.

The all circuits of the RF unit is regulated to 2.2V by regulator IC (IC101).

Receiver circuits

Block diagram of receiver circuits

Front-end

The received signal at the antenna connector will be injected to the RF amplifier Q102 through SAW-BPF (Band Pass Filter FL103) and antenna switch (D103). The received signal will be rejected any unwanted signals by SAW-BPF (FL103). Output from the RF amplifier will be fed to the 1st mixer (Q108).

Receiver 1st IF

Amplified signal being mixed with the 2nd local oscillator output coming from the PLL circuits, it will be converted to the 21.7MHz of the receiver 1st IF signal.

IF signal output from mixer (Q108) will be rejected unwanted signals by Monolithic-filter (FL102). Then it will be led to the IF amplifier (Q109). It output signal will be led to IF IC (IC103).

IF amplifier IC

IF IC (IC103) is consisted of the receiver 2nd mixer, the limmiter amplifier, the FM de-modulator, and RSSI circuit.

The IF signal output from the IF amplifier Q109 will be input to the receiver 2nd mixer, a part of IC103.Being converted with 2nd local oscillator output coming from X'tal oscillator, a part of the PLL IC (IC102). Through IC102 #17. It will be converted to 450kHz of the receiver 2nd IF frequency.

The receiver 2nd IF signals will be rejected unwanted signals by ceramic-filter (FL101). Then it will be led to the limmiter amplifier, a part of IC103. It output signal will be led to the FM de-modulator circuits.

Carrier sense circuits

In a FM receiver, audio noise is produces in its IF and AF circuits when receiving no RF signals. However, these noises are suppressed when receiving a signal. The carrier sense circuit acts in accordance with this phenomenon.

The carrier sense circuits is consisted of the noise amplifier using operational amplifier (IC301: B), Detector consisting Diode (D111), LPF consisting R306 and C137 and comparator (IC105).

The noise in the de-modulated signal from IF IC (IC103) will be fed to noise amplifier, and will be amplified by the noise amplifier (IC301: B). Then it signals are detected by D111 and will be integrated by R306 and C137.

Output signal from the integrator will be fed to comparator, and is compared with reference voltage.

Reference voltage is adjusted by VR102 for Q112 turned ON with 2uV at antenna input.

The carrier sense output signal from Q112 is applied to the CPU P92 port (IC3 #15) through CN3 #11.

When carrier sense outputs "L", transmit operation inhibit from CPU program.

Transmit circuits

Block diagram of transmitter circuits

5.1 Modulator

The modulation circuits is consisted of the IDC (limmiter), LPF, the 1st local oscillator and the multiplexer. The IDC is consisted of two operational amplifiers (IC501: A,B), and the

LPF is consisted of two operational amplifiers (IC502:A,B). The 1st local oscillator is consisted of Q106, X103, C127, C128, C130, L111, D101 and R126.

The TX DATA will be led to the IDC from port P22 of the CPU (IC3 #53) through CN3 #17. And TX DATA signal is amplified by the IDC (amplifier). The amplitude of this signal is limited by the IDC circuits, and adjust the Variable register VR501 for 2kHz of deviation.

The output signal from the IDC circuits will be led to the LPF circuit. A character of the LPF is the 5th butter-worth with 1.2kHz cut-off frequency.

The output signal from the LPF will be led to the modulation input of the oscillator (Q106).

The 1st local oscillator frequency is adjusted by variable register VR103 for 10.85MHz. And output signal from this 1st local oscillator will be led to the multiplexer (Q105).

5.2 The TX mixer

The output signal from Q105, for the TX 1st local oscillator, will be injected to transmit mixer Q104. The output signal from the TX mixer (Q104) will be converted to the 434.92MHz of the transmission RF signal.

RF signal output from mixer (Q104) will be rejected unwanted signals by BPF, which is consisted of C and L. Then it will be led to the 3 stage RF amplifier (Q101-Q103). And it signal is amplified by each RF amplifiers.

And it signal from RF amplifier will be led to SAW-BPF, will be rejected unwanted signals, and output signal from SAW-BPF will be output through the antenna connector CN1.

RF output power is adjusted variable register VR101 for 0.15mW at antenna connector, the antenna gain is approximately -8dBi, and radiation level from antenna is approximately 8300uV/m.

And deviation of the RF power is not occur, because the all circuits of the RF unit is regulated to 2.2V by regulator IC (IC101).