CIRCUIT DESCRIPTION

1) Receiver System

The receiver system is a double superheterodyne system with a 21.7 MHz first IF and a 450 kHz second IF.

1. Front End

The received signal at any frequency in the 130.00- to 173.995-MHz range is passed through thelow-pass filter (L2, L3, L11, C13, C14, C15 and C60) and tuning circuit (L16 and D15), and amplified by the RF amplifier (Q11). The signal from Q11 is then passed through the tuning circuit (L17, L18, L19 and varicaps D13, D14 and D16) and converted into 21.7 MHz by the mixer (Q9). The tuning circuit, which consists of L16, L17, varicaps D15 and D13, L18, L19, varicaps D14 and D16, is controlled by the tracking voltage form the CPU so that it is optimized for the reception frequency. The local signal from the VCO is passed through the buffer (Q13), and supplied to the source of the mixer (Q9). The radio uses the lower side of the superheterodyne system.

2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (XF1, XF2) selects 21.7 MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q10) then amplifies the signal of the selected frequency.

3. Demodulator Circuit

After the signal is amplified by the first IF amplifier (Q10), it is input to pin 16 of the demodulator IC (IC5). The second local signal of 21.25 MHz (shared with PLL IC reference oscillation), which is oscillated by the internal oscillation circuit in IC1 and crystal (X1), is input through pin 1 of IC5. Then, these two signals are mixed by the internal mixer in IC5 and the result is converted into the second IF signal with a frequency of 450 kHz. The second IF signal is output from pin 3 of IC5 to the ceramic filter (FL1), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC5 through pins 5.

The second IF signal input via pin 5 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC5, and output as an audio signal through pin 10.

4. Audio Circuit

The audio signal from pin 10 of IC5 is compensated to the audio frequency characteristics in the de-emphasis circuit (R104, R103, C122, C121) and amplified by the AF amplifier (Q26). The signal is then input to pin 2 of the electronic volume (IC4) for volume adjustment, and output from pin 1. The adjusted signal is sent to the audio power amplifier (IC3) through pin 2 to drive the speaker.

5. Squelch Circuit

The signal except for the noise component in AF signal of IC5 is cut by the active filter inside IC. The noise component is amplified and rectified, then converted to the DC voltage to output from pin13 of IC5. The voltage is led to pin 2 of CPU and compared with the setting voltage. The squelch will open if the input voltage is lower than the setting voltage.

2) Transmitter System

1. Modulator Circuit

The audio signal is converted to an electric signal in either the internal or external microphone, and input to the microphone amplifier (IC7). IC7 consists of two operational amplifiers; one amplifier (pins 5, 6, and 7) is composed of pre-emphasis and IDC circuits and the other (pins 1, 2, and 3) is composed of a splatter filter. The maximum frequency deviation is obtained by VR202 and input to the cathode of the varicap of the VCO, to change the electric capacity in the oscillation circuit. This produces the frequency modulation.

2. Power Amplifier Circuit

The transmitted signal is oscillated by the VCO, amplified by the pre-drive amplifier (Q4) and drive amplifier (Q3), and input to the final amplifier (Q2). The signal is then amplified by the final amplifier (Q2) and led to the antenna switch (D1) and low-pass filter (L5, L4, L3, L2, C16, C15, C14 and C13), where unwanted high harmonic waves are reduced as needed, and the resulting signal is supplied to the antenna.

3. APC Circuit

Part of the transmission power from the low-pass filter is detected by D6, converted to DC, and then amplified by a differential amplifier. The output voltage controls the bias voltage from the source of Q2 and Q3 to maintain the transmission power constant.

3) PLL Synthesizer Circuit

1. PLL

The dividing ratio is obtained by sending data from the CPU (IC9) to pin 2 and sending clock pulses to pin 3 of the PLL IC (IC1). The oscillated signal from the VCO is amplified by the buffer (Q5) and input to pin 6 of IC1. Each programmable divider in IC1 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

2. Reference Frequency Circuit

The reference frequency appropriate for the channel steps is obtained by dividing the 21.25 MHz reference oscillation (X1) by 4250 or 3400, according to the data from the CPU (IC9). When the resulting frequency is 5 kHz, channel steps of 5, 10, 15, 20, 25, 30, and 50 kHz are used. When it is 6.25 kHz, the 12.5 kHz channel step is used.

3. Phase Comparator Circuit

The PLL (IC1) uses the reference frequency, 5 or 6.25kHz. The phase comparator in the IC1 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25kHz, which is obtained by the internal divider in IC1.

4. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 8) of IC1 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

5. VCO Circuit A Colpitts oscillation circuit driven by Q1 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC9) and

PLL circuit is input to the varicaps (D32 and D34). This change the oscillation frequency, which is amplified by the VCO buffer (Q5) and output from the VCO unit.

4) CPU and Peripheral Circuits

1. LCD Display Circuit

The CPU turns ON the LCD via segment and common terminals with 1/4 the duty and 1/4 the bias, at the frame frequency is 112.5Hz.

2. Display Lamp Circuit

When the LAMP key is pressed, "H" is output form pin 50 of CPU (IC9) to the bases of Q12. Q12 then turn ON and the LEDs (D12 and D17) light.

3. Reset and Backup

When the power form the DC jack or external battery increases from Circuits 0 V to 2.5 or more, "H" level reset signal is output form the reset IC (IC11) to pin 33 of the CPU (IC9), causing the CPU to reset. The reset signal, however, waits at 100, and does not enter the CPU untilthe CPU clock (X2) has stabilized.

4. S(Signal) Meter Circuit

The DC potential of pin 8 of IC5 is input to pin 1 of the CPU (IC9), converted from an analog to a digital signal, and displayed as the S-meter signal on the LCD.

5. DTMF Encoder

The CPU (IC9) is equipped with an internal DTMF encoder. The DTMF signal is output from pin 10, through R102 and R158 (for level adjust-ment), and then through the microphone amplifier (IC7), and is sent to the varicap of the VCO for modulation. At the same time, the monitor-ing tone passes through the AF circuit and is output form the speaker.6. CTCSS Encoder The CPU (IC9) is equipped with an internal tone encoder. The tone signal (67.0 to 250.3 Hz) is output form pin 9 of the CPU to the varicap D3 of the VCO for modulation.

6. Tone Encoder

The CPU (IC9) is equipped with an internal tone encoder.The tone signal (67.0 to 250.3 Hz) is output from pin 9 of the CPU to the varicap of the VCO for modulation.

7. DCS Encoder

The CPU (IC9) is equipped with an internal DCS code encoder. The code (023 to 754) is output from pin 9 of the CPU to the varicap (D3) of the PLL reference oscillator. When DCS is ON, DCS MUTE circuit (Q15-ON, Q18-ON, Q16-OFF) works. The modulation activates in X1 side only.

8. CTCSS, DCS Decoder

The voice band of the AF output signal from pin 10 of IC5 is cut by sharp active filter IC8 (VCVS) and amplified, then led to pin 4 of CPU. The input signal is compared with the programmed tone frequency code in the CPU. The squelch will open when they match.

9. Clock Shift

In the unlikely event that CPU clock noise is present on a particular operating frequency programmed into the radio, you can shift the CPU clock frequency to avoid

the CPU clock-noise. The output signal from pin 31 of the CPU turns on Q30. Then the oscillation frequency of X2 will be shifted about 300 ppm.

ＤＪ－１９５　ＦＣＣ／ＣＥ申請資料

1999. 2. 25

アルインコ（株）電子品質保証部　清光

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ＦＣＣ申請チェックリスト

機種名：ＤＪ-195Ｔ

NO	チェック項目	数量	開発確認	USA確認
1	ブロックダイヤグラム	2部	㊞	
2	回　路　図	2部	㊞	
3	測定データ（設計基準1）	1部	㊞	
4	申請セット（量産セットと同一仕様）	1台	㊞	
5	付属マイク	1個	／	
6	電源ケーブル	1個	—	
7	定格銘板（本体に貼付け）	1個	㊞	
8	アンテナ（ハンディ機のみ）または専用測定ケーブル	1個	㊞	
9	変調入力用マイクプラグ付コード（ハンディ機のみ）	1個	—	
10	バッテリーパック（ハンディ機のみ）	1個	㊞	
11	不正規項目一覧表（量産品との相違）	1部	㊞	
12	回路説明	1部	㊞	

DJ－195 FCC／CE検査結果要項

アルインコ(株)電子品質保証部

測定検査項目		機種 DR－１９５E／T				Date 1999.2.22	
測定項目	周波数	規格	T000491	T000490	T000491	T000491	
1 受信感度 12dB SINAD	135.050 145.050 173.950	-6.0dBμ以下 -8.0dBμ以下 -6.0dBμ以下	-9.5 -10.6 -9.1	-10.3 -10.8 -9.9	-10.4 -11.2 -9.38	-10.4 -10.7 -10.2	
2 受信歪 FM	145.0500	4%以下	1.1	1.05	1.7	1.3	
3 受信S／N	145.0500	40dB 以上	47	47	47	45	
4 ｽｹﾙﾁ 感度	145.0500	-13dBμ以下	-16.5	-17.0	-18.0	-16.0	
5 ﾀｲﾄｽｹﾙﾁ	145.0500	-6dBμ以上	-3.0	-3.0	-4.0	-4.0	
6 低周波出力	145.0500	1.55V(300mW)	1.70	1.68	1.72	1.68	
7 不要輻射	145.995	-57dBm以下	-82	-82	-81	-83	
1 送信出力 (HI) (LOW)	135.050 145.050 173.950 145.050	4 ～ 5W 4 ～ 5W 4 ～ 5W 0.3～0.6W	4.62 4.46 4.46 0.50	4.63 4.46 4.44 0.50	4.95 4.80 4.70 0.40	4.90 4.75 4.65 0.50	
2 消費電流 H	145.050	1.3 A以下	1.07	1.10	1.06	1.10	
3 周波数偏差	145.050	±1.0KHz	-0.05	-0.01	+0.04	-0.04	
4 スプリアス (HI) (LOW)	144.000 145.000 145.995 144.000 145.000 145.995	60dB以上 60dB以上 60dB以上 60dB以上 60dB以上 60dB以上	69 69 69 75 74 75	71 71 71 78 78 78	69 70 71 70 70 68	70 70 71 70 70 69	
5 DEV [25mV]	145.050	4.5K±500Hz	4.39	4.40	4.40	4.45	
6 変調歪[1.5k]		4% 以下	1.725	1.80	1.79	1.78	
7 送信S/N	BPF300Hz-3k	40dB以上	48	49	48	49	
8 DTMF [1]		2.2～3.7kHz	2.72	2.71	2.36	2.76	
9 DTMF [D]		2.2～3.7kHz	3.22	3.05	2.82	2.84	
10 CTCSS [67.0]	LPF500Hz	0.4～1.0Hz	0.79	0.82	0.71	0.89	
11 CTCSS [88.5]	LPF500Hz	0.4～1.2Hz	0.88	0.90	0.85	0.92	
12 CTCSS[250.3]	LPF500Hz	0.4～1.0Hz	0.79	0.81	0.76	0.82	
13 DCS [255]	LPF500Hz	0.4～1.2Hz	0.6	0.68	0.65	0.70	
14 TBURST[1750]		2.2～3.7kHz	2.63	2.51	2.50	2.57	

ＦＣＣ申請セット性能確認１．

機種名：DJ-195T

NO	チェック項目	開発確認	USA確認
1	送信スプリアスは許容値内か。（30M ～225MHZの送信域） 送信出力 25W 以上：60dB以上 送信出力 25W 未満：40dB以上かつ25uW以内（但し10uW以下にする必要はない） （例）50W 機 → 60dB以上　1W機 → 46dB以上 10W 機 → 56dB以上　0.5W機 → 43dB以上 5W 機 → 53dB以上　0.05W機 → 37dB以上		
2	受信スプリアスは許容値内に入っているか。　規格　－60dB以下		
3	送信出力は許容値内に入っているか。		
4	高次スプリアスの他に近接のスプリアスはないか。		
5	ローパワーでのスプリアスも確認したか。		
6	最大周波数偏移は許容値内に入っているか。		
7	付属マイクで送信できるか。又変調がのるか。		
8	付属の電源ケーブルで試験をしたか。		
9	各基板、ケース等は正しくビス止めされているか。		
10	シフト・スプリット．リバースモードでオフバンド送信にならないか。		
11	オフバンド送信されない事。送信拡張されていない事。		
12	電源ON/OFF繰り返し、電源立上り立下りゆっくりした時誤動作（誤送信）はないか。		
13	周波数ズレは１時間以上で確認したか。		
14	同軸ケーブルの長さを変えて出力が変化しない事。		